

# CD4027B Types

## CMOS Dual J-K Master-Slave Flip-Flop

High-Voltage Types (20-Volt Rating)

■ CD4027B is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J, K, Set, Reset, and Clock input signals. Buffered Q and  $\bar{Q}$  signals are provided as outputs. This input-output arrangement provides for compatible operation with the RCA-CD4013B dual D-type flip-flop.

The CD4027B is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.

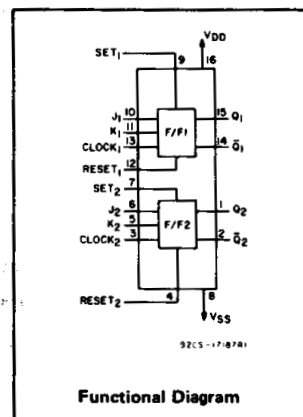
The CD4027B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline package (NSR suffix), and in chip form (H suffix).

### Features:

- Set-Reset capability
- Static flip-flop operation — retains state indefinitely with clock level either "high" or "low"
- Medium speed operation — 16 MHz (typ.) clock toggle rate at 10 V
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
  - 1 V at  $V_{DD} = 5$  V
  - 2 V at  $V_{DD} = 10$  V
  - 2.5 V at  $V_{DD} = 15$  V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Applications:

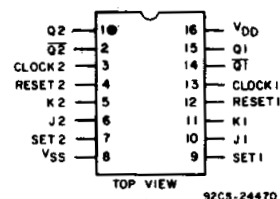
- Registers, counters, control circuits



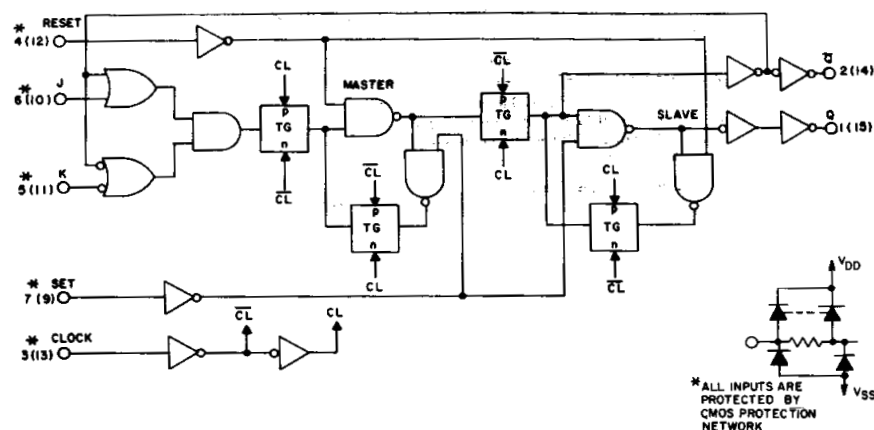
Functional Diagram

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )	
Voltages referenced to $V_{SS}$ Terminal)	–0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5V to $V_{DD} + 0.5$ V
DC INPUT CURRENT, ANY ONE INPUT	$\pm 10$ mA
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$	500mW
For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$	Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$	100mW
OPERATING-TEMPERATURE RANGE ( $T_A$ )	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
STORAGE TEMPERATURE RANGE ( $T_{stg}$ )	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79$ mm) from case for 10s max	$+265^\circ\text{C}$



### TERMINAL ASSIGNMENT



PRESENT STATE					NEXT STATE	
J	K	S	R	Q	Q	Q-bar
1	x	0	0	0	1	0
x	0	0	0	1	1	0
0	x	0	0	0	0	1
x	1	0	0	1	0	1
x	x	0	0	x	← NO CHANGE	
x	x	1	0	x	1	0
x	x	0	1	x	0	1
x	x	1	1	x	1	1

LOGIC 1 = HIGH LEVEL  
LOGIC 0 = LOW LEVEL  
x = LEVEL CHANGE  
X = DON'T CARE

92CS-27551R1

Fig. 1 – Logic diagram and truth table for CD4027B (one of two identical J-K flip flops).

## CD4027B Types

**RECOMMENDED OPERATING CONDITIONS at  $T_A = 25^\circ\text{C}$ , Except as Noted.**  
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V <sub>DD</sub> (V)	LIMITS		UNITS
		All Packages		
		Min.	Max.	
Supply-Voltage Range (For T <sub>A</sub> = Full Package Temperature Range)	—	3	18	V
Data Setup Time t <sub>S</sub>	5 10 15	200 75 50	— — —	ns
Clock Pulse Width t <sub>W</sub>	5 10 15	140 60 40	— — —	ns
Clock Input Frequency (Toggle Mode) f <sub>CL</sub>	5 10 15	dc	3.5 8 12	MHz
Clock Rise or Fall Time t <sub>rCL</sub> *, t <sub>fCL</sub>	5 10 15	— — —	45 5 2	μs
Set or Reset Pulse Width t <sub>W</sub>	5 10 15	180 80 50	— — —	ns

\* If more than one unit is cascaded in a parallel clocked operation,  $t_{rCL}$  should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

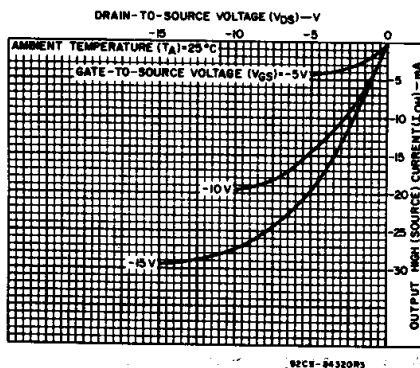


Fig. 4 - Typical output high (source) current characteristics.

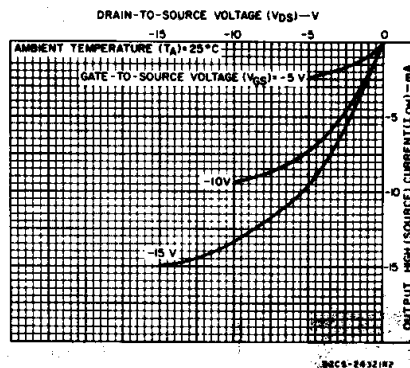


Fig. 5 - Minimum output high (source) current characteristics.

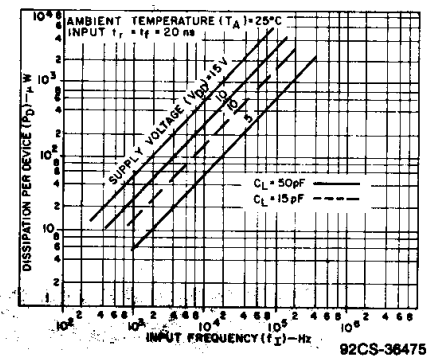


Fig. 6 - Typical power dissipation vs. frequency.

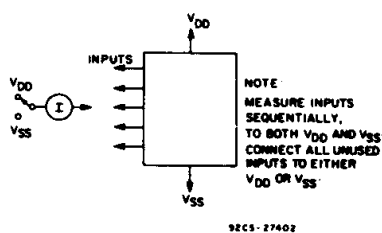


Fig. 7 - Input current test circuit.

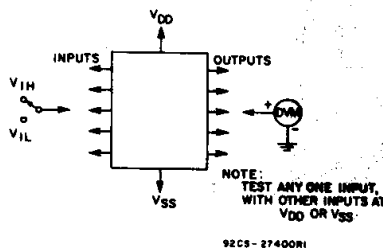


Fig. 8 - Input-voltage test circuit.

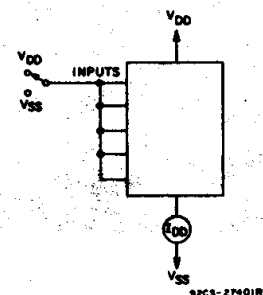


Fig. 9 - Quiescent device current test circuit.

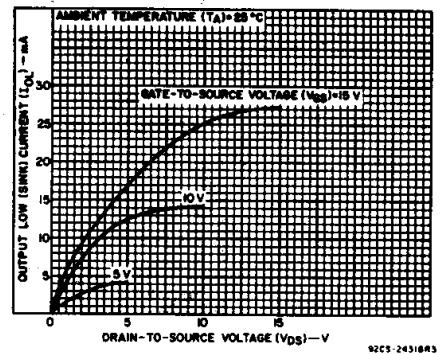


Fig. 2 - Typical output low (sink) current characteristics.

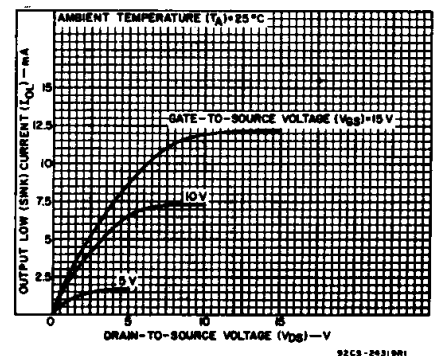


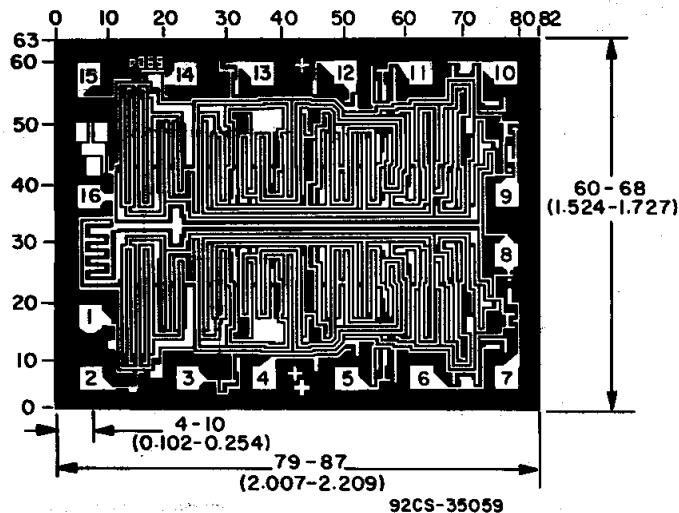
Fig. 3 - Minimum output low (sink) current characteristics.

3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

## CD4027B Types

### STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS	
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25				
								Min.	Typ.	Max.		
Quiescent Device Current, I <sub>DD</sub> Max.	—	0.5	5	1	1	30	30	—	0.02	1	μA	
	—	0.10	10	2	2	60	60	—	0.02	2		
	—	0.15	15	4	4	120	120	—	0.02	4		
	—	0.20	20	20	20	600	600	—	0.04	20		
Output Low (Sink) Current, I <sub>OL</sub> Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA	
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	—		
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	—		
	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—		
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—		
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—		
Output High (Source) Current, I <sub>OH</sub> Min.	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—		
	Output Voltage: Low-Level, V <sub>OL</sub> Max.	—	0.5	5	0.05				—	0	0.05	V
		—	0.10	10	0.05				—	0	0.05	
—		0.15	15	0.05				—	0	0.05		
Output Voltage: High-Level, V <sub>OH</sub> Min.	—	0.5	5	4.95				4.95	5	—		
	—	0.10	10	9.95				9.95	10	—		
	—	0.15	15	14.95				14.95	15	—		
Input Low Voltage, V <sub>IL</sub> Max.	0.5, 4.5	—	5	1.5				—	—	1.5	V	
	1.9	—	10	3				—	—	3		
	1.5, 13.5	—	15	4				—	—	4		
Input High Voltage, V <sub>IH</sub> Min.	0.5, 4.5	—	5	3.5				3.5	—	—		
	1.9	—	10	7				7	—	—		
	1.5, 13.5	—	15	11				11	—	—		
Input Current, I <sub>IN</sub> Max.	—	0.18	18	±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	μA	



Dimensions in millimeters are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$ ).

Dimensions and Pad Layout for CD4027BH

## CD4027B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20\text{ ns}$ ,  
 $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	VDD (V)	LIMITS			UNITS
		All Packages			
		Min.	Typ.	Max.	
Propagation Delay Time: Clock to Q or $\bar{Q}$ Outputs $t_{PHL}, t_{PLH}$	5	—	150	300	ns
	10	—	65	130	
	15	—	45	90	
Set to Q or Reset to $\bar{Q}$ $t_{PLH}$	5	—	150	300	ns
	10	—	65	130	
	15	—	45	90	
Set to $\bar{Q}$ or Reset to Q $t_{PHL}$	5	—	200	400	ns
	10	—	85	170	
	15	—	60	120	
Transition Time $t_{THL}, t_{TLH}$	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
Maximum Clock Input Frequency# (Toggle Mode) $f_{CL}$	5	3.5	7	—	MHz
	10	8	16	—	
	15	12	24	—	
Minimum Clock Pulse Width $t_W$	5	—	70	140	ns
	10	—	30	60	
	15	—	20	40	
Minimum Set or Reset Pulse Width $t_W$	5	—	90	180	ns
	10	—	40	80	
	15	—	25	50	
Minimum Data Setup Time $t_S$	5	—	100	200	ns
	10	—	35	75	
	15	—	25	50	
Clock Input Rise or Fall Time $t_{rCL}, t_{fCL}$	5	—	—	45	$\mu$ s
	10	—	—	5	
	15	—	—	2	
Input Capacitance $C_I$		—	5	7.5	pF

# Input  $t_r, t_f = 5\text{ ns}$ .

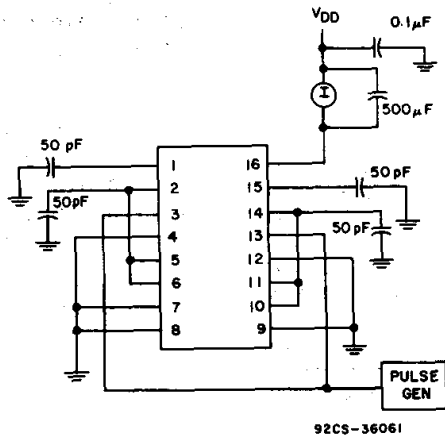


Fig. 13—Dynamic power dissipation test circuit.

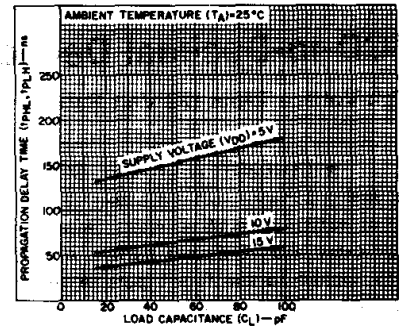


Fig. 10—Typical propagation delay time vs. load capacitance (CLOCK or SET to Q, CLOCK or RESET to  $\bar{Q}$ ).

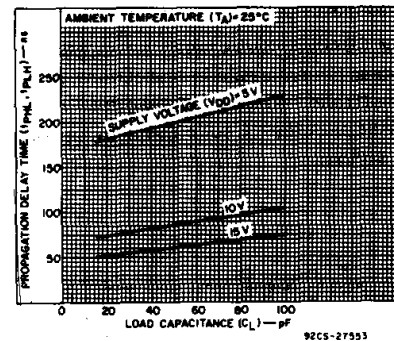


Fig. 11—Typical propagation delay time vs. load capacitance (SET to  $\bar{Q}$  or RESET to Q).

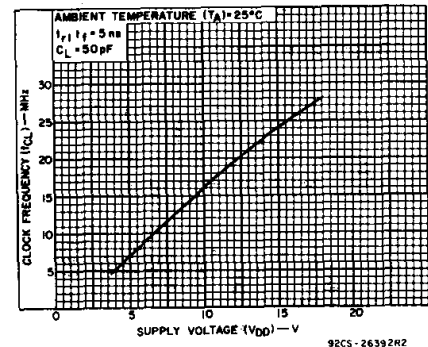


Fig. 12—Typical maximum clock frequency vs. supply voltage (toggle mode).

## **IMPORTANT NOTICE**

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments  
Post Office Box 655303  
Dallas, Texas 75265