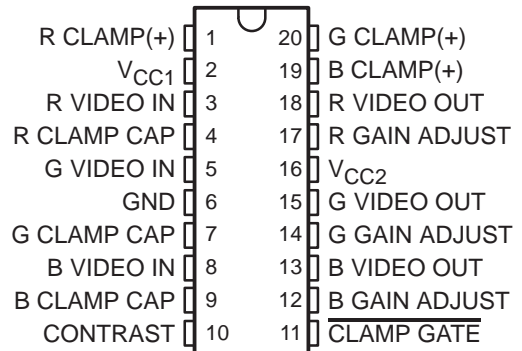


# TLS1233 VIDEO PREAMPLIFIER SYSTEM

SLVS126C – JULY 1995 – REVISED JUNE 1996

- Wide Bandwidth . . . Typ 100 MHz at –3 dB
- Three Channels
- 0 V to 4 V, Digital Level-Contrast Control
- 0 V to 4 V, Digital Level-Gain Adjust Control
- 20-Pin Plastic DIP for Small PCB Area Required
- Fewer Peripheral Components Required Than for LM1203 Applications
- Independent CLAMP(+) Adjustment to Each Channel

N PACKAGE  
(TOP VIEW)

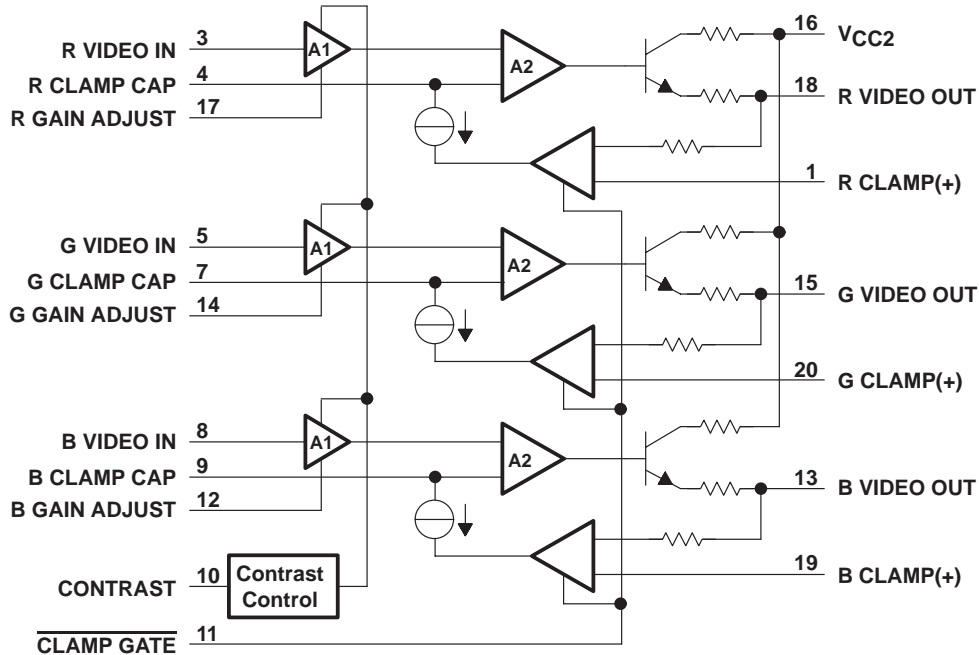


## description

The TLS1233 is a 100-MHz wide-band video preamplifier system intended for mid-to-high-resolution RGB (red-green-blue) color monitors. Each video amplifier (R, G, and B) contains a gain set for adjusting maximum system gain ( $A_V = 7.8$  V/V). The TLS1233 provides digital level-operated contrast, brightness, and gain adjustment control. All the control inputs offer high input impedance and an operation range from 0 V to 4 V for easy interface to the serial digital buses. Provided in a 20-pin plastic dual-in-line package (DIP), the TLS1233 integrates most of the external components required to accommodate the video system.

The TLS1233 operates from a 12-V supply and contains an internal input bias voltage. Also, the TLS1233 contains the feedback resistor required between output and CLAMP(–) for dc level holding. The device is characterized for operation from 0°C to 70°C.

## functional block diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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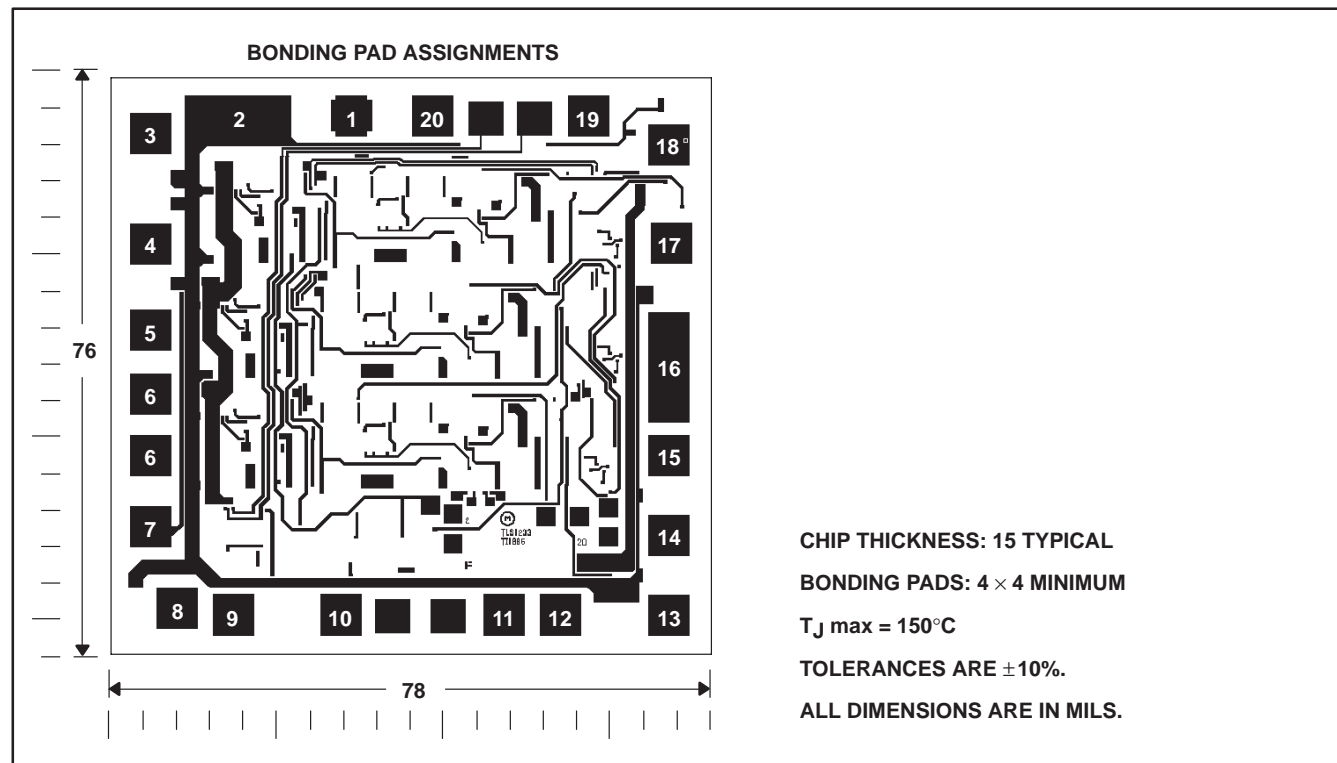
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# TLS1233 VIDEO PREAMPLIFIER SYSTEM

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## TLS1233Y chip information

This chip, when properly assembled, displays characteristics similar to the TLS1233. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC}$	13.5 V
Input voltage range, $V_I$ (see Note 1)	0 V to $V_{CC}$
Video output current, $I_O$ (per channel)	28 mA
Total power dissipation at (or below) 25°C free-air temperature (see Note 2)	1.87 W
Operating virtual junction temperature range, $T_J$	-55°C to 150°C
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All  $V_{CC}$  terminals must be externally wired together to prevent internal damage during  $V_{CC}$  power-on/-off cycles.  
 2. For operation above 25°C free-air temperature, derate linearly from 1.87 W ( $T_A = 25^\circ\text{C}$ ) to 1.2 W ( $T_A = 70^\circ\text{C}$ ). This equates to a derating factor of 15 mW/°C.

### recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC1</sub> and V <sub>CC2</sub>		11	12	13	V
High-level input voltage range, $\overline{\text{CLAMP GATE}}$ , V <sub>IH</sub>	Clamp comparators off	2.4		5	V
Low-level input voltage range, $\overline{\text{CLAMP GATE}}$ , V <sub>IL</sub>	Clamp comparators on	0		0.8	V
Operating free-air temperature, T <sub>A</sub>		0		70	°C

**electrical characteristics at 25°C free-air temperature range,  $\overline{\text{CLAMP GATE}} = 0$  V,  $\text{CLAMP}(+) = 2$  V,  $\text{CONTRAST} = \text{R,G,B GAIN ADJUST} = 4$  V,  $V_{CC1} = V_{CC2} = 12$  V (see Figure 2) (unless otherwise noted)**

PARAMETER	ALTERNATE SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC}$ Supply current		$V_{CC1} + V_{CC2}$		84	94	mA
$V_{ref}$ Video input reference voltage		Measure R/G/B video input	2.1	2.3	2.5	V
$I_I$ Contrast and R,G,B GAIN ADJUST input current		Measure CONTRAST, R/G/B GAIN ADJUST		-0.5	-10	μA
$I_{IL}$ Clamp gate low input current		$\overline{\text{CLAMP GATE}} = 0$ V		-0.5	-2.4	μA
$I_{IH}$ Clamp gate high input current		$\overline{\text{CLAMP GATE}} = 12$ V		0.005	1	μA
Clamp capacitor charge current	$I_{K(chg)}$	R,G,B CLAMP CAP = 0 V		1		mA
Clamp capacitor discharge current	$I_{K(dschg)}$	R,G,B CLAMP CAP = 5 V		-1		mA
$V_{OL}$ Low-level output voltage		R,G,B CLAMP CAP = 0 V		0.3		V
$V_{OH}$ High-level output voltage		R,G,B CLAMP CAP = 5 V		7.8		V
$V_{O(diff)}$ Output voltage difference	$V_{O(diff)}$	Between any two channels		±0.5	±50	mV

**operating characteristics at 25°C free-air temperature,  $\overline{\text{CLAMP GATE}} = 0$  V,  $\text{CLAMP}(+) = 4$  V,  $\text{CONTRAST} = \text{R,G,B GAIN ADJUST} = 4$  V,  $f_I = 10$  kHz,  $V_{CC1} = V_{CC2} = 12$  V (unless otherwise noted)**

PARAMETER	ALTERNATE SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$A_{V(max)}$ Maximum voltage amplification	$A_{VMAX}$	$\text{CONTRAST} = 4$ V, $V_{I(PP)} = 700$ mV		7.8		V/V
$A_{V(mid)}$ Midrange voltage amplification	$A_{VMID}$	$\text{CONTRAST} = 2$ V, $V_{I(PP)} = 700$ mV		2		V/V
Contrast voltage for minimum amplification	$V_{CONT-LOW}$	$V_{I(PP)} = 1$ V, See Note 3		1		V
Amplification match at $A_{V(max)}$	$A_{Vmax(diff)}$	$\text{CONTRAST} = 4$ V, See Note 4		±0.2		dB
Amplification match at $A_{V(mid)}$	$A_{Vmid(diff)}$	$\text{CONTRAST} = 2$ V, See Note 3		±0.2		dB
Amplification match at $A_{V(low)}$	$A_{Vlow(diff)}$	$\text{CONTRAST} = V_{CONT-LOW}$ , See Note 3 and 4		±0.2		dB
THD Total harmonic distortion		$\text{CONTRAST} = 1$ V, $V_{I(PP)} = 1$ V		0.5		%
BW Amplifier bandwidth	$BW(-3 \text{ dB})$	$\text{CONTRAST} = 4$ V, See Notes 5 And 7		100		MHz
Crosstalk attenuation	$a_x$	$\text{CONTRAST} = 4$ V, $f = 10$ kHz, See Note 6		60		dB
		$\text{CONTRAST} = 4$ V, See Notes 6 or 7 $f = 10$ MHz,		40		dB
Pulse test for rise time	$t_r$	$\text{CONTRAST} = 4$ V, $\text{CLAMP}(+) = 2$ V, $V_{O(PP)} = 4$ V		3		ns
Pulse test for fall time	$t_f$	See Notes 5 and 7		4		ns

- NOTES: 3. Determine  $V_{CONT-LOW}$  for -40 dB attenuation of output. Reference to  $A_{V(max)}$ .  
4. Measure gain difference between any two amplifiers,  $V_{I(PP)} = 1$  V.  
5. Adjust input frequency from 10 kHz ( $A_{V(max)}$  reference level) to the -3-dB corner frequency ( $f - 3$  dB).  $V_{I(PP)} = 700$  mV.  
6.  $V_{I(PP)} = 700$  mV at  $f = 10$  kHz to any amplifier. Measure output levels of the other two undriven amplifiers relative to driven amplifier.  
7. A special test fixture without a socket and a double-sided full-ground-plane PC board are required.

# TLS1233 VIDEO PREAMPLIFIER SYSTEM

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## PARAMETER MEASUREMENT INFORMATION

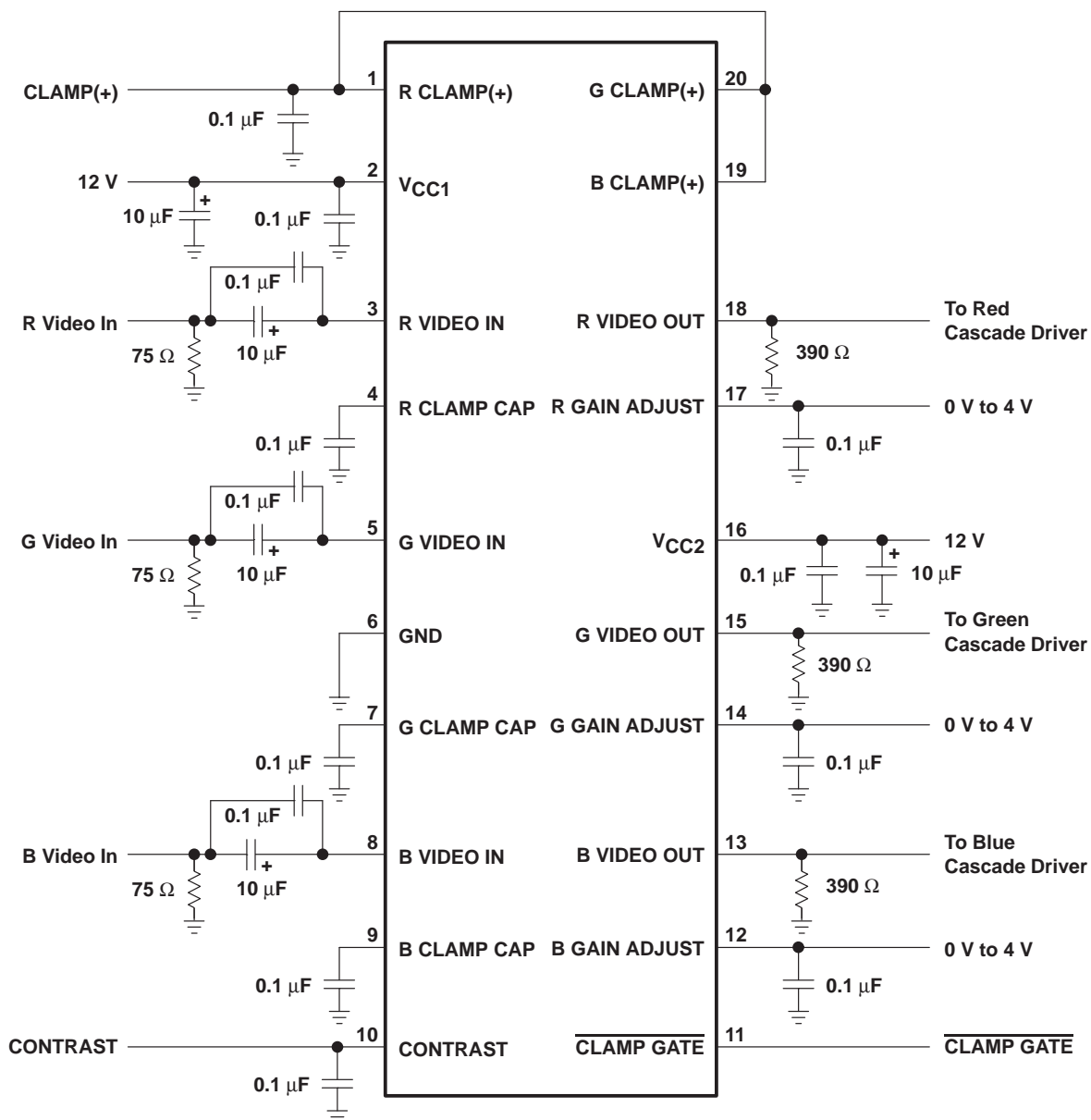


Figure 1. Test Circuit

# APPLICATION INFORMATION

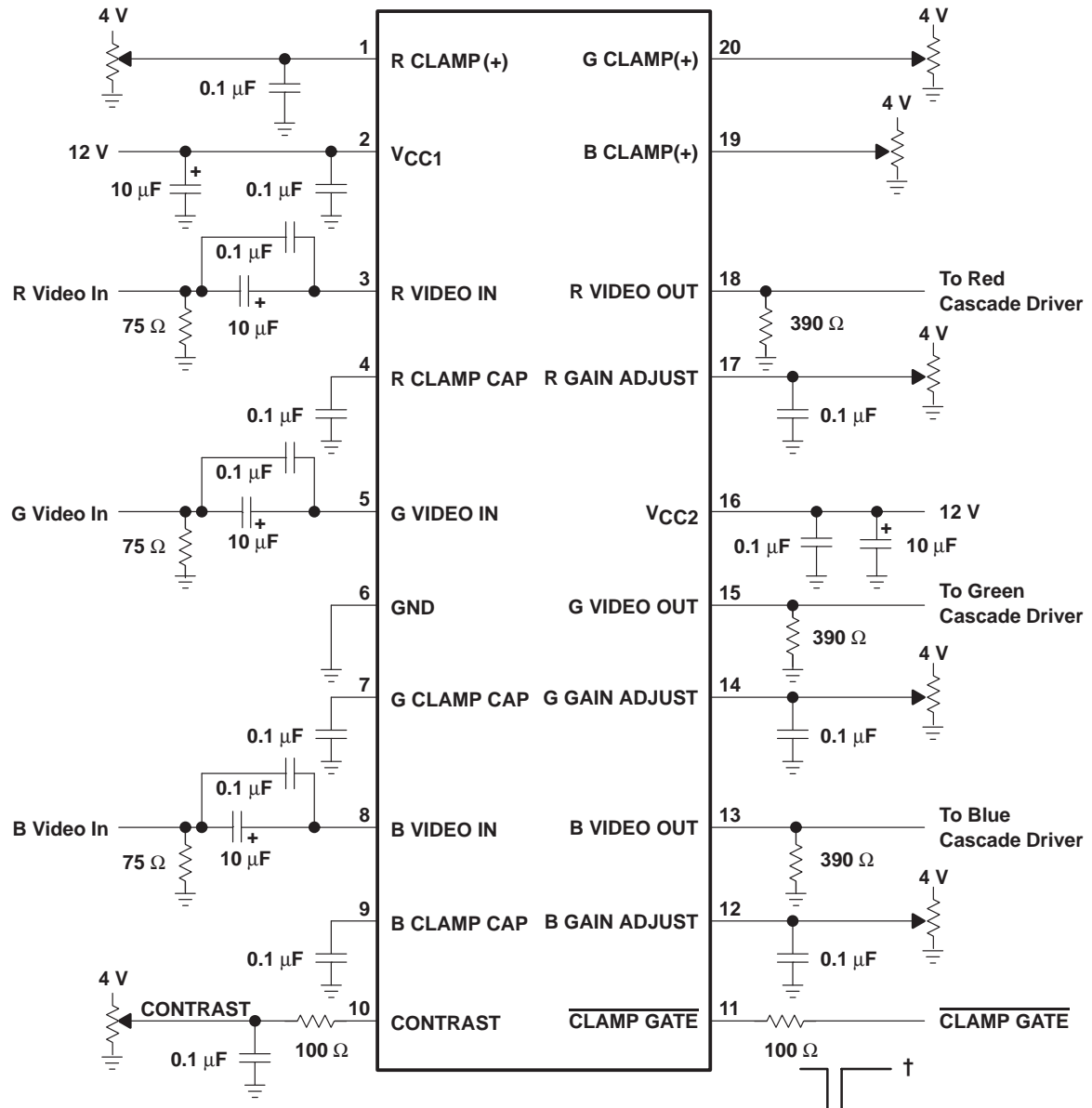


Figure 2. Application Circuit

# TLS1233 VIDEO PREAMPLIFIER SYSTEM

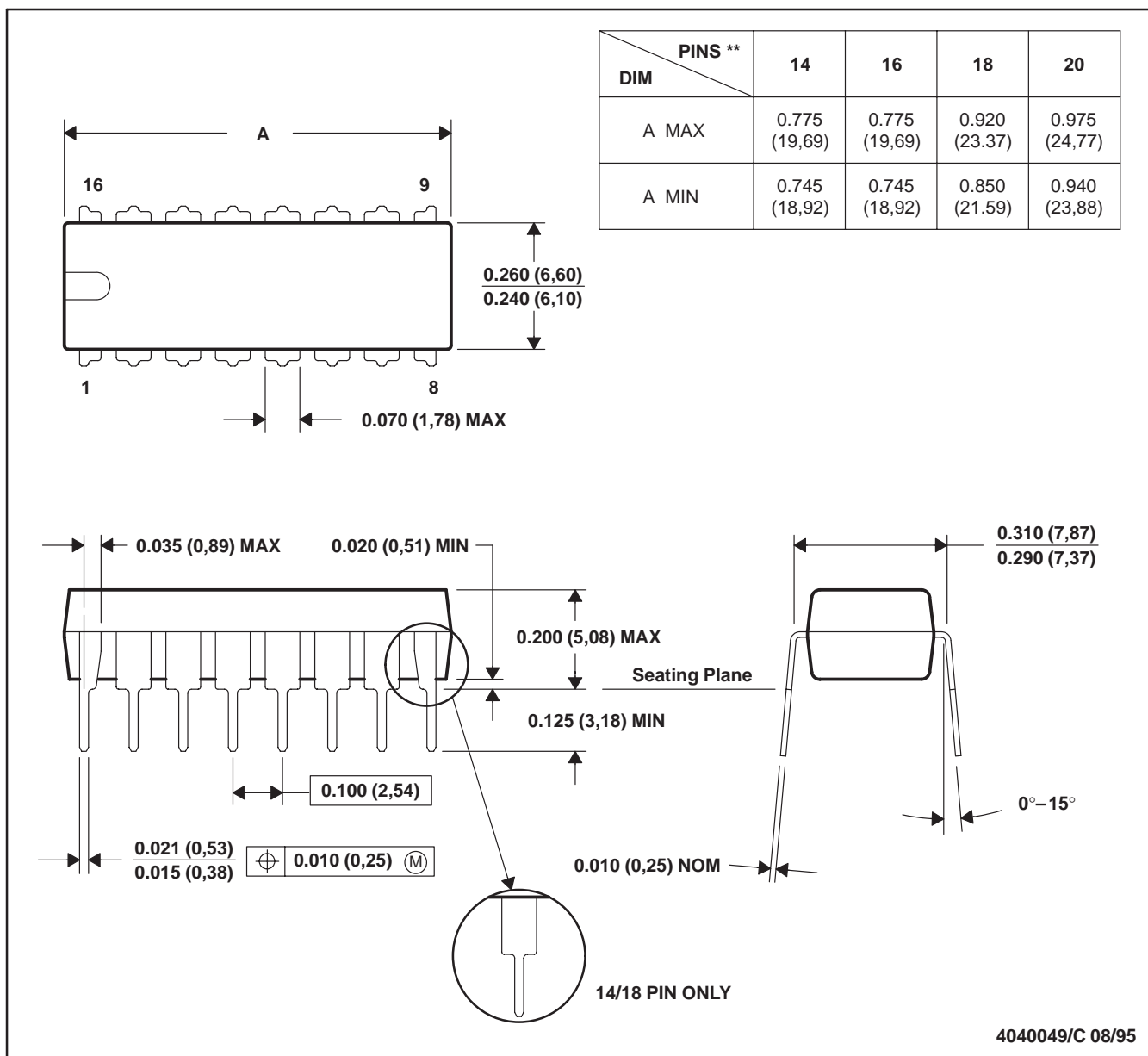
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## MECHANICAL DATA

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001 (20 pin package is shorter than MS-001.)

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TLS1233N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLS1233NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Mailing Address: Texas Instruments  
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