

General features

$V_{CS(ON)}$	I_C	$R_{CS(ON)}$
0.8 V	8 A	0.10 Ω

- High voltage / high current Cascode configuration
- Low equivalent on resistance
- very fast-switch up to 150 kHz
- Squared RBSOA up to 1200V
- Very low C_{iss} driven by $R_G = 47Ω$
- Very low turn-off cross over time

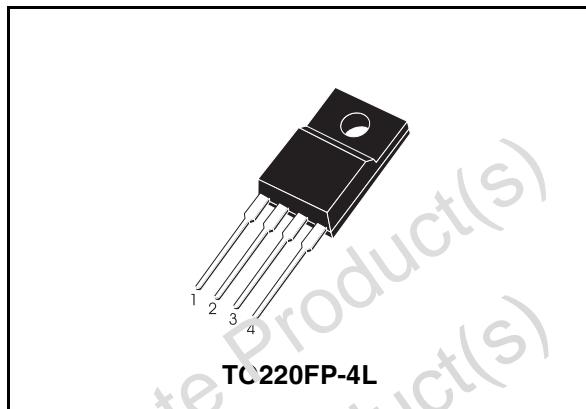
Applications

- Aux SMPS for three phase mains

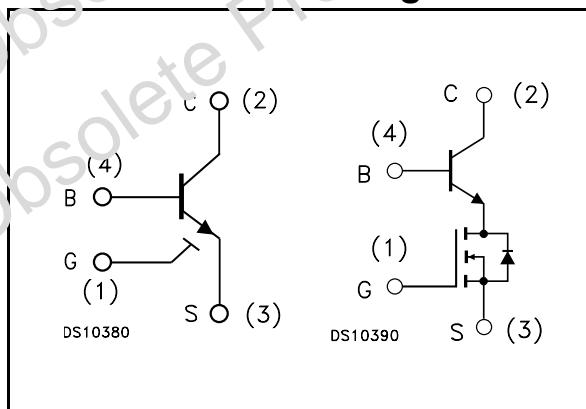
Description

The STP08IE120F4 is manufactured in Monolithic ESBT Technology, aimed to provide best performances in high frequency / high voltage applications.

It is designed for use in Gate Driven based topologies.



Internal schematic diagrams



Order codes

Part Number	Marking	Package	Packing
STP08IE120F4	P08IE120F4	TO220FP-4L	Tube

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1 Electrical ratings

Table 1. Absolute maximum rating

Symbol	Parameter	Value	Unit
$V_{CS(ss)}$	Collector-source voltage ($V_{BS} = V_{GS} = 0$ V)	1200	V
$V_{BS(OS)}$	Base-source voltage ($I_C = 0$, $V_{GS} = 0$ V)	30	V
$V_{SB(OS)}$	Source-base voltage ($I_C = 0$, $V_{GS} = 0$ V)	17	V
V_{GS}	Gate-source voltage	± 17	V
I_C	Collector current	8	A
I_{CM}	Collector peak current ($t_P < 5$ ms)	24	A
I_B	Base current	5	A
I_{BM}	Base peak current ($t_P < 5$ ms)	12	A
P_{tot}	Total dissipation at $T_c = 25$ °C	21	W
T_{stg}	Storage temperature	-40 to 150	°C
T_J	Max. operating junction temperature	150	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	6	°C/W

2 Electrical characteristics

($T_{case} = 25^\circ\text{C}$ unless otherwise specified)

Table 3. Electrical characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{CS(ss)}$	Collector-source current ($V_{BS} = V_{GS} = 0$)	$V_{CE} = 1200\text{V}$			100	μA
$I_{BS(OS)}$	Base-source current ($I_C = 0, V_{GS} = 0$)	$V_{BS(OS)} = 30\text{V}$			10	μA
$I_{SB(OS)}$	Source-base current ($I_C = 0, V_{GS} = 0$)	$V_{SB(OS)} = 17\text{V}$			100	μA
$I_{GS(OS)}$	Gate-source leakage	$V_{GS} = \pm 17\text{V}$			100	nA
$V_{CS(ON)}$	Collector-source ON voltage	$V_{GS} = 10\text{V} \quad I_C = 8\text{A} \quad I_B = 1.6\text{A}$ $V_{GS} = 10\text{V} \quad I_C = 4\text{A} \quad I_B = 0.4\text{A}$		0.8 0.5	1 1.2	V
h_{FE}	DC current gain	$V_{GS} = 10\text{V} \quad I_C = 8\text{A} \quad V_{CS} = 1\text{V}$ $V_{GS} = 10\text{V} \quad I_C = 4\text{A} \quad V_{CS} = 1\text{V}$	5 7			
$V_{BS(ON)}$	Base Source ON voltage	$V_{BS} = 0\text{V} \quad I_C = 8\text{A} \quad I_B = 1.6\text{A}$ $V_{BS} = 10\text{V} \quad I_C = 4\text{A} \quad I_B = 0.4\text{A}$		1.5 1.5		V
$V_{GS(th)}$	Gate threshold voltage	$V_{BS} = V_{GS} \quad I_B = 250\mu\text{A}$	2	3	4	V
C_{ISS}	Input capacitance	$V_{CS} = 25\text{V} \quad f = 1\text{MHz}$ $V_{GS} = 0$		550		pF
$Q_{GS(tot)}$	Gate source charge	$V_{GS} = 10\text{V}$		26		nC
t_s t_f	INDUCTIVE LOAD Storage time Fall time	$I_C = 4\text{A} \quad I_B = 0.8\text{A} \quad V_{GS} = 10\text{V}$ $V_{Clamp} = 960\text{V} \quad R_G = 47\Omega$ $t_p = 4\mu\text{s}$		670 15		ns ns
t_s t_f	INDUCTIVE LOAD Storage time Fall time	$I_C = 4\text{A} \quad I_B = 0.4\text{A} \quad V_{GS} = 10\text{V}$ $V_{Clamp} = 960\text{V} \quad R_G = 47\Omega$ $t_p = 4\mu\text{s}$		340 10.2		ns ns
V_{CSW}	Maximum collector-source voltage switched without snubber	$R_G = 47\Omega \quad h_{FE} = 5\text{A} \quad I_C = 8\text{A}$	1200			V
$V_{CS(dyn)}$	Collector-source dynamic voltage (500ns)	$V_{CC} = V_{Clamp} = 400\text{V} \quad V_{GS} = 10\text{V}$ $R_G = 47\Omega \quad I_C = 4\text{A} \quad I_B = 0.8\text{A}$ $I_{Bpeak} = 4\text{A} \quad t_{peak} = 500\text{ns}$		5.75		V
$V_{CS(dyn)}$	Collector-source dynamic voltage (1 μs)	$V_{CC} = V_{Clamp} = 400\text{V} \quad V_{GS} = 10\text{V}$ $R_G = 47\Omega \quad I_C = 4\text{A} \quad I_B = 0.8\text{A}$ $I_{Bpeak} = 4\text{A} \quad t_{peak} = 500\text{ns}$		3.35		V

2.1 Electrical characteristics (curves)

Figure 1. Output characteristics

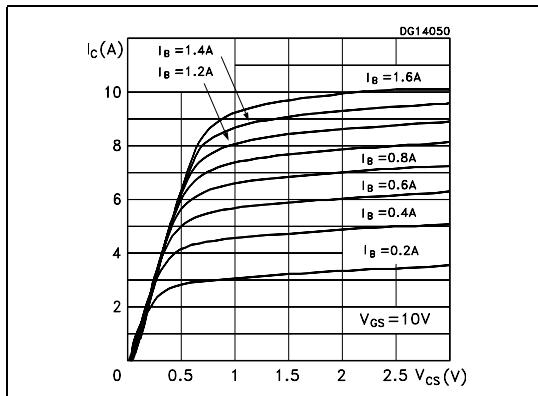


Figure 2. DC current gain

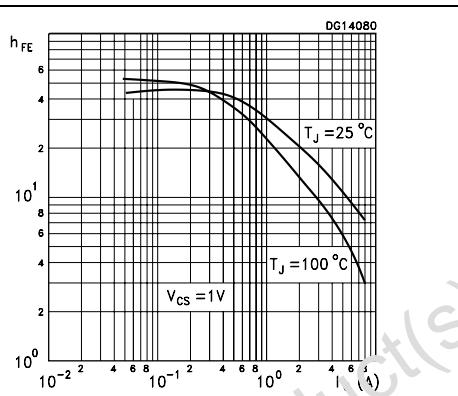


Figure 3. Collector-source On voltage

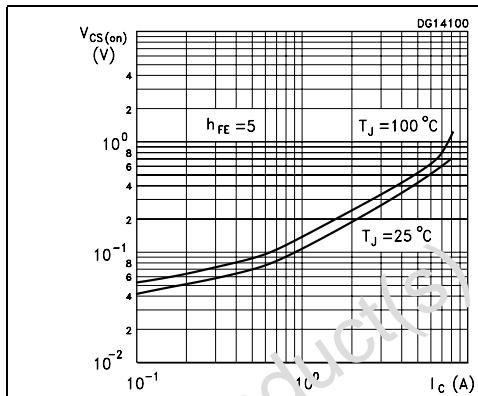


Figure 4. Collector-source On voltage

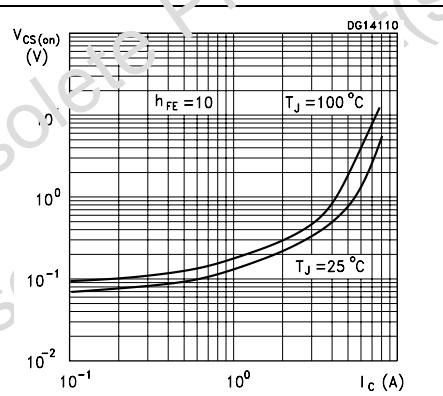


Figure 5. Base-source On voltage

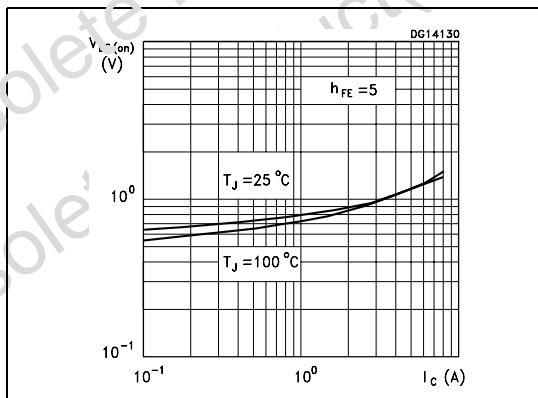


Figure 6. Base-source On voltage

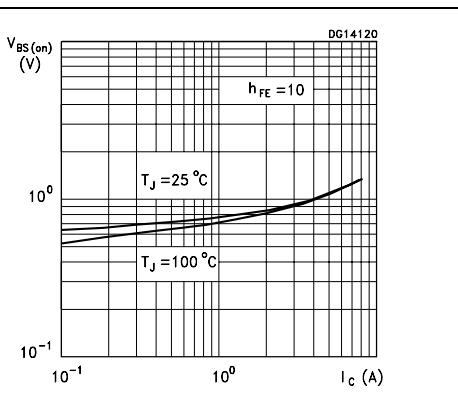


Figure 7. Reverse biased safe operating area

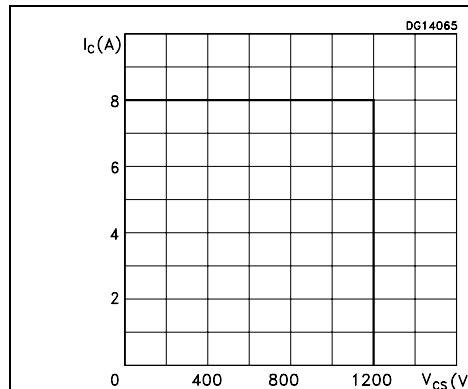


Figure 9. Dynamic collector-emitter saturation voltage

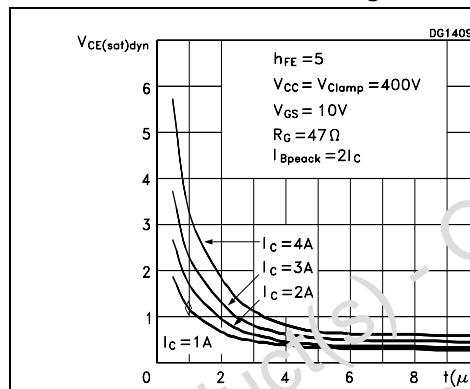


Figure 11. Inductive load switching time

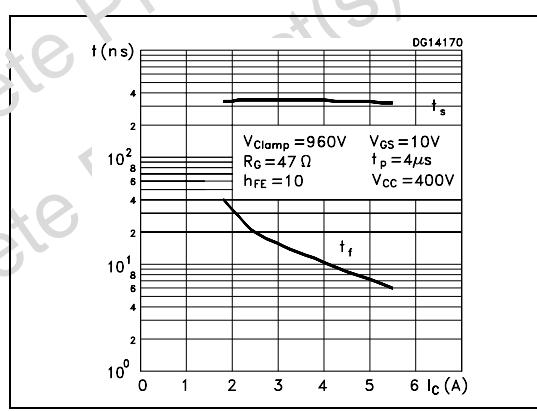


Figure 8. Gate threshold voltage vs temperature

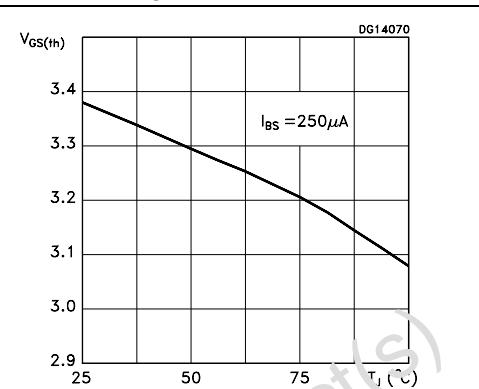
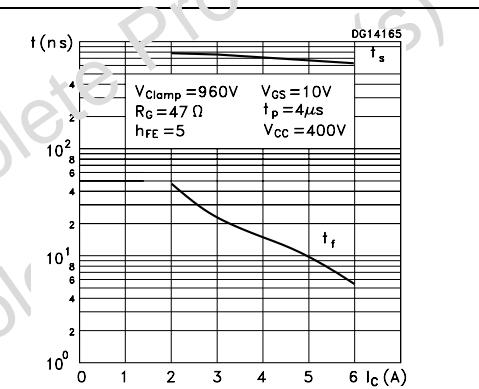
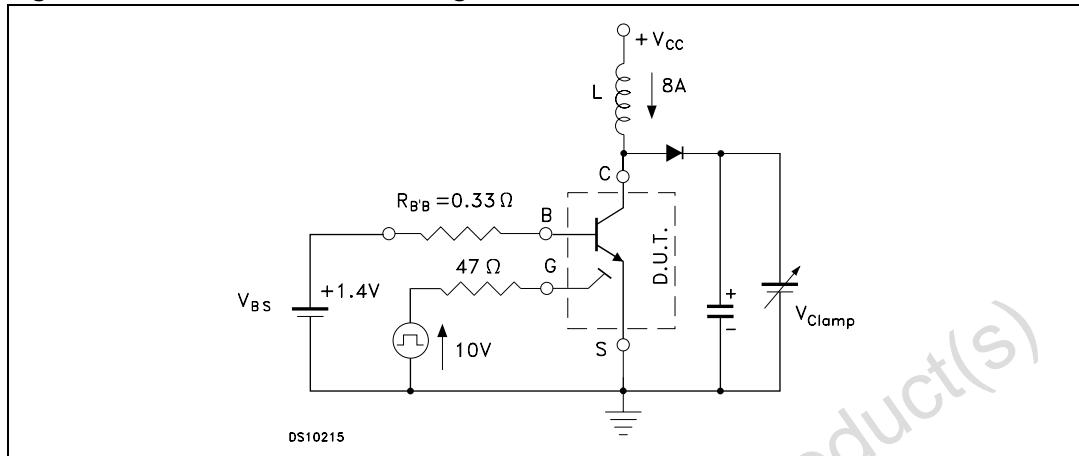


Figure 10. Inductive load switching time



2.2 Test circuits

Figure 12. Inductive load switching and RBSOA test circuit

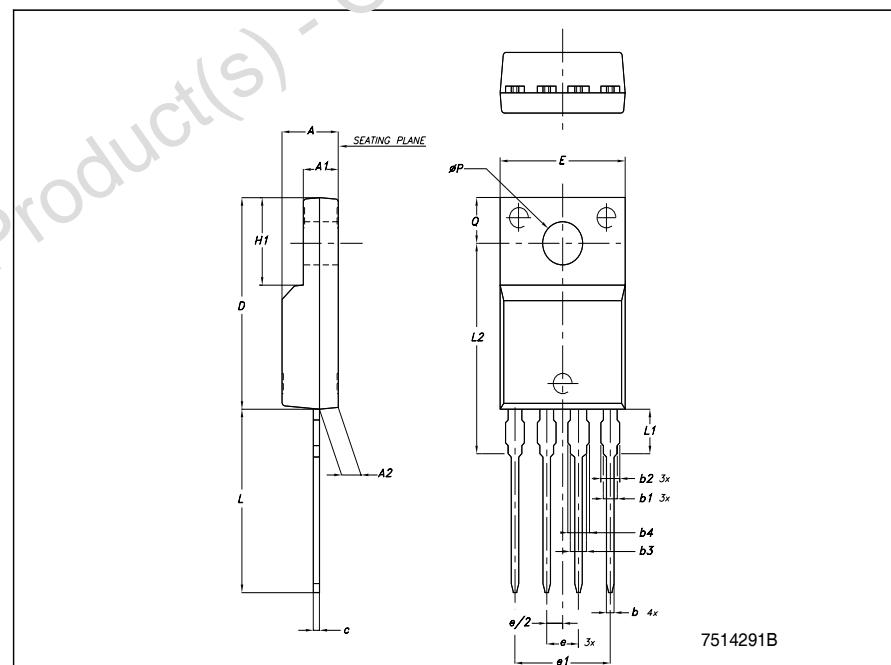


3 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO220FP-4L MECHANICAL DATA

DIM.	MIN.	mm. TYP.	MAX.
A	4.30		4.70
A1	2.60		3
A2	1.30	1.50	1.70
b	0.50		0.70
b1	1.05		
b2			1.3
b3	1.25		
b4			0.50
c	0.45	0.50	0.60
D	15.50		15.90
E	9.80		10.20
e	2.29	2.54	2.79
e1		7.62	
H1	6.30		6.70
L		10.60	
L1		9.30	
L2	15.40		15.80
Dia P	3		3.40
Q	3.30		3.50



4 Revision history

Table 4. Revision history

Date	Revision	Changes
28-Nov-2006	1	Initial release.

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