DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

Check for Samples: SN54LV123A, SN74LV123A

FEATURES

- **2-V to 5.5-V V_{CC} Operation**
- **Max t_{pd} of 11 ns at 5 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **Schmitt-Trigger Circuitry on $\overline{A}$, B, and $\overline{CLR}$ Inputs for Slow Input Transition Rates**
- **Edge Triggered From Active-High or Active-Low Gated Logic Inputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Retriggerable for Very Long Output Pulses, up to 100% Duty Cycle**
- **Overriding Clear Terminates Output Pulse**
- **Glitch-Free Power-Up Reset on Outputs**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class 11**

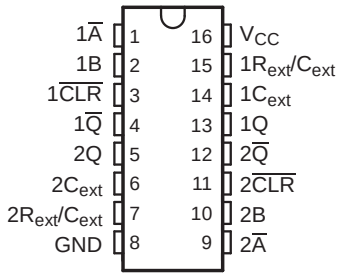
DESCRIPTION

The 'LV123A devices are dual retriggerable monostable multivibrators designed for 2-V to 5.5-V V_{CC} operation.

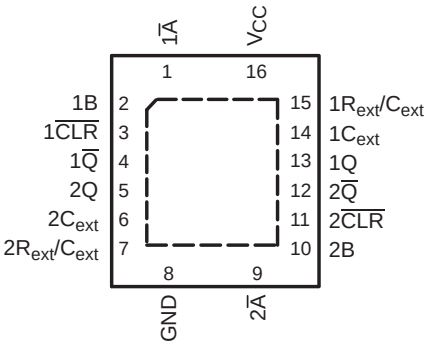
These edge-triggered multivibrators feature output pulse-duration control by three methods. In the first method, the $\overline{A}$ input is low, and the B input goes high. In the second method, the B input is high, and the $\overline{A}$ input goes low. In the third method, the $\overline{A}$ input is low, the B input is high, and the clear ($\overline{CLR}$) input goes high.

The output pulse duration is programmable by selecting external resistance and capacitance values. The external timing capacitor must be connected between C_{ext} and R_{ext}/C_{ext} (positive) and an external resistor connected between R_{ext}/C_{ext} and V_{CC}. To obtain variable pulse durations, connect an external variable resistance between R_{ext}/C_{ext} and V_{CC}. The output pulse duration also can be reduced by taking $\overline{CLR}$ low.

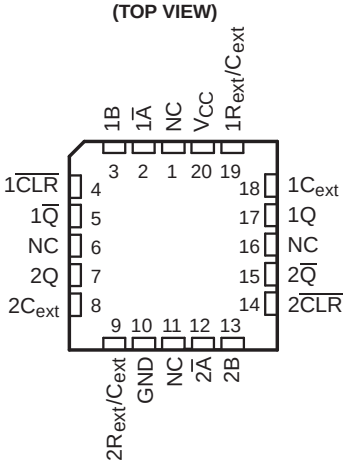
SN54LV123A . . . J OR W PACKAGE
SN74LV123A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN74LV123A . . . RGY PACKAGE
(TOP VIEW)



SN54LV123A . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. The $\overline{A}$, B, and $\overline{CLR}$ inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

Once triggered, the basic pulse duration can be extended by retriggering the gated low-level-active ($\overline{A}$) or high-level-active (B) input. Pulse duration can be reduced by taking $\overline{CLR}$ low. The input/output timing diagram illustrates pulse control by retriggering the inputs and early clearing.

During power up, Q outputs are in the low state, and $\overline{Q}$ outputs are in the high state. The outputs are glitch free, without applying a reset pulse.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Pin assignments for these devices are identical to those of the 'AHC123A and 'AHCT123A devices for interchangeability, when allowed.

Table 1. FUNCTION TABLE (EACH MULTIVIBRATOR)

INPUTS			OUTPUTS	
$\overline{CLR}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L(1)	H(1)
X	X	L	L(1)	H(1)
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

(1) These outputs are based on the assumption that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the setup.

Figure 1. LOGIC DIAGRAM, EACH MULTIVIBRATOR (POSITIVE LOGIC)

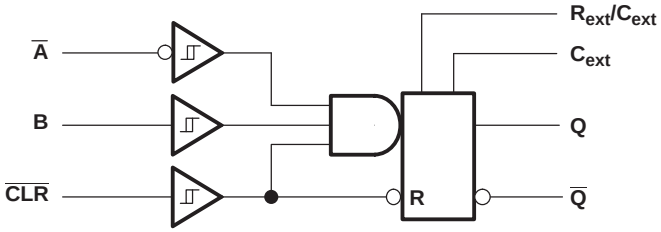
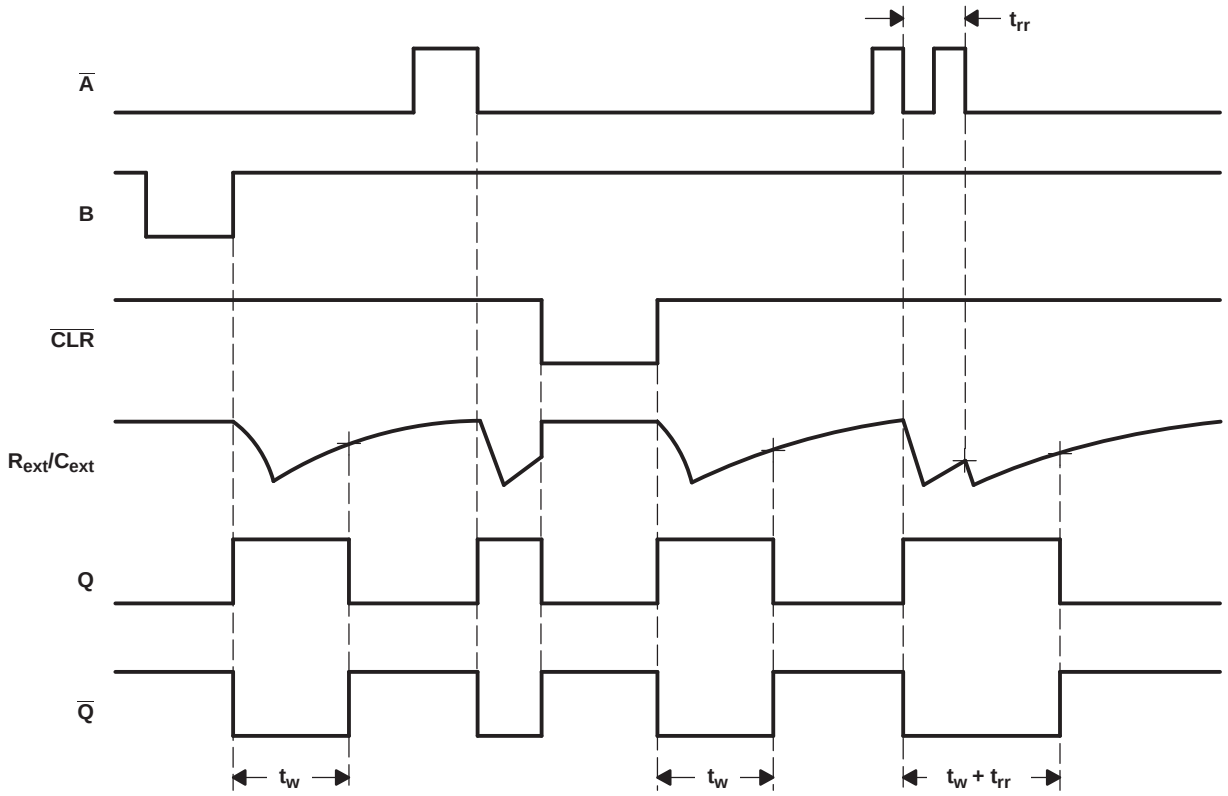


Figure 2. INPUT/OUTPUT TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
V_O	Output voltage range in the high or low state(2) (3)		–0.5	V_{CC} + 0.5	V
V_O	Output voltage range in power-off state(2)		–0.5	7	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance	D package		73	°C/W
		DB package		82	
		DBV package		120	
		NS package		64	
		PW package		108	
		RGY package		39	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value is limited to 5.5 V maximum.

RECOMMENDED OPERATING CONDITIONS(1)

			SN54LV123A(2)		SN74LV123A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 2.3 V to 2.7 V		–2		–2	mA
		V_{CC} = 3 V to 3.6 V		–6		–6	
		V_{CC} = 4.5 V to 5.5 V		–12		–12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		6		6	
		V_{CC} = 4.5 V to 5.5 V		12		12	
R_{ext}	External timing resistance	V_{CC} = 2 V	5		5		kΩ
		V_{CC} ≥ 3 V	1		1		
C_{ext}	External timing capacitance		No restriction		No restriction		pF
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		1		1		ms/V
T_A	Operating free-air temperature		–40	125	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) Product Preview

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	–55°C to 125°C SN54LV123A (1)			–40°C to 85°C SN74LV123A			Recommended –40°C to 125°C SN74LV123A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}		I_{OH} = –50 µA	2 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1			V_{CC} – 0.1			V
		I_{OH} = –2 mA	2.3 V	2			2			2			
		I_{OH} = –6 mA	3 V	2.48			2.48			2.48			
		I_{OH} = –12 mA	4.5 V	3.8			3.8			3.8			
V_{OL}		I_{OL} = 50 µA	2 V to 5.5 V			0.1			0.1			0.1	V
		I_{OL} = 2 mA	2.3 V			0.4			0.4			0.4	
		I_{OL} = 6 mA	3 V			0.44			0.44			0.44	
		I_{OL} = 12 mA	4.5 V			0.55			0.55			0.55	
I_I	R_{ext}/C_{ext} (2)	V_I = 5.5 V or GND	5.5 V			±2.5			±2.5			±25	µA
I_I	$\overline{A}$, B, and $\overline{CLR}$	V_I = 5.5 V or GND	0 V			±1			±1			±1	µA
			0 to 5.5 V			±1			±1			±1	
I_{CC}	Quiescent	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			20			20			20	µA
I_{CC}	Active state (per circuit)	$V_I = V_{CC}$ or GND, R_{ext}/C_{ext} = 0.5 V_{CC}	3 V			280			280			280	µA
			4.5 V			650			650			650	
			5.5 V			975			975			975	
I_{off}		V_I or V_O = 0 to 5.5 V	0 V						5			5	µA
C_i		$V_I = V_{CC}$ or GND	3.3 V		1.9			1.9			1.9		pF
			5 V		1.9			1.9			1.9		

(1) Product Preview
(2) This test is performed with the terminal in the off-state condition.

TIMING REQUIREMENTS

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 3)

PARAMETER			TEST CONDITIONS		T_A = 25°C		–55°C to 125°C SN54LV123A (1)		–40°C to 85°C SN74LV123A		–40°C to 125°C SN74LV123A		UNIT
					MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$			6		6.5		6.5		6.5		ns
		$\overline{A}$ or B trigger			6		6.5		6.5		6.5		
t_{rr}	Pulse retrigger time		R_{ext} = 1 kΩ	C_{ext} = 100 pF	See (2)	94	See (2)		See (2)		See (2)		ns
				C_{ext} = 0.01 µF	See (2)	2	See (2)		See (2)		See (2)		µs

(1) Product Preview
(2) See etriggering data in the Application Information section

TIMING REQUIREMENTS

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 3)

PARAMETER			TEST CONDITIONS		T_A = 25°C		–55°C to 125°C SN54LV123A (1)		–40°C to 85°C SN74LV123A		–40°C to 125°C SN74LV123A		UNIT
					MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$			5		5		5		5		ns
		$\overline{A}$ or B trigger			5		5		5		5		
t_{rr}	Pulse retrigger time		R_{ext} = 1 kΩ	C_{ext} = 100 pF	See (2)	76	See (2)		See (2)		See (2)		ns
				C_{ext} = 0.01 µF	See (2)	1.8	See (2)		See (2)		See (2)		µs

(1) Product Preview
(2) See retriggering data in the Application Information section

TIMING REQUIREMENTS

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 3)

PARAMETER			TEST CONDITIONS		T_A = 25°C		–55°C to 125°C SN54LV123A (1)		–40°C to 85°C SN74LV123A		–40°C to 125°C SN74LV123A		UNIT
					MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$			5		5		5		5		ns
		$\overline{A}$ or B trigger			5		5		5		5		
t_{rr}	Pulse retrigger time		R_{ext} = 1 kΩ	C_{ext} = 100 pF	See (2)	59	See (2)		See (2)		See (2)		ns
				C_{ext} = 0.01 µF	See (2)	1.5	See (2)		See (2)		See (2)		µs

(1) Product Preview
(2) See retriggering data in the Application Information section

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			–55°C to 125°C SN54LV123A(1)		–40°C to 85°C SN74LV123A		–40°C to 125°C SN74LV123A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	$\overline{A}$ or B	Q or $\overline{Q}$	C_L = 15 pF		14.5	31.4(2)	1(2)	37(2)	1	37	1	37	ns
	$\overline{CLR}$	Q or $\overline{Q}$			13	25(2)	1(2)	29.5(2)	1	29.5	1	29.5	
	$\overline{CLR}$ trigger	Q or $\overline{Q}$			15.1	33.4(2)	1(2)	39(2)	1	39	1	39	
t_{pd}	$\overline{A}$ or B	Q or $\overline{Q}$	C_L = 50 pF		16.6	36	1	42	1	42	1	42	ns
	$\overline{CLR}$	Q or $\overline{Q}$			14.7	32.8	1	34.5	1	34.5	1	34.5	
	$\overline{CLR}$ trigger	Q or $\overline{Q}$			17.4	38	1	44	1	44	1	44	
t_w (3)		Q or $\overline{Q}$	C_L = 50 pF, C_{ext} = 28 pF, R_{ext} = 2 kΩ		197	260		320		320		320	ns
			C_L = 50 pF, C_{ext} = 0.01 µF, R_{ext} = 10 kΩ	90	100	110	90	110	90	110	90	110	µs
			C_L = 50 pF, C_{ext} = 0.1 µF, R_{ext} = 10 kΩ	0.9	1	1.1	0.9	1.1	0.9	1.1	0.9	1.1	ms
Δt_w (4)			C_L = 50 pF		±1								%

(1) Product Preview
(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(3) t_w = Duration of pulse at Q and $\overline{Q}$ outputs
(4) Δt_w = Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			–55°C to 125°C SN54LV123A(1)		–40°C to 85°C SN74LV123A		–40°C to 125°C SN74LV123A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	$\overline{A}$ or B	Q or $\overline{Q}$	C_L = 15 pF		10.2	20.6(2)	1(2)	24(2)	1	24	1	24	ns
	$\overline{CLR}$	Q or $\overline{Q}$			9.3	15.8(2)	1(2)	18.5(2)	1	18.5	1	18.5	
	$\overline{CLR}$ trigger	Q or $\overline{Q}$			10.6	22.4(2)	1(2)	26(2)	1	26	1	26	
t_{pd}	$\overline{A}$ or B	Q or $\overline{Q}$	C_L = 50 pF		11.8	24.1	1	27.5	1	27.5	1	27.5	ns
	$\overline{CLR}$	Q or $\overline{Q}$			10.5	19.3	1	22	1	22	1	22	
	$\overline{CLR}$ trigger	Q or $\overline{Q}$			12.3	25.9	1	29.5	1	29.5	1	29.5	
t_w (3)		Q or $\overline{Q}$	C_L = 50 pF, C_{ext} = 28 pF, R_{ext} = 2 kΩ		182	240		300		300		300	ns
			C_L = 50 pF, C_{ext} = 0.01 µF, R_{ext} = 10 kΩ	90	100	110	90	110	90	110	90	110	µs
			C_L = 50 pF, C_{ext} = 0.1 µF, R_{ext} = 10 kΩ	0.9	1	1.1	0.9	1.1	0.9	1.1	0.9	1.1	ms
Δt_w (4)			C_L = 50 pF		±1								%

(1) Product Preview
(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(3) t_w = Duration of pulse at Q and $\overline{Q}$ outputs
(4) Δt_w = Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			–55°C to 125°C SN54LV123A(1)		–40°C to 85°C SN74LV123A		–40°C to 125°C SN74LV123A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	$\overline{A}$ or B	Q or $\overline{Q}$	C_L = 15 pF		7.1	12(2)	1(2)	14(2)	1	14	1	14	ns
	$\overline{CLR}$	Q or $\overline{Q}$			6.5	9.4(2)	1(2)	11(2)	1	11	1	11	
	$\overline{CLR}$ trigger	Q or $\overline{Q}$			7.4	12.9(2)	1(2)	15(2)	1	15	1	15	
t_{pd}	$\overline{A}$ or B	Q or $\overline{Q}$	C_L = 50 pF		8.3	14	1	16	1	16	1	16	ns
	$\overline{CLR}$	Q or $\overline{Q}$			7.4	11.4	1	13	1	13	1	13	
	$\overline{CLR}$ trigger	Q or $\overline{Q}$			8.7	14.9	1	17	1	17	1	17	
t_w (3)		Q or $\overline{Q}$	C_L = 50 pF, C_{ext} = 28 pF, R_{ext} = 2 kΩ		167	200		240		240		240	ns
			C_L = 50 pF, C_{ext} = 0.01 µF, R_{ext} = 10 kΩ	90	100	110	90	110	90	110	90	110	µs
			C_L = 50 pF, C_{ext} = 0.1 µF, R_{ext} = 10 kΩ	0.9	1	1.1	0.9	1.1	0.9	1.1	0.9	1.1	ms
Δt_w (4)			C_L = 50 pF		±1								%

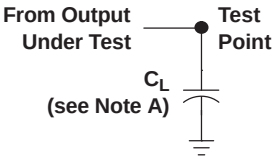
(1) Product Preview
(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(3) t_w = Duration of pulse at Q and $\overline{Q}$ outputs
(4) Δt_w = Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package

OPERATING CHARACTERISTICS

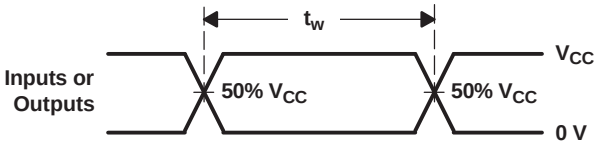
T_A = 25°C

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 10 MHz	3.3 V	44	pF
				5 V	49	

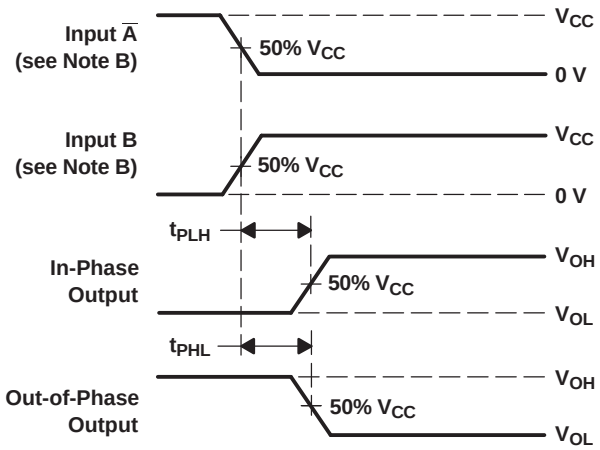
PARAMETER MEASUREMENT INFORMATION



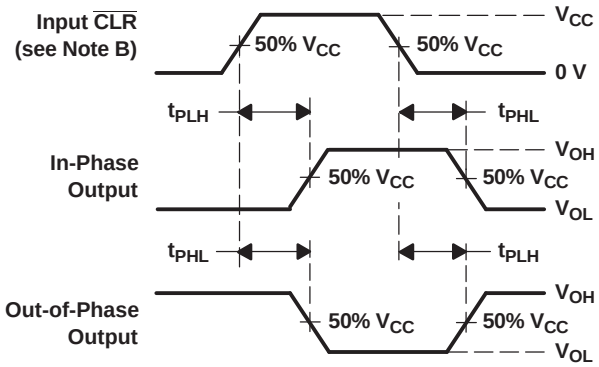
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time, with one input transition per measurement.

Figure 3. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

Operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied.

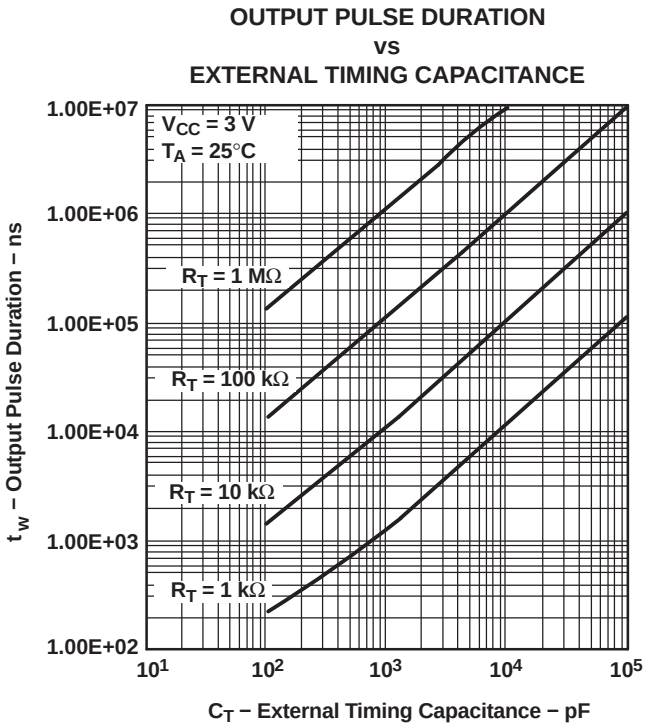


Figure 4.

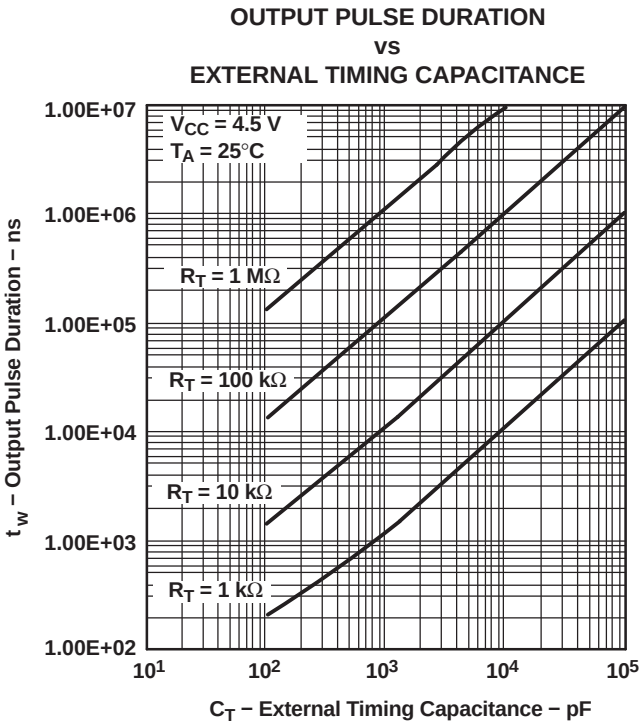


Figure 5.

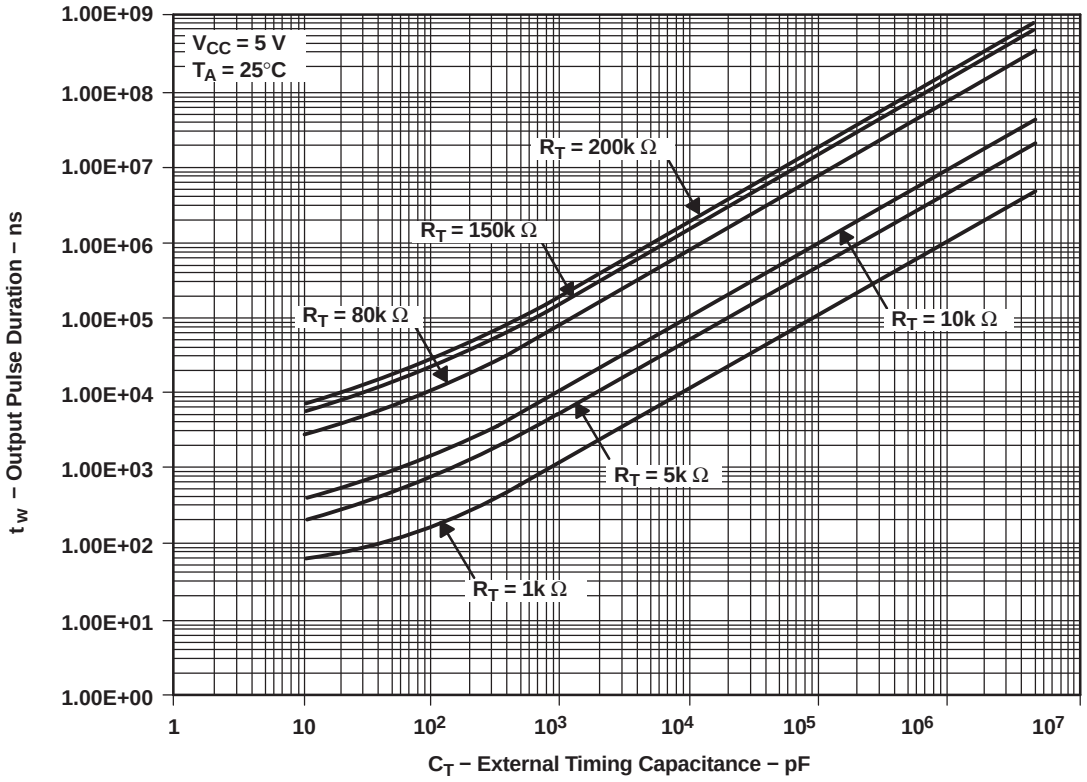


Figure 6. Output Pulse Duration vs External Timing Capacitance

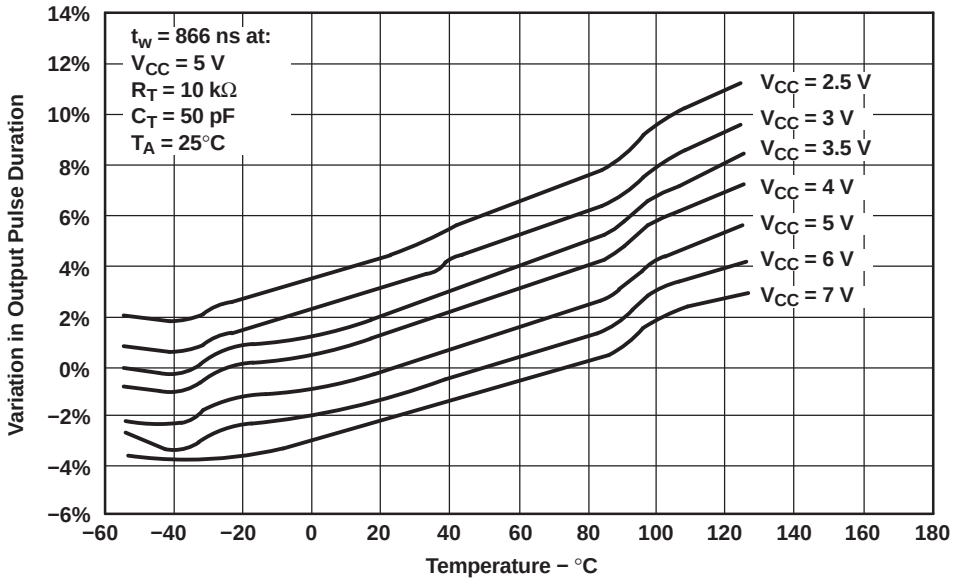


Figure 7. Variations in Output Pulse Duration vs Temperature

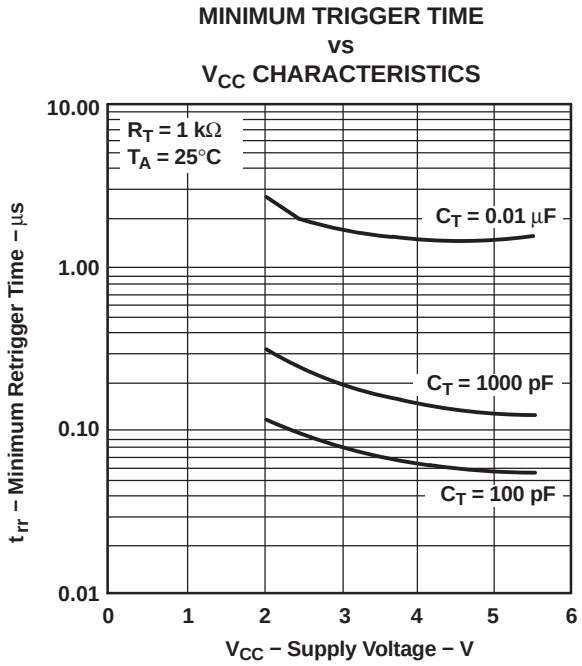


Figure 8.

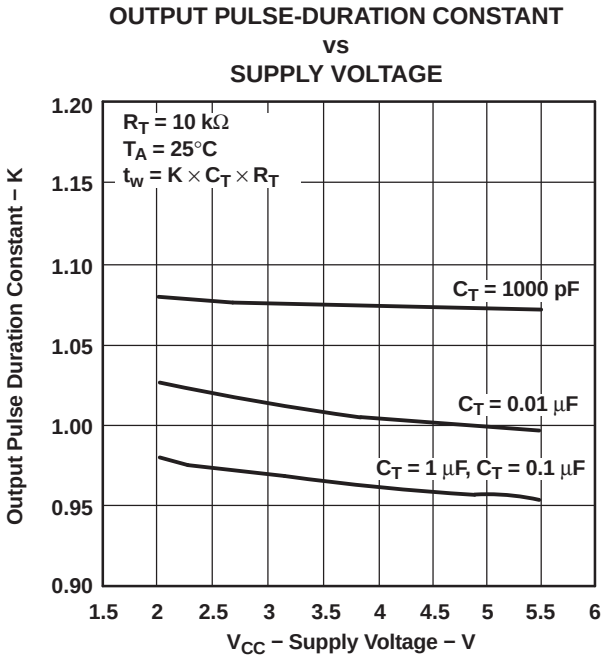


Figure 9.

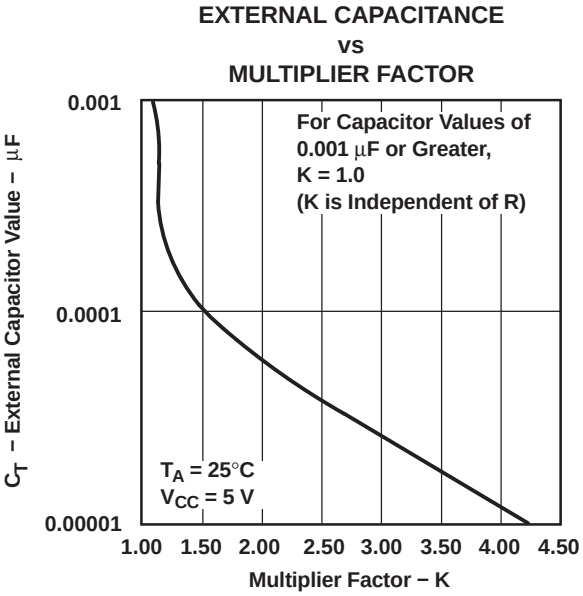


Figure 10.

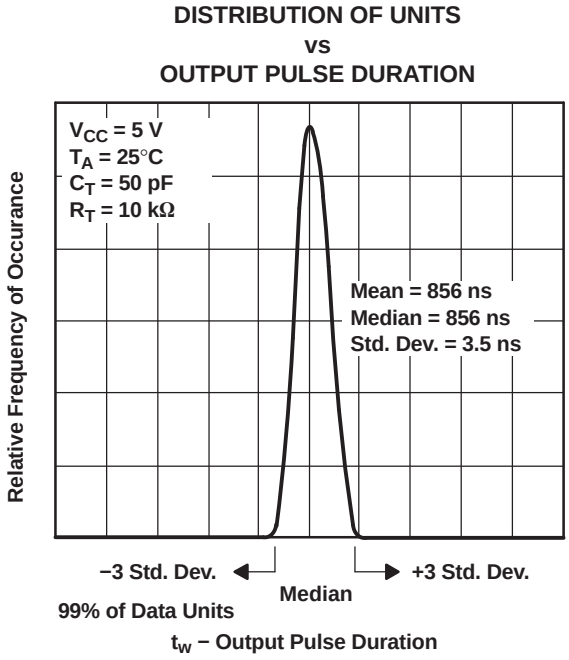


Figure 11.

Caution In Use

To prevent malfunctions due to noise, connect a high-frequency capacitor between V_{CC} and GND, and keep the wiring between the external components and Cext and Rext/Cext terminals as short as possible.

Power-Down Considerations

Large values of Cext can cause problems when powering down the 'LV123A devices because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor can discharge from V_{CC} through the protection diodes at pin 2 or pin 14. Current through the input protection diodes must be limited to 30 mA; therefore, the turn-off time of the V_{CC} power supply must not be faster than t = V_{CC} y Cext/30 mA. For example, if V_{CC} = 5 V and Cext = 15 pF, the V_{CC} supply must turn off no faster than t = (5 V) y (15 pF)/30 mA = 2.5 ns. Usually, this is not a problem because power supplies are heavily filtered and cannot discharge at this rate. When a more rapid decrease of V_{CC} to zero occurs, the 'LV123A devices can sustain damage. To avoid this possibility, use external clamping diodes.

Output Pulse Duration

The output pulse duration, t_w, is determined primarily by the values of the external capacitance (C_T) and timing resistance (R_T). The timing components are connected as shown in Figure 12.

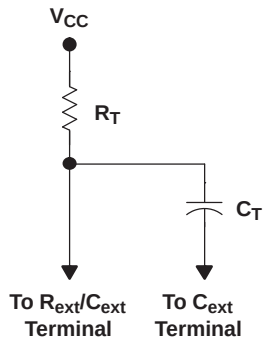


Figure 12. Timing-Component Connections

The pulse duration is given by:

$$t_w = K \times R_T \times C_T \quad (1)$$

if C_T is .1000 pF, K = 1.0 or

if C_T is <1000 pF, K can be determined from Figure 10

where:

t_w = pulse duration in ns

R_T = external timing resistance in kΩ

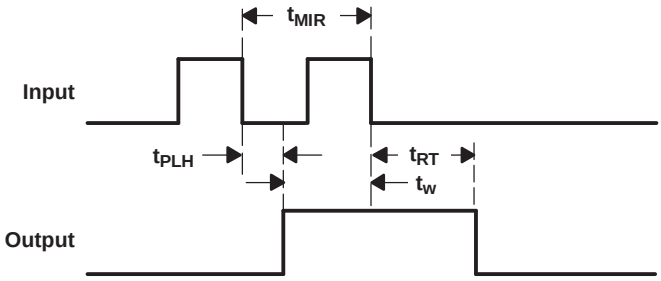
C_T = external capacitance in pF

K = multiplier factor

Equation 1 and Figure 5 can be used to determine values for pulse duration, external resistance, and external capacitance.

Retriggering Data

The minimum input retriggering time (t_{MIR}) is the minimum time required after the initial signal before retriggering the input. After t_{MIR}, the device retriggers the output. Experimentally, it also can be shown that to retrigger the output pulse, the two adjacent input signals should be t_{MIR} apart, where t_{MIR} = 0.30 × t_w. The retrigger pulse duration is calculated as shown in Figure 13.



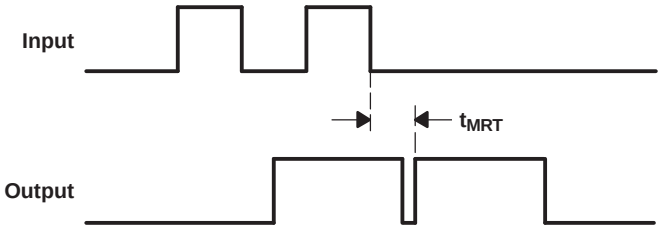
$t_{RT} = t_w + t_{PLH} = (K \times R_T \times C_T) + t_{PLH}$

Where:

t_{MIR} = Minimum Input Retriggering Time
t_{PLH} = Propagation Delay
t_{RT} = Retrigger Time
t_w = Output Pulse Duration Before Retriggering

Figure 13. Retrigger Pulse Duration

The minimum value from the end of the input pulse to the beginning of the retriggered output should be approximately 15 ns to ensure a retriggered output (see Figure 14).



t_{MRT} = Minimum Time Between the End of the Second Input Pulse and the Beginning of the Retriggered Output
t_{MRT} = 15 ns

Figure 14. Input/Output Requirements

REVISION HISTORY

Changes from Revision O (April 1998) to Revision P	Page
• Updated document to new TI datasheet format - no specification changes.	1
• Removed Ordering Information table.	2
• Updated operating temperature range.	5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV123AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV123A	Samples
SN74LV123ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV123A	Samples
SN74LV123ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV123A	Samples
SN74LV123ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV123A	Samples
SN74LV123ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	LV123A	Samples
SN74LV123ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV123A	Samples
SN74LV123ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV123A	Samples
SN74LV123ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV123A	Samples
SN74LV123APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV123A	Samples
SN74LV123APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV123A	Samples
SN74LV123APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	LV123A	Samples
SN74LV123APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV123A	Samples
SN74LV123APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV123A	Samples
SN74LV123ARGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV123A	Samples
SN74LV123ARGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV123A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74LV123A :

- Automotive: SN74LV123A-Q1
- Enhanced Product: SN74LV123A-EP

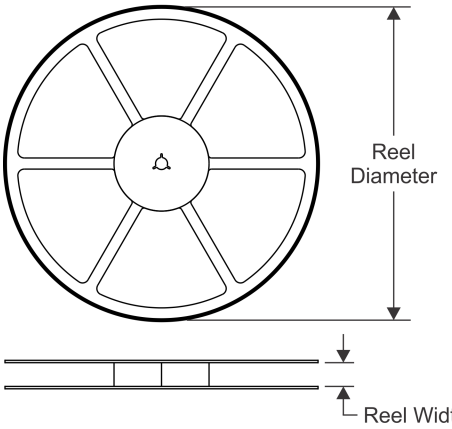
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

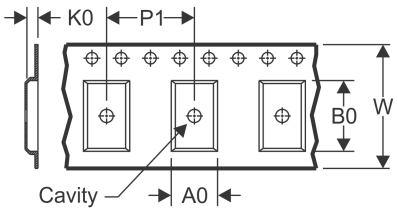
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

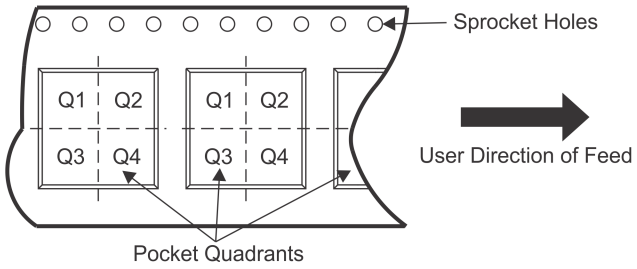


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

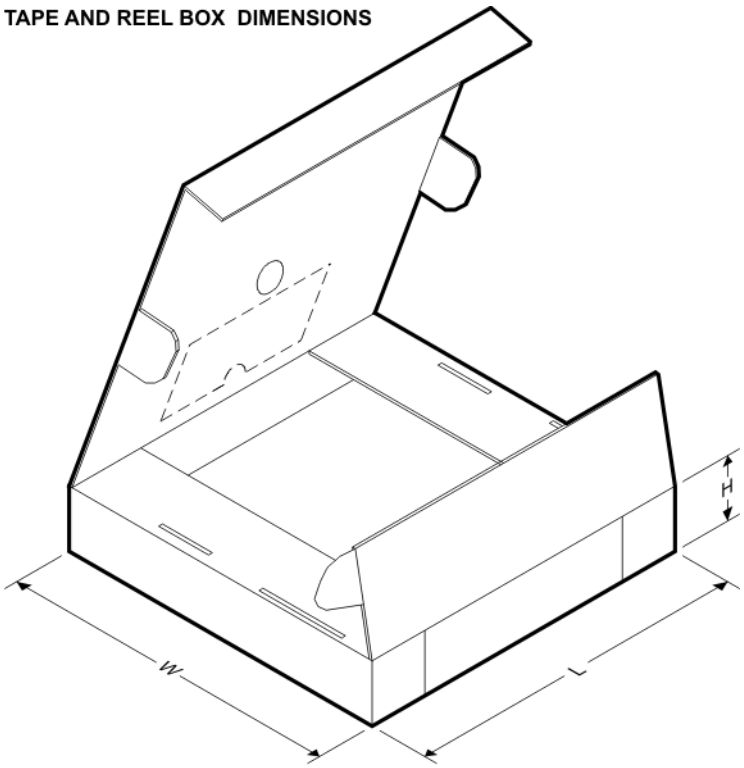
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV123ADBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LV123ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV123ADR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV123ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV123ADRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV123APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV123APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV123APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV123APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV123ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

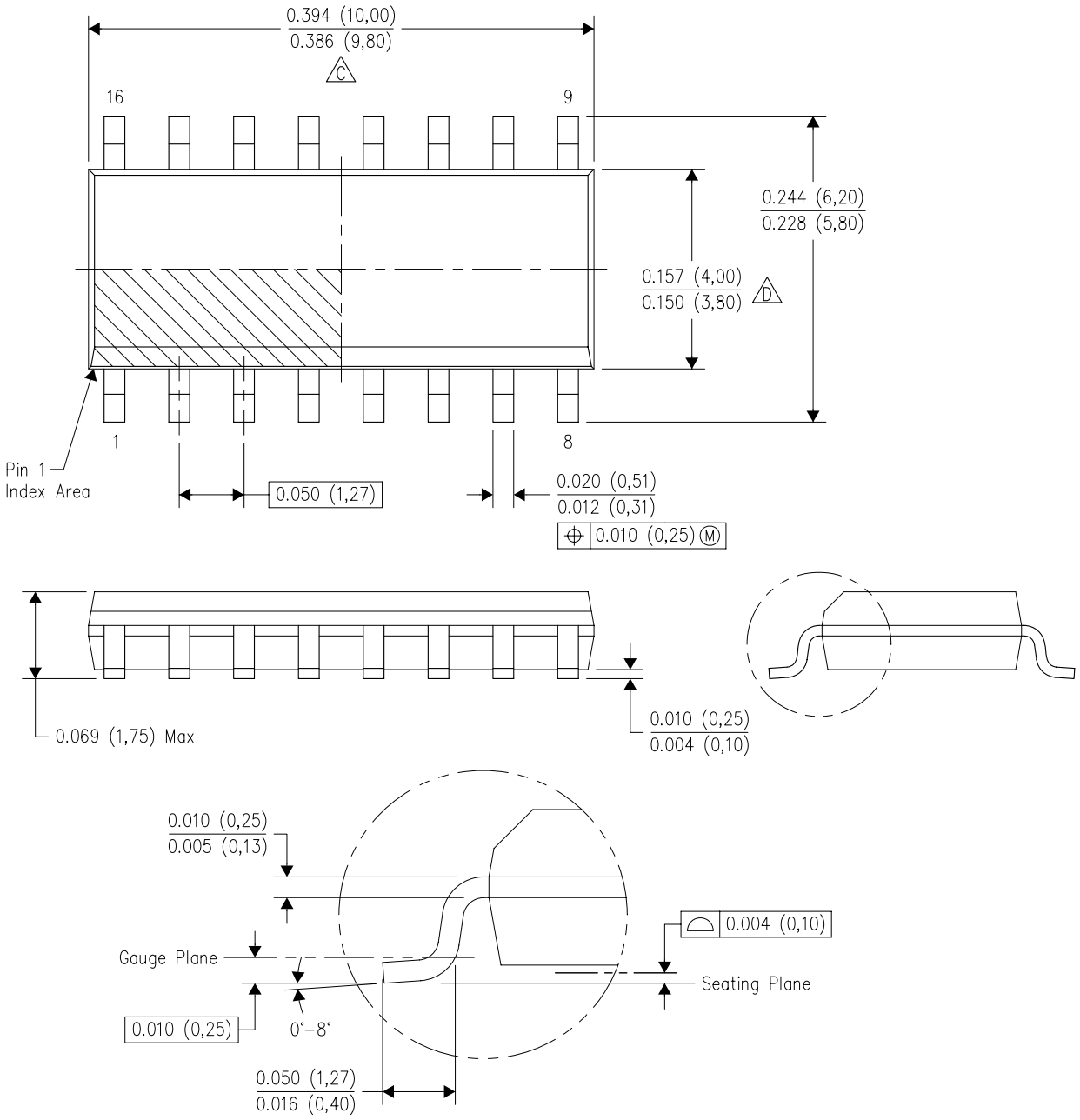
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

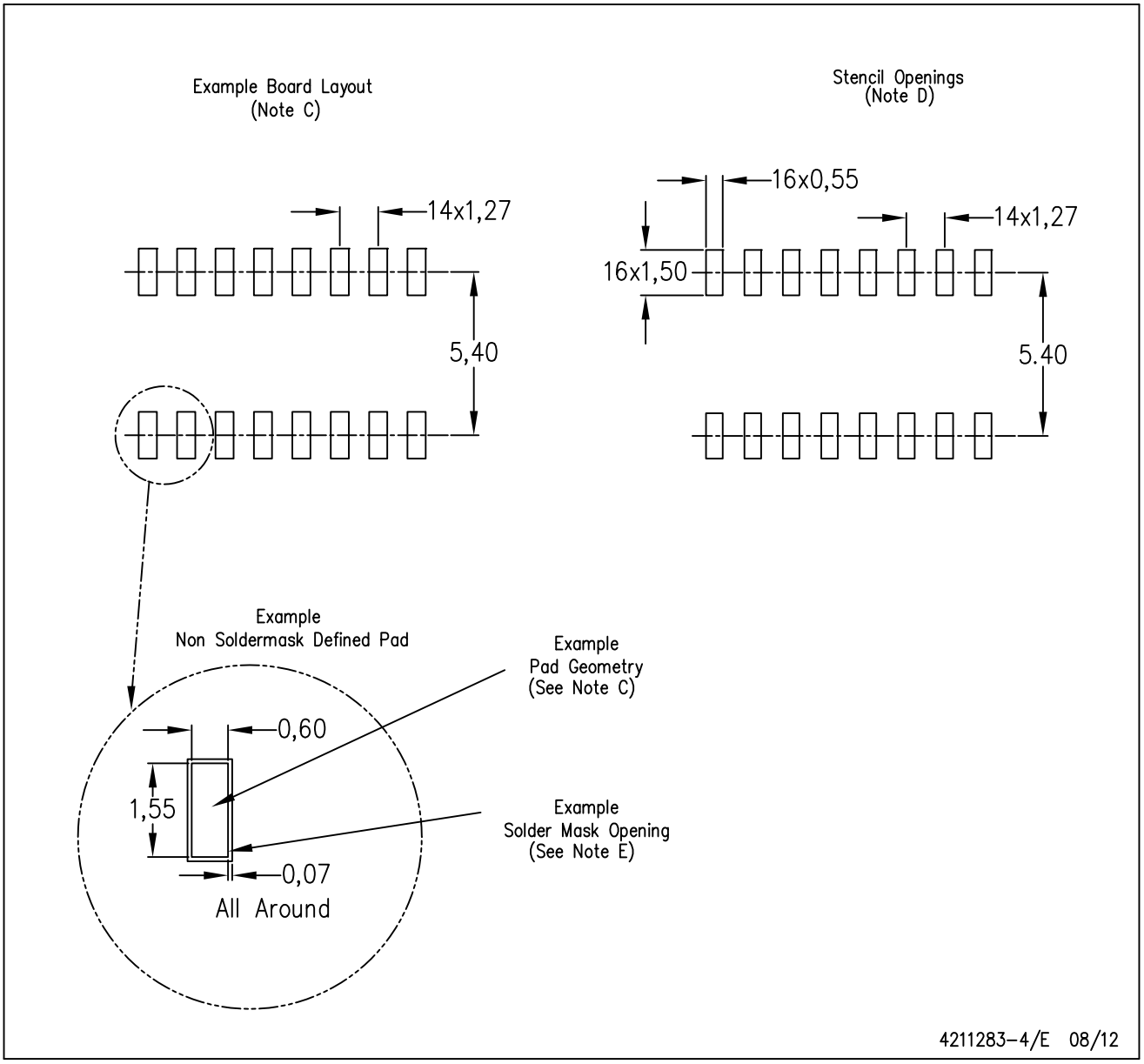
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV123ADBR	SSOP	DB	16	2000	367.0	367.0	38.0
SN74LV123ADGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74LV123ADR	SOIC	D	16	2500	364.0	364.0	27.0
SN74LV123ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV123ADRG4	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV123APWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV123APWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74LV123APWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV123APWT	TSSOP	PW	16	250	367.0	367.0	35.0
SN74LV123ARGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



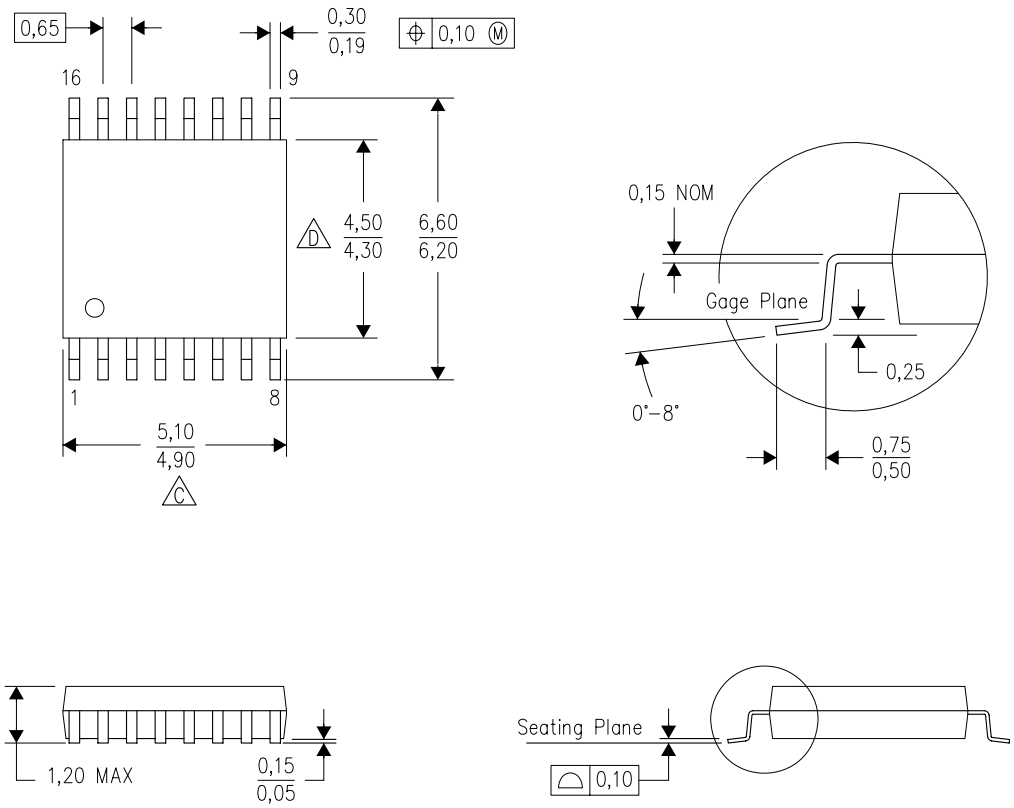
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

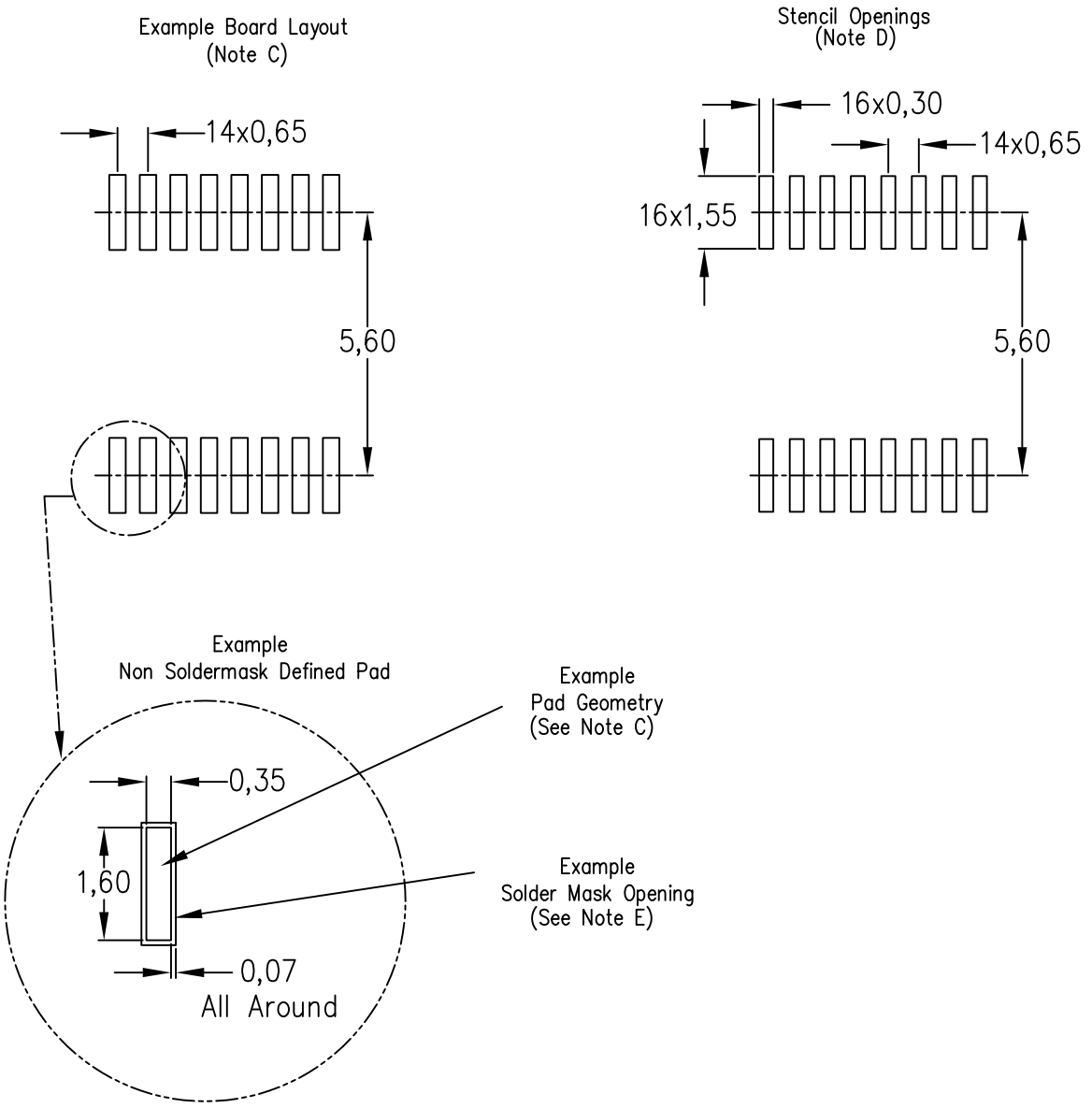
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE

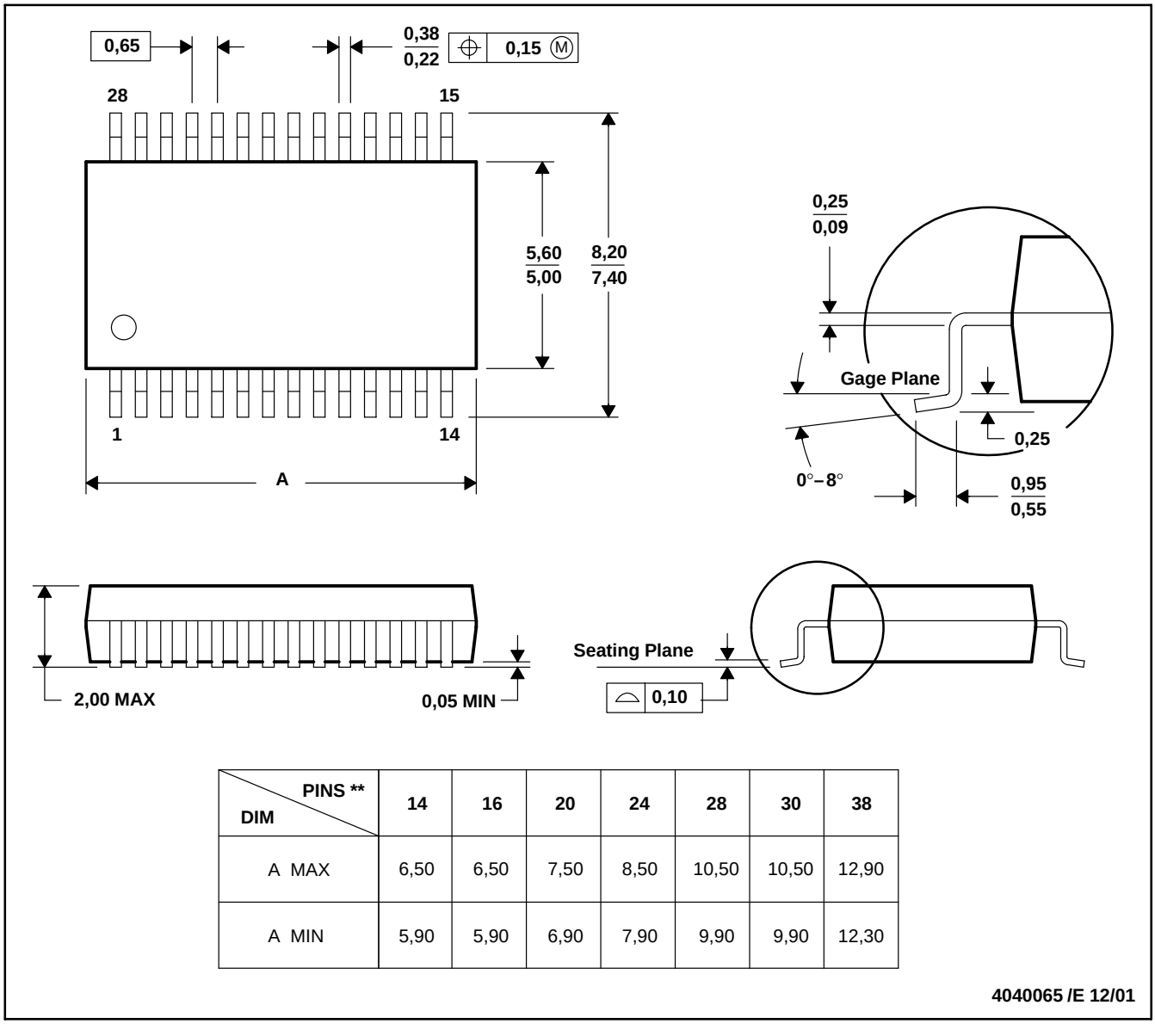


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

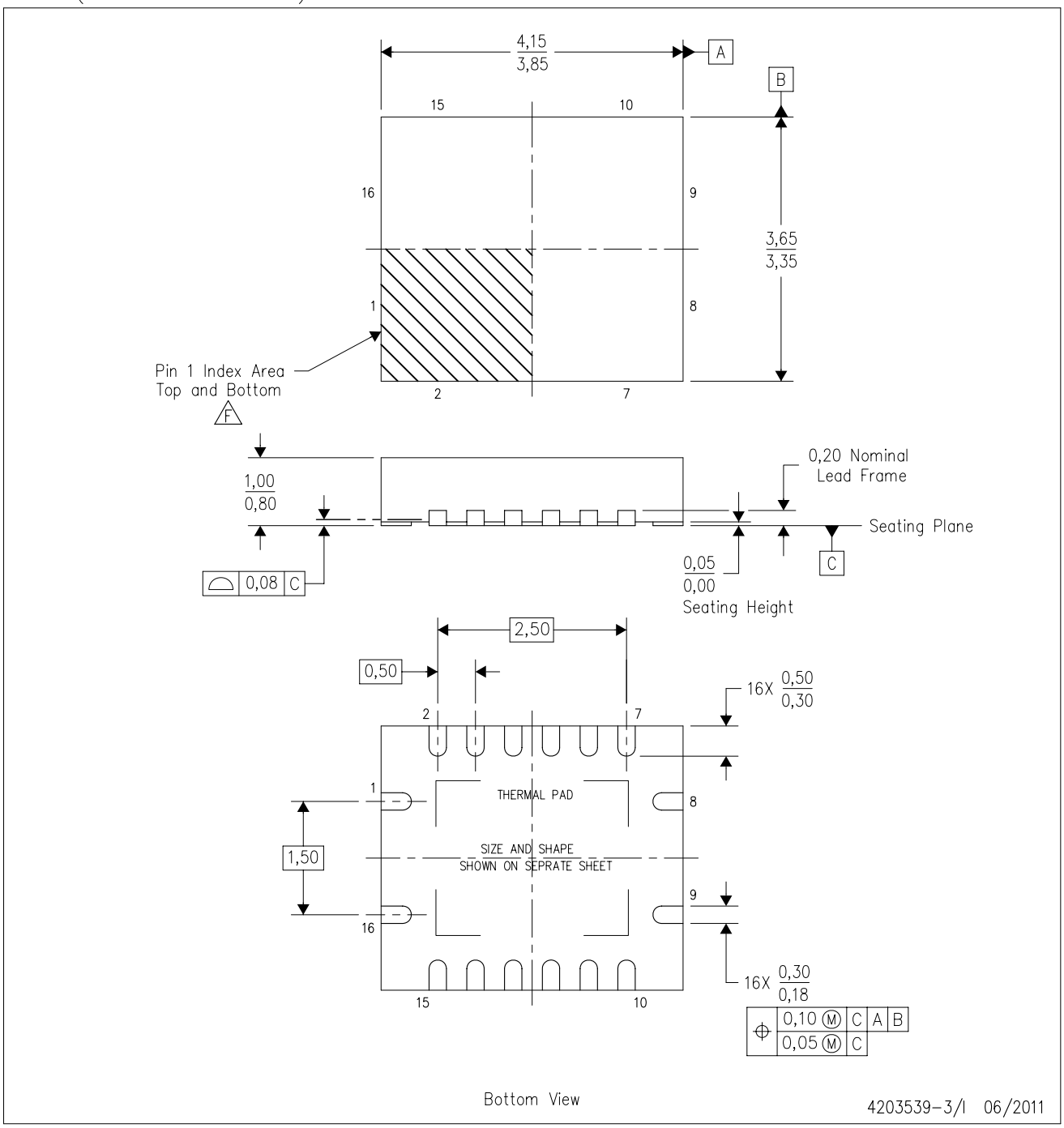


DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

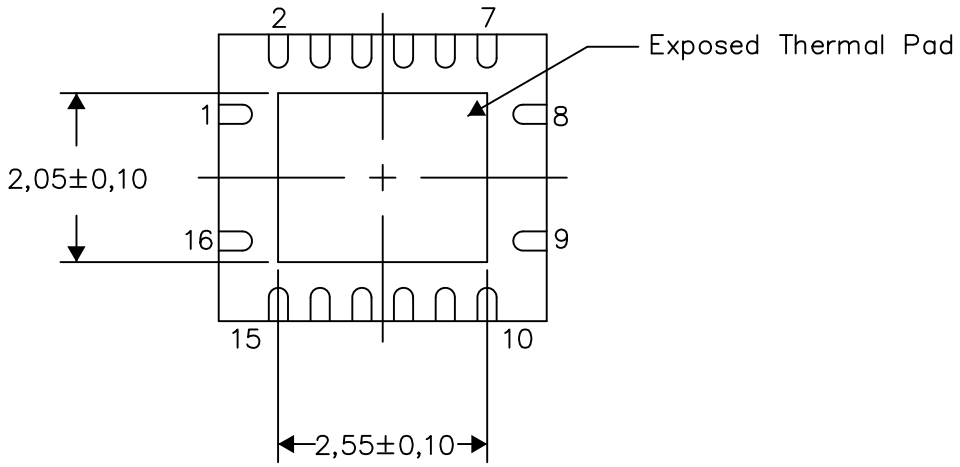
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



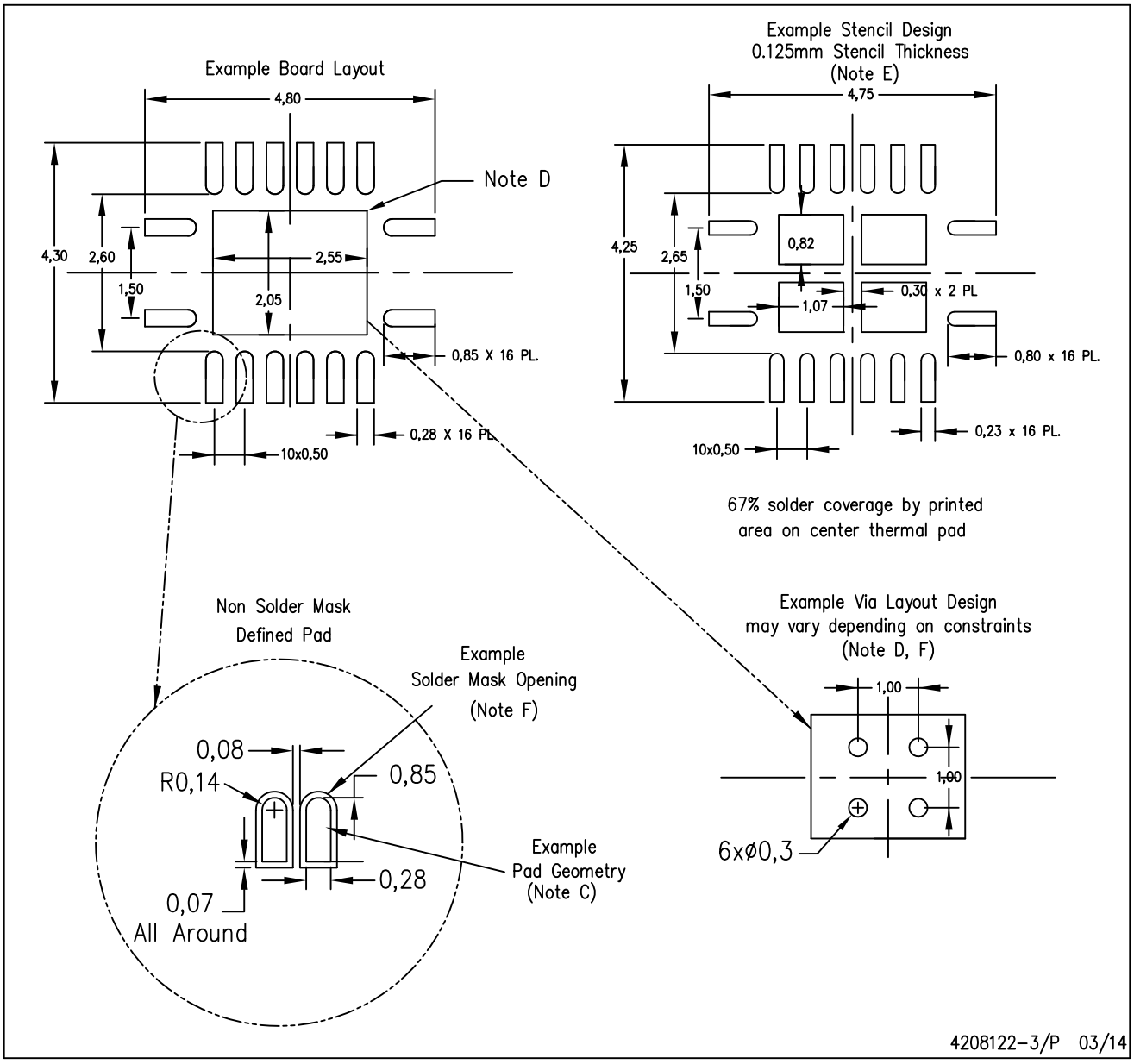
Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

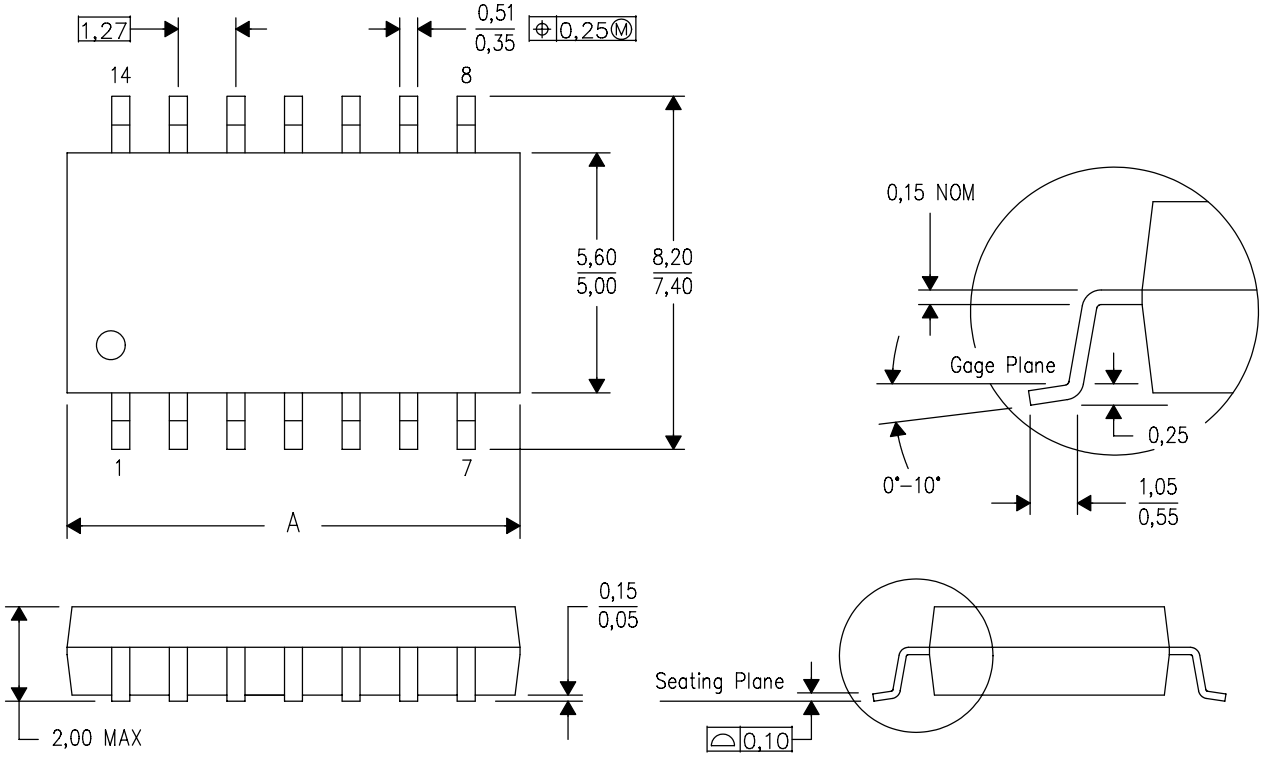


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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