



Matched N-Channel Pairs

PRODUCT SUMMARY					
Part Number	$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	g_{fs} Min (mS)	I_G Typ (pA)	$ V_{GS1} - V_{GS2} $ Typ (mV)
U430	-1 to -4	-25	10	-15	25
U431	-2 to -6	-25	10	-15	25

FEATURES

- Two-Chip Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 15 pA
- Low Noise
- High CMRR: 75 dB

BENEFITS

- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signals

APPLICATIONS

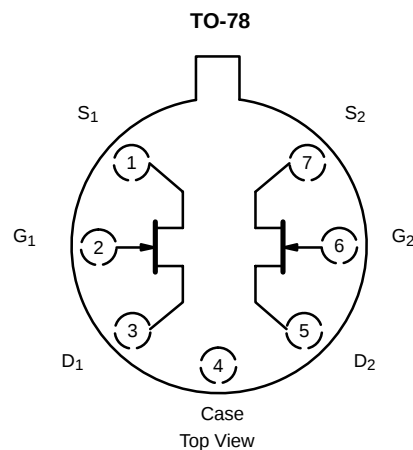
- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters

DESCRIPTION

The U430/431 are matched JFET pairs assembled in a TO-78 package. These devices offer good power gain even at frequencies beyond 250 MHz.

The TO-78 package is available with full military processing (see Military Information).

For similar products, see the low-noise U/SST401 series, the high-gain 2N5911/5912, and the low-leakage U421/423 data sheets.



ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage -25 V
Gate Current 10 mA
Lead Temperature ($1/16$ " from case for 10 sec.) 300 °C
Storage Temperature -65 to 200 °C
Operating Junction Temperature -55 to 150 °C

Power Dissipation : Per Side^a 300 mW
Total^b 500 mW

Notes

- Derate 2.4 mW/°C above 25 °C
- Derate 4 mW/°C above 25 °C



SPECIFICATIONS (T _A = 25° C UNLESS OTHERWISE NOTED)								
Parameter	Symbol	Test Conditions	Typ ^b	Limits				Unit
				U430		U431		
				Min	Max	Min	Max	
Static								
Gate-Source Breakdown Voltage	V _{(BR)GSS}	I _G = -1 μA, V _{DS} = 0 V	-35	-25		-25		V
Gate-Source Cutoff Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 nA		-1	-4	-2	-6	
Saturation Drain Current ^b	I _{DSS}	V _{DS} = 10 V, V _{GS} = 0 V		12	30	24	60	mA
Gate Reverse Current	I _{GSS}	V _{GS} = -15 V, V _{DS} = 0 V	-5		-150		-150	pA
		T _A = 150°C	-10		-150		-150	nA
Gate Operating Current	I _G	V _{DG} = 10 V, I _D = 5 mA	-15					pA
		T _A = 150°C	-10					nA
Gate-Source Forward Voltage	V _{GS(F)}	I _G = 10 mA , V _{DS} = 0 V	0.8		1		1	V
Dynamic								
Common-Source Forward Transconductance ^b	g _{fs}	V _{DS} = 10 V, I _D = 10 mA , f = 1 kHz	15	10		10		mS
Common-Source Output Conductance ^b	g _{os}		100		250		250	μS
Common-Source Input Capacitance	C _{iss}	V _{GS} = -10 V, V _{DS} = 0 V, f = 1 MHz	4.5		5		5	pF
Common-Source Reverse Transfer Capacitance	C _{rss}		2		2.5		2.5	
Equivalent Input Noise Voltage	$\bar{e}_n$	V _{DS} = 10 V, I _D = 10 mA f = 100 Hz	6					nV/ √Hz
High Frequency								
Common-Source Forward Transconductance	g _{fs}	V _{DS} = 10 V, I _D = 10 mA f = 100 MHz	14					mS
Common-Source Output Conductance	g _{os}		0.13					
Power-Match Source Admittance	g _{ig}		12					
Matching								
Differential Gate-Source Voltage	V _{GS1} -V _{GS2}	V _{DG} = 10 V, I _D = 10 mA	25					mV
Saturation Drain Current Ratio ^c	$\frac{I_{DSS1}}{I_{DSS2}}$	V _{DS} = 10 V, V _{GS} = 0 V	0.95	0.9	1	0.9	1	
Transconductance Ratio ^c	$\frac{g_{fs1}}{g_{fs2}}$	V _{DS} = 10 V, I _D = 10 mA, f = 1 kHz	0.95	0.9	1	0.9	1	
Gate-Source Cutoff Voltage Ratio ^c	$\frac{V_{GS(off)1}}{V_{GS(off)2}}$	V _{DS} = 10 V, I _D = 1 nA	0.95	0.9	1	0.9	1	
Differential Gate Current	I _{G1} -I _{G2}	V _{DG} = 10 V, I _D = 5 mA	-2					pA
Common Mode Rejection Ratio	CMRR	V _{DG} = 5 to 10 V, I _D = 10 mA	75					dB

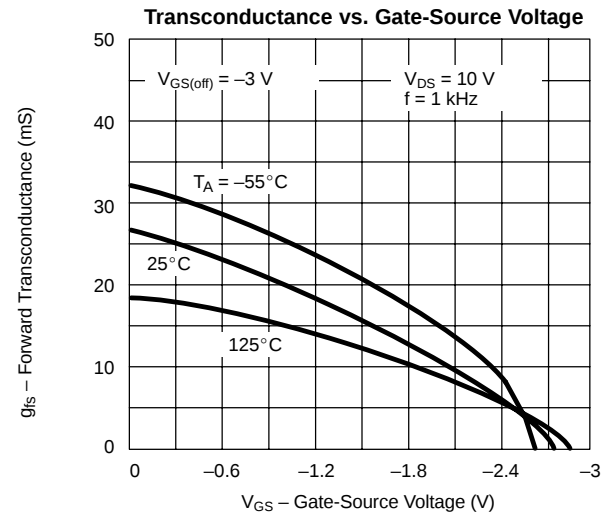
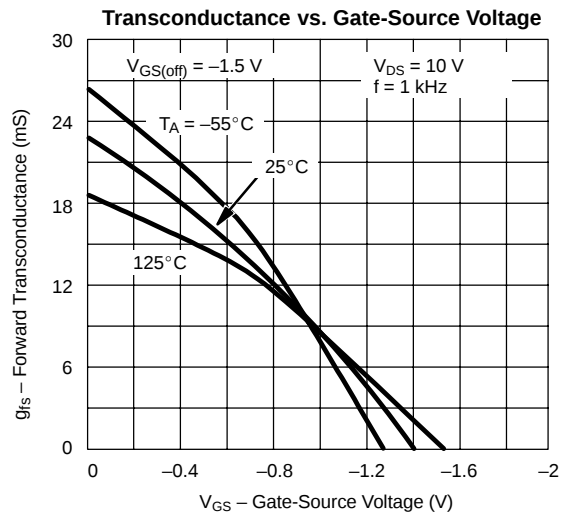
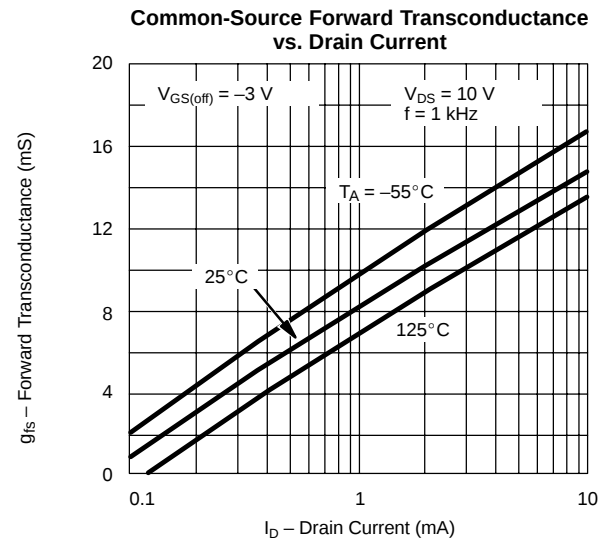
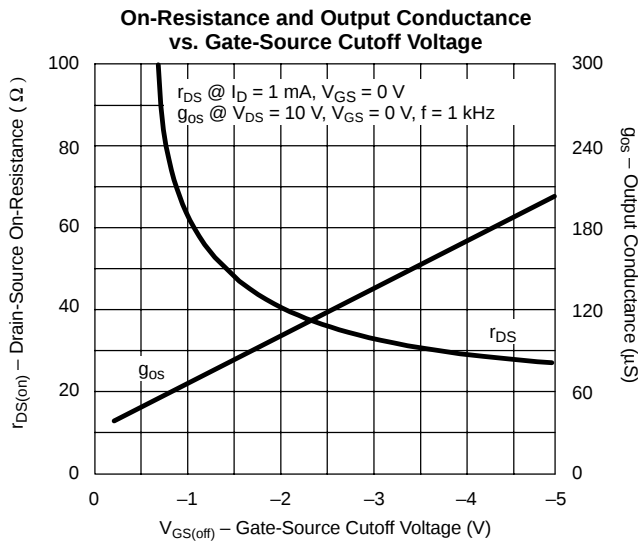
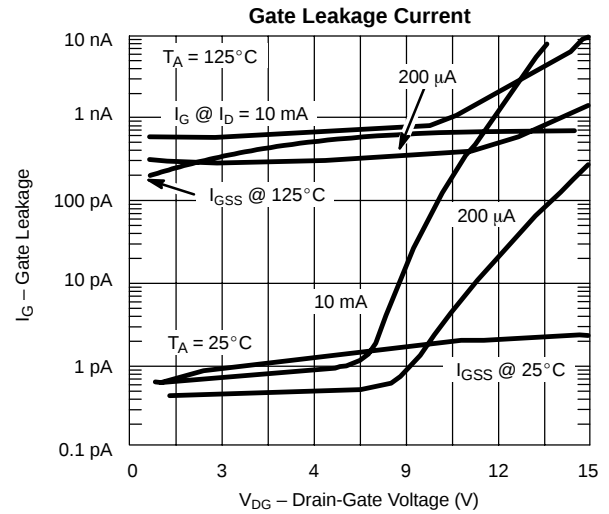
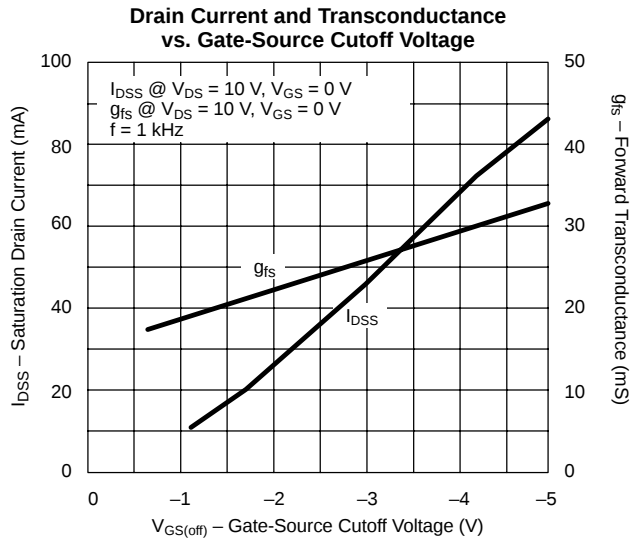
Notes

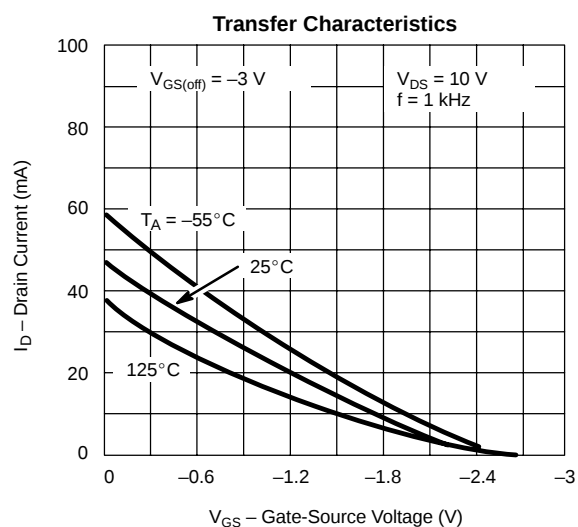
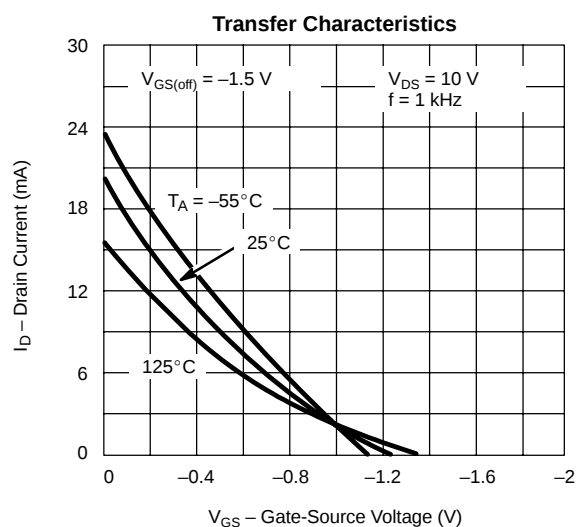
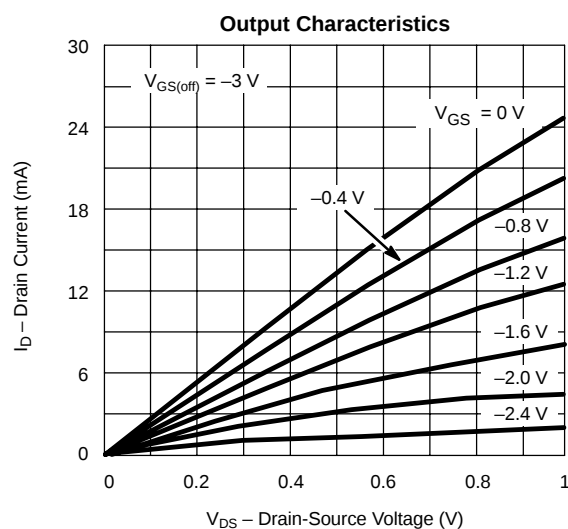
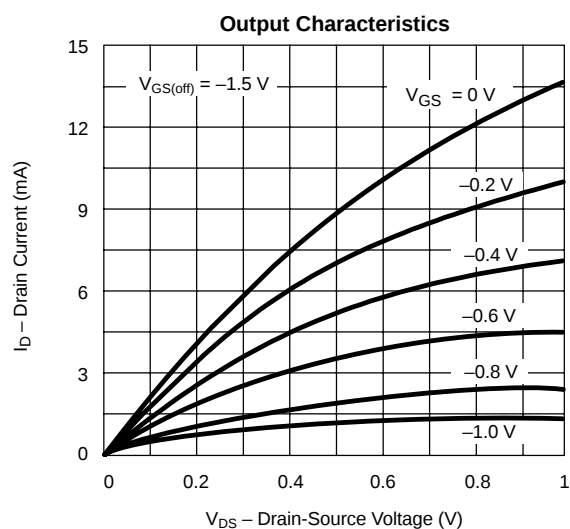
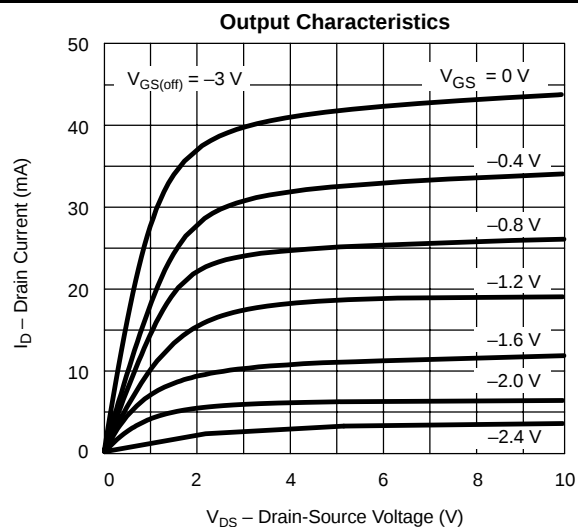
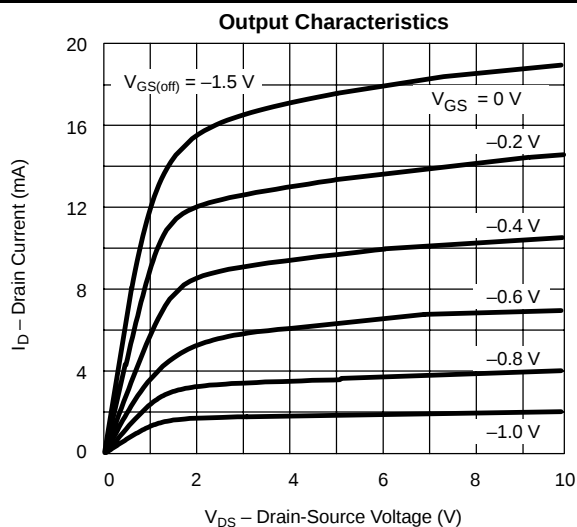
- a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
 b. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.
 c. Assumes smaller value in the numerator.

NZBD



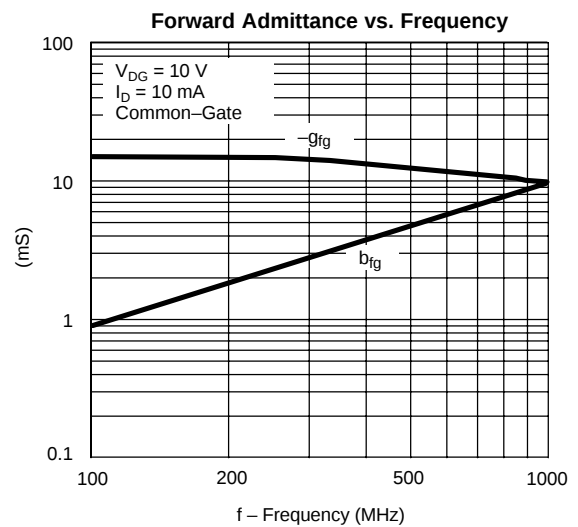
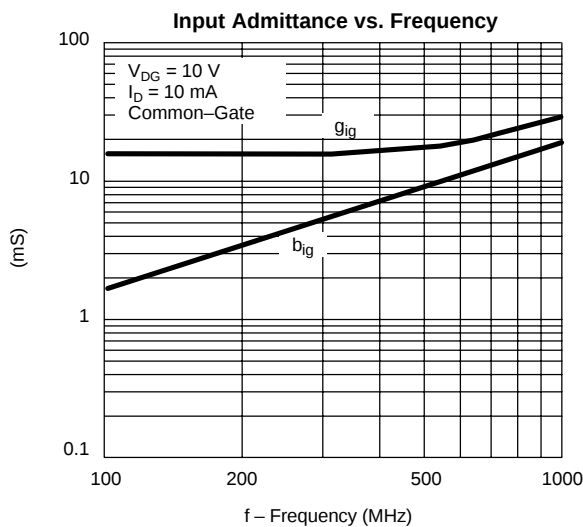
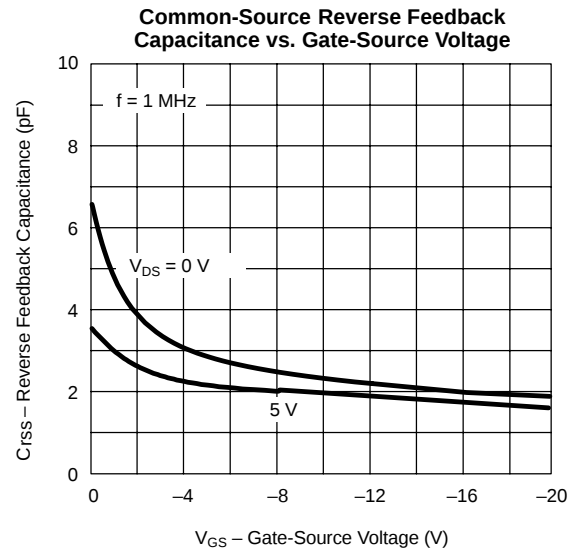
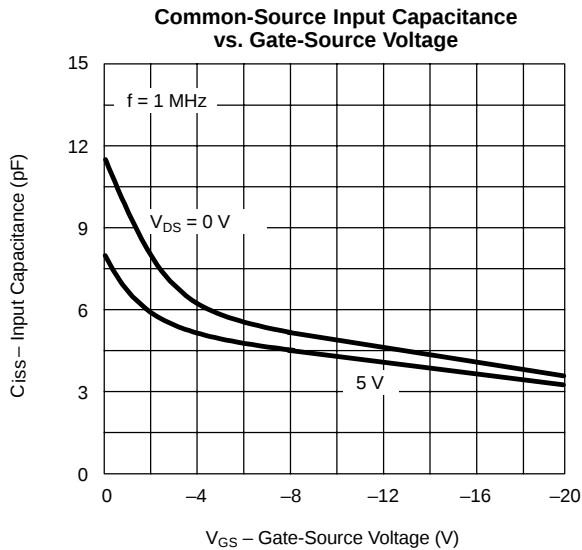
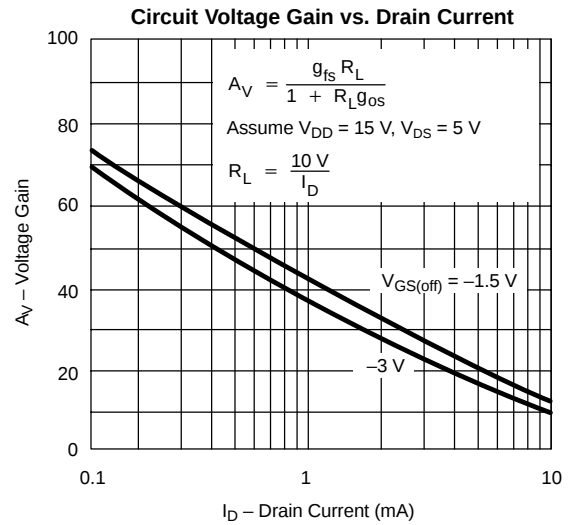
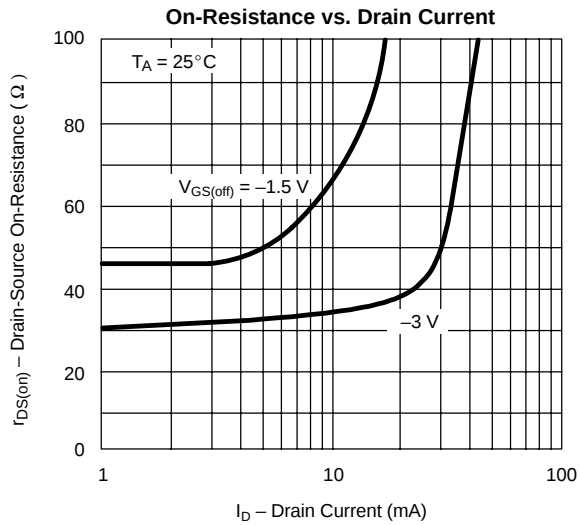
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