

CMOS Logic MN400B Series

MN4021B/MN4021BS

6932852 PANASONIC INDL, ELECTRONIC

66C 04968 D T-46-09-05

MN4021B / MN4021BS

8-Bit Static Shift Registers

Description

The MN4021B/S are 8-bit static shift registers composed of 8 register cells with its own parallel input. Parallel input/series output and parallel input-series output conversion are enabled on the clock synchronization by controlling parallel/series control input (PL).

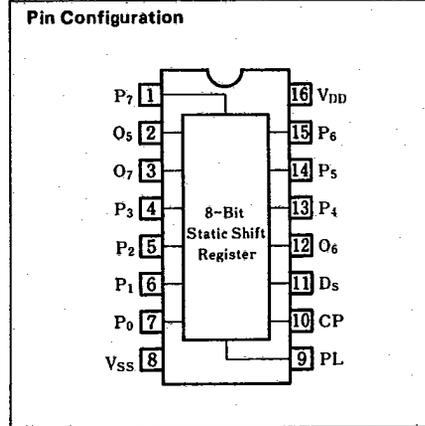
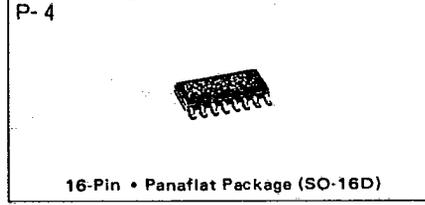
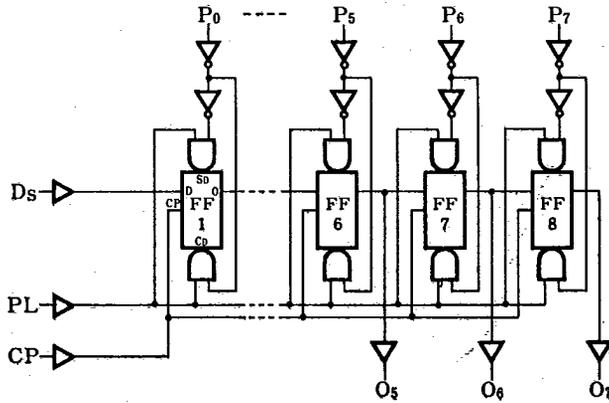
Truth Table

Serial Action				Output		
n	CP	Ds	PL	O _s	O _e	O _t
1	⌊	D ₁	L	×	×	×
2	⌊	D ₂	L	×	×	×
3	⌊	D ₃	L	×	×	×
6	⌊	×	L	D ₁	×	×
7	⌊	×	L	D ₂	D ₁	×
8	⌊	×	L	D ₃	D ₂	D ₁
	⌋	×	L	no change		

Parallel Action				Output		
n	CP	Ds	PL	O _s	O _e	O _t
	×	×	H	P ₃	P _e	P _t

Note) X : don't care
 D_n : H or L
 n : Clock pulse number

Logic Diagram



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■ Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Unit
Supply Voltage	V _{DD}	-0.5~+18	V
Input Voltage	V _I	-0.5~V _{DD} +0.5*	V
Output Voltage	V _O	-0.5~V _{DD} +0.5*	V
Peak Input · Output Current	±I _I	max. 10	mA
Power Dissipation (per package)	P _D	Ta=-40~+60°C	max. 400
		Ta=+60~+85°C	Decrease up to 200mW rating at 8mW/°C
Power Dissipation (per output terminal)	P _D	max. 100	mW
Operating Ambient Temperature	T _{opr}	-40~+85	°C
Storage Temperature	T _{stg}	-65~+150	°C

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V _{DD} (V)	Sym- bol	Conditions	Ta=-40°C		Ta=25°C		Ta=85°C		Unit
				min.	max.	min.	max.	min.	max.	
Quiescent Power Supply Current	5	I _{DD}	V _I =V _{SS} or V _{DD}	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Output Voltage Low Level	5	V _{OL}	V _I =V _{SS} or V _{DD} I _O < 1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V _{OH}	V _I =V _{SS} or V _{DD} I _O < 1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V _{IL}	I _O < 1μA V _O =0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			—	3	—	3	—	3	
	15			—	4	—	4	—	4	
Input Voltage High Level	5	V _{IH}	I _O < 1μA V _O =0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			7	—	7	—	7	—	
	15			11	—	11	—	11	—	
Output Current Low Level	5	I _{OL}	V _O =0.4V, V _I =0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10			1.3	—	1.1	—	0.9	—	
	15			3.6	—	3	—	2.4	—	
Output Current High Level	5	-I _{OH}	V _O =4.6V, V _I =0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10			1.3	—	1.1	—	0.9	—	
	15			3.6	—	3	—	2.4	—	
Output Current High Level	5	-I _{OH}	V _O =2.5V, V _I =0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	±I _I	V _I =0 or 15V	—	0.3	—	0.3	—	1	μA

■ Switching Characteristics (Ta=25°C, V_{SS}=0V, C_L=50pF)

Item	V _{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t _{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t _{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	

CMOS Logic MN4000B Series

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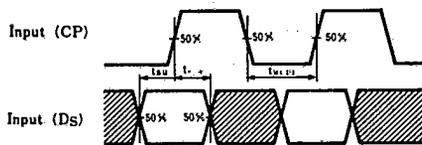
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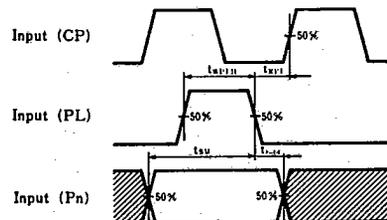
■ Switching Characteristics (Ta=25°C, V_{SS}=0V, C_L=50pF) (Continued)

Item	V _{DD} (V)	Symbol	min.	typ.	max.	Unit
Propagation Delay Time CP→On (H→L)	5	t _{PHL}	—	170	510	ns
	10		—	65	195	
	15		—	45	135	
Propagation Delay Time CP→On (L→H)	5	t _{PLH}	—	130	390	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time PL→On (H→L)	5	t _{PHL}	—	240	720	ns
	10		—	90	270	
	15		—	60	180	
Propagation Delay Time PL→On (L→H)	5	t _{PLH}	—	175	525	ns
	10		—	70	210	
	15		—	50	150	
Set-up Time D _S →CP	5	t _{su}	—	45	135	ns
	10		—	15	45	
	15		—	10	30	
Set-up Time P _n →PL	5	t _{su}	—	70	210	ns
	10		—	25	75	
	15		—	20	60	
Hold Time D _S →CP	5	t _{hold}	—	20	60	ns
	10		—	10	30	
	15		—	8	24	
Hold Time P _n →PL	5	t _{hold}	—	-10	24	ns
	10		—	0	24	
	15		—	0	24	
Minimum Clock Pulse Width	5	t _{wCP}	—	55	165	ns
	10		—	20	60	
	15		—	15	45	
Minimum PL Pulse Width	5	t _{wPL}	—	75	225	ns
	10		—	25	75	
	15		—	20	60	
PL Recovery Time	5	t _{RPL}	—	65	195	ns
	10		—	20	60	
	15		—	15	45	
Maximum Clock Frequency	5	f _{max}	4	9	—	MHz
	10		12	25	—	
	15		18	37	—	
Input Capacitance		C _i	—	—	7.5	pF

● Dynamic Signal Waveforms



Waveforms showing minimum clock pulse width, set-up time and hold time for CP and D_S



Waveforms showing minimum PL pulse width, recovery time for PL, and set-up and hold times for P_n to PL; set-up and hold times are shown as positive values but may be specified as negative values.