



PC Card (PCMCIA) Interface Switch

FEATURES

- Single SO-8 Package
- CMOS-Logic Compatible Inputs
- Slow V_{CC} Ramp Time
- Smart Switching
- Extremely Low R_{ON}
- Reverse Blocking Switches
- Low Power Consumption
- Safe Power Up

DESCRIPTION

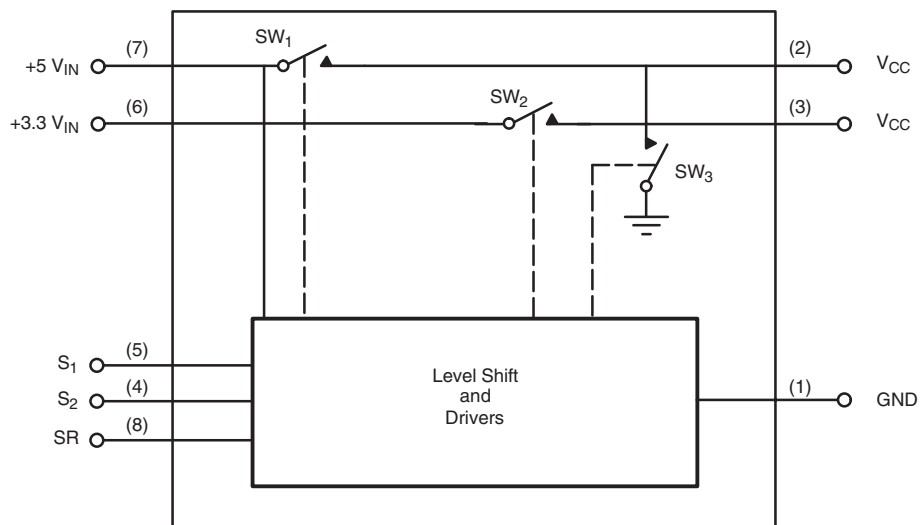
The Si9706DY offers an integrated solution for PC Card power interfaces that only require V_{CC} switching. This part is ideal for systems that operate at 5 V and provide V_{PP} from the main supply or from a dedicated Flash RAM 12-V supply.

The Si9706DY operates off the 5-V supply and has built-in level shifting for gate drive. Internal logic protects against a control logic error that would short 5 V to the 3.3-V supply. This protection logic also allows the Si9706DY to be configured for

positive or negative control logic for compatibility with a variety of PC Card controllers. These control inputs are CMOS logic compatible and can be driven to 3.3 V or 5 V.

The Si9706DY PC Card interface switch is packaged in a narrow body SO-8 package and is rated over the industrial temperature range -40 to 85°C . The Si9706DY is available in lead free.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to Ground

+5 V _{IN}	7 V
+3.3 V _{IN}	7 V
S ₁ , S ₂ (CMOS Inputs)	7 V
All Pins	-0.5 V
I _{OUT} V _{CC} ^a	4 A

PD Max ^b : (T _A = 25°C)	1.59 W
(T _A = 85°C)	0.63 W
Junction Temperature	125°C
Thermal Ratings ^b : R _{ΘJA}	63 °C/W

Notes

- Pins 2, 3 connected together externally.
- Mounted on 1-IN², FR4 PC Board.

RECOMMENDED OPERATING CONDITIONS

+5 V _{IN} (must be present)	5 V ± 10%
+3.3 V _{IN}	3.3 V ± 10%
C _{SR}	33 nF
I _{OUT} V _{CC} ^a	2 A

V _{CC} Load Capacitance	150 μF Max
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Notes

- Pins 2, 3 connected together externally.

SPECIFICATIONS							
Parameter	Symbol	Test Conditions Unless Otherwise Specified $C_{SR} = 33\text{ nF}$, $+5\text{ V}_{IN} = 5\text{ V}$ $+3.3\text{ V}_{IN} = 3.3\text{ V}$, $\text{Low} \leq 0.8\text{ V}$, $\text{High} \geq 2.2\text{ V}$		Limits			Unit
				Min ^a	Typ ^b	Max ^a	
Switch SW ₁							
On-Resistance	R _{ON}	I = 500 mA, S ₁ = High S ₂ = Low	T _A = 25°C		58	70	mΩ
			T _A = 85°C		73	90	
Off Current (V _{CC})	I _{OFF}	$+5\text{ V}_{IN} = 5.5\text{ V}$, $V_{CC} = 0\text{ V}$ S ₁ = S ₂ = Low	T _A = 25°C			1	μA
			T _A = 85°C			10	
Rise Time	t _{S1(on)}	S ₂ = Low, See Figure 1		0.2	1.7	5	ms
Fall Time	t _{S1(off)}			10	30	50	
Switch SW ₂							
On-Resistance	R _{ON}	I = 500 mA, S ₂ = High S ₁ = Low	T _A = 25°C		44	55	mΩ
			T _A = 85°C		55	70	
Off Current ($+3.3\text{ V}_{IN}$)	I _{OFF}	$+3.3\text{ V}_{IN} = 3.6\text{ V}$, $V_{CC} = 0\text{ V}$ S ₁ = S ₂ = Low	T _A = 25°C			1	μA
			T _A = 85°C			10	
Rise Time	t _{S2(on)}	S ₁ = Low, See Figure 1		0.1	0.9	5	ms
Fall Time	t _{S2(off)}			5	20	40	
Switch SW ₃							
On-Resistance	R _{ON}	I = 2 mA, S ₁ = S ₂ = Low	T _A = 25°C		140	400	Ω
			T _A = 85°C		200	500	
Power Supply							
$+5\text{ V}_{IN}$ Current Input (on)	I _{+5VIN(1)}	S ₁ = 0 V, S ₂ = 3 V			20	50	μA
	I _{+5VIN(2)}	S ₁ = 3 V, S ₂ = 0V			20	50	
$+5\text{ V}_{IN}$ Current Input (off)	I _{+5VIN(3)}	S ₁ = S ₂ = 0 V			< 1	10	
Input Voltage High	V _{I(H)}	$+5\text{ V}_{IN} = 5.5\text{ V}$	2.2	1.8			V
		$+5\text{ V}_{IN} = 4.5\text{ V}$	2.2	1.6			
Input Voltage Low	V _{I(L)}	$+5\text{ V}_{IN} = 5.5\text{ V}$		1.6	0.8		
		$+5\text{ V}_{IN} = 4.5\text{ V}$		1.4	0.8		
Input Current High	I _{I(H)}	S ₁ , S ₂ = 5 V				1.0	μA
Input Current Low	I _{I(L)}	S ₁ , S ₂ = GND	-1.0				

Notes

- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

TIMING WAVEFORMS

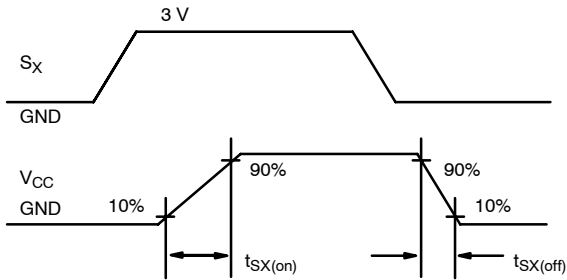


FIGURE 1. Switch Ramp

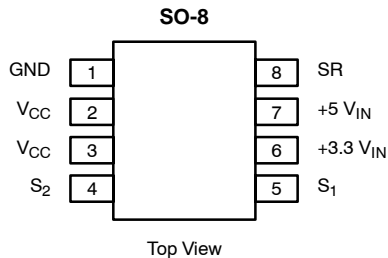
TRUTH TABLE

S ₁	S ₂	Switch 1	Switch 2	Switch 3
0	0	Off	Off	On
0	1	Off	On	Off
1	0	On	Off	Off
1	1	Off	Off	On

Notes

- a. The smart switching of the Si9706DY avoids potential host damage by defaulting to off during error conditions.

PIN CONFIGURATION AND DESCRIPTION



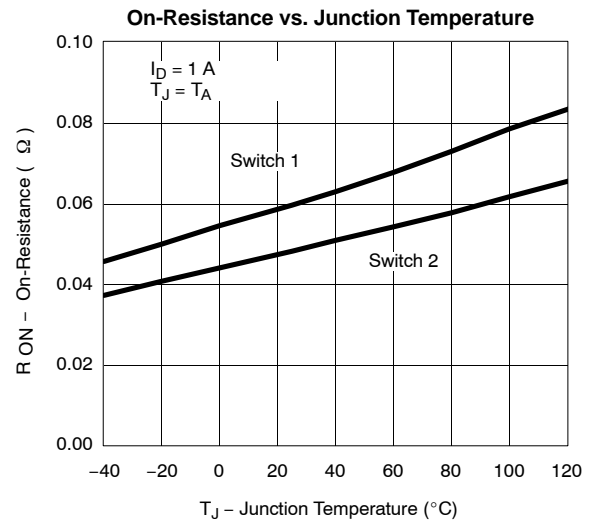
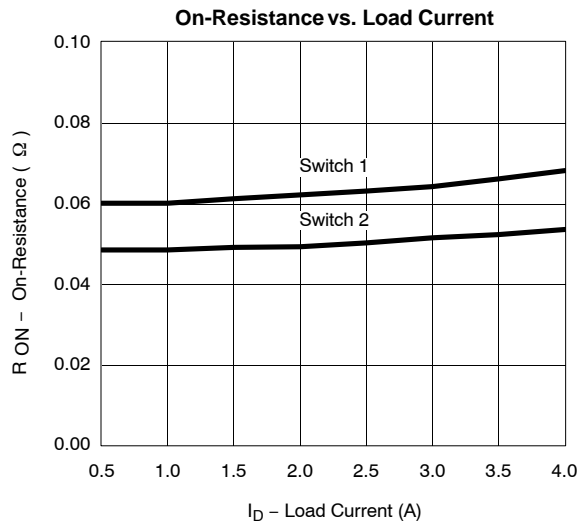
Top View

Pin	Function	Description
1	GND	Ground connection.
2, 3	V _{CC}	Supply voltage to slot.
4	S ₂	Control input for selecting +3.3 V _{IN} to V _{CC} .
5	S ₁	Control input for selecting +5 V _{IN} to V _{CC} .
6	+3.3 V _{IN}	+3.3-V supply.
7	+5 V _{IN}	+5-V supply.
8	SR	Slew rate control pin.

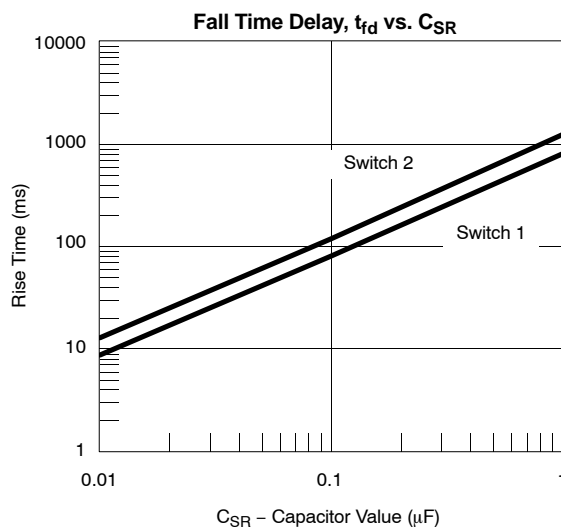
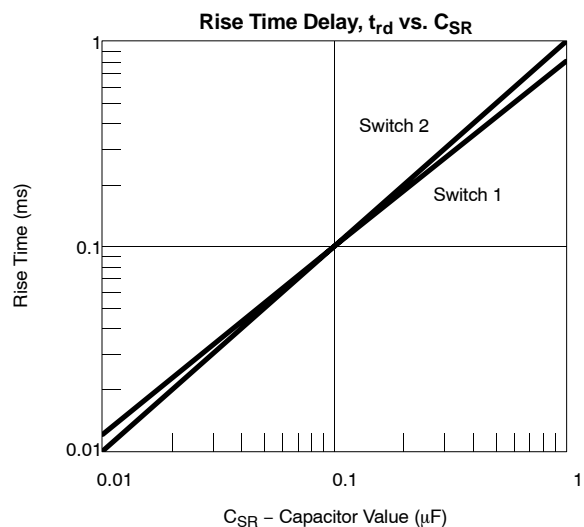
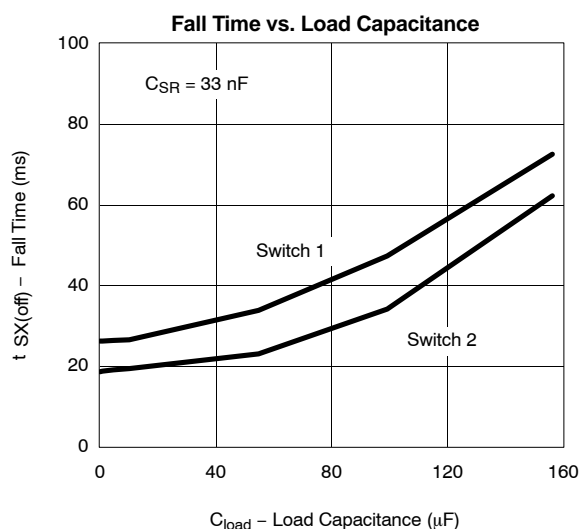
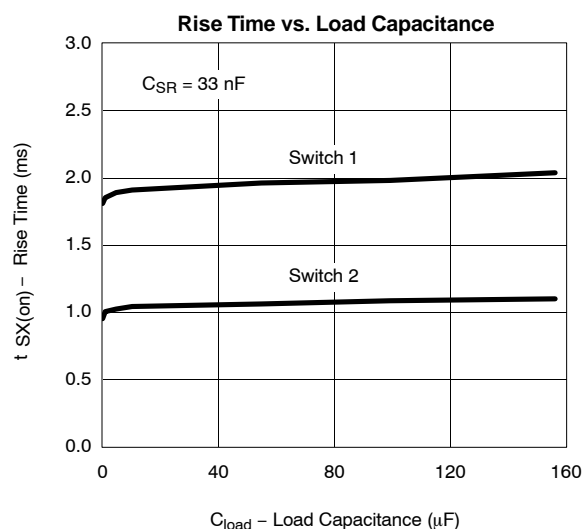
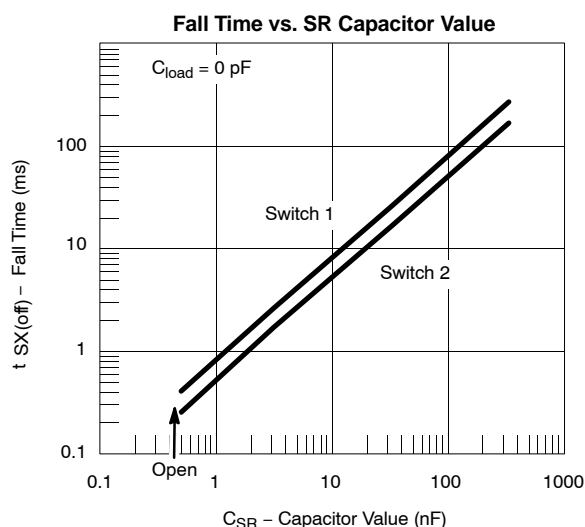
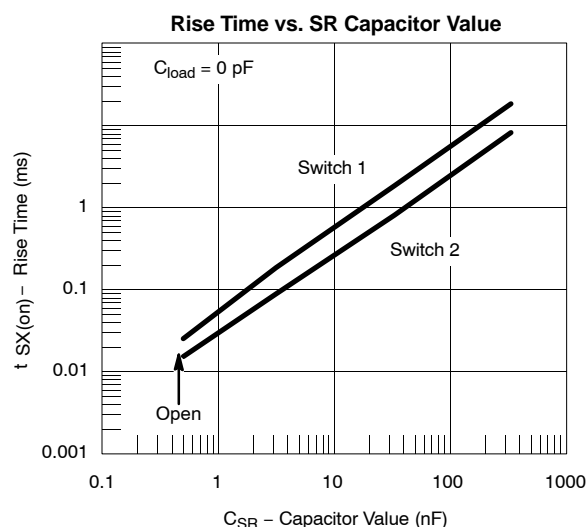
ORDERING INFORMATION

Part Number	Temperature Range
Si9706DY-T1	-40 to 85 °C
Si9706DY-T1—E3 (Lead Free)	

TYPICAL CHARACTERISTICS (25 °C UNLESS OTHERWISE NOTED)



TYPICAL CHARACTERISTICS (25 °C UNLESS OTHERWISE NOTED)



SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				



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