MP7745

2 x 20W Class D Stereo Single Ended Audio Amplifer

The Future of Analog IC Technology

DESCRIPTION

The MP7745 is a Stereo 2 x 20W Class D Audio Amplifier. It is one of MPS' products of fully integrated audio amplifiers which dramatically reduces solution size by integrating the following:

250mΩ power MOSFETs

Startup / Shutdown pop elimination

Short circuit protection circuits

The MP7745 utilizes a single ended output structure capable of delivering 20W per channel into 4Ω speakers. MPS Class D Audio Amplifiers exhibit the high fidelity of a Class A/B amplifier at high efficiencies. The circuit is based on the MPS' proprietary variable frequency topology that delivers excellent linearity, fast response time and operates on a single power supply.

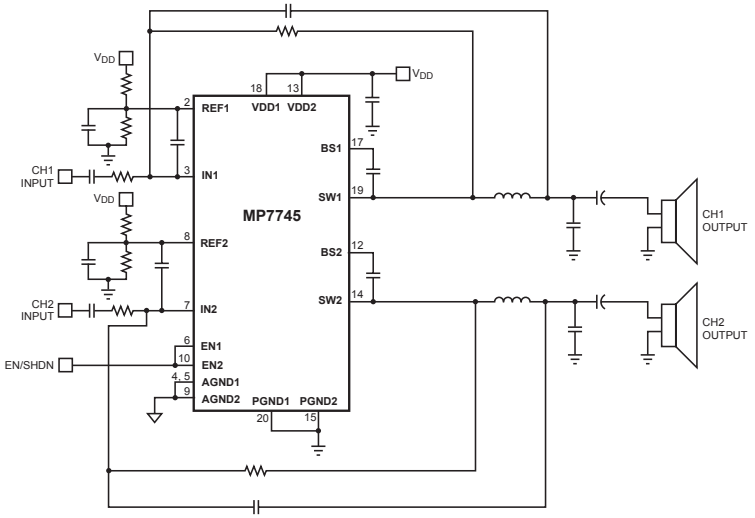
FEATURES

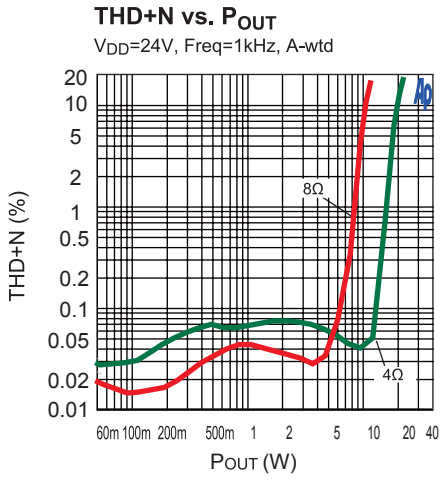
- 2 x 20W Output at V_{DD} = 24V into 4Ω load
- THD+N = 0.05% at 1W, 8Ω
- 93% Efficiency at 20W, 4Ω & V_{DD} = 24V
- Low Noise (103μV Typical)
- Switching Frequency Up to 1MHz
- 9.5V to 26V Operation from a Single Supply
- Integrated Startup and Shutdown Pop Elimination Circuit
- Thermal and Short Circuit Protection
- Integrated Power FETs
- Pin Compatible with MP7722 and MP7742
- Available in TSSOP20-Exposed Package

APPLICATIONS

- Flat Panel TV
- Portable Docking Stations
- Surround Sound DVD Systems
- Televisions
- Multimedia Computers
- Home Stereo Systems

TYPICAL APPLICATION



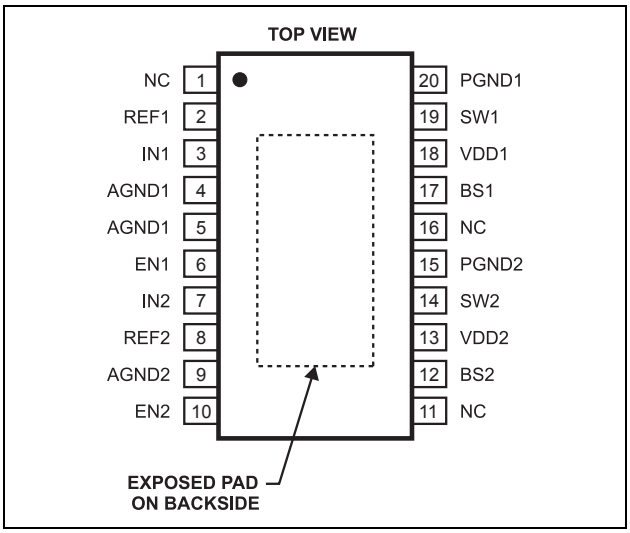


ORDERING INFORMATION

Part Number*	Package	Top Marking	Temperature
MP7745DF	TSSOP20F	MP7745DF	–40°C to +85°C

*For Tape & Reel, add suffix –Z (e.g. MP7745DF–Z). For Lead Free, add suffix –LF (e.g. MP7745DF–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{DD} 32V
BS Voltage ..... V_{SW} – 0.3V to V_{SW} + 6.5V
Enable Voltage V_{EN} .....–0.3V to +6V
V_{SW} .....–1V (-5V for <10nS) to V_{DD} + 1V
V_{PIN}, V_{NIN} ..... –1V to V_{DD} + 1V
AGND to PGND .....–0.3V to +0.3V
Continuous Power Dissipation (T_A = +25°C) (2)
……...3.1W
Junction Temperature .....150°C
Lead Temperature .....260°C
Storage Temperature..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{DD} .....9.5V to 26V
Operating Temperature T_A..... –40°C to +85°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
TSSOP20F	40	6	°C

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD5 1-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS (5, 6)

V_{DD} = 24V, V_{EN} = 5V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Standby Current		V_{EN} = 0V		40	100	µA
Quiescent Current		SW=0V		3	6	mA
Output Drivers						
SW On Resistance		Sourcing and Sinking		0.25		Ω
Short Circuit Current		Sourcing and Sinking		4.5		A
Inputs						
REF1/2, IN1/2, Input Common Mode Voltage Range			0	$\frac{V_{DD}}{2}$	V_{DD} – 1.5	V
REF1/2, IN1/2, Input Current		V_{PIN} = V_{NIN} = 12V		1	5	µA
EN Enable Threshold Voltage		V_{EN} Rising		1.8	2.5	V
		V_{EN} Falling	0.8	1.2		V
EN Enable Input Current		V_{EN} = 5V		1		µA
Thermal Shutdown						
Thermal Shutdown Trip Point		T_J Rising		150		°C
Thermal Shutdown Hysteresis				30		°C

Note:

5) The device is not guaranteed to function outside its operating rating.
6) Electrical Characteristics are for the IC only with no external components except bypass capacitors.

OPERATING SPECIFICATIONS (7)

Circuit of Figure 1, V_{DD} = 24V, V_{EN} = 5V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition		Min	Typ	Max	Units
Standby Current		V_{EN} = 0V			260		μA
Quiescent Current					26		mA
Power Output		f = 1KHz, THD+N = 10%, 4Ω Load			20.0		W
		f = 1KHz, THD+N = 10%, 8Ω Load			11.0		W
THD+ Noise		P_{OUT} = 1W, f = 1KHz, 4Ω Load			0.07		%
		P_{OUT} = 1W, f = 1KHz, 8Ω Load			0.05		%
Efficiency		f = 1KHz, P_{OUT} =20W, 4Ω Load			93		%
		f = 1KHz, P_{OUT} =11W, 8Ω Load			96		%
Maximum Power Bandwidth					20		KHz
Dynamic Range					97		dB
Noise Floor		A-Weighted			103		μV
Power Supply Rejection		V_{RIPPLE}=200mV_{PP} C_R=100μF, Input ac-grounded	f = 217Hz		-56		dB
			f = 1kHz		-59		dB

Note:

7) Operating Specifications are for the IC in Typical Application circuit (Figure 1).

PIN FUNCTIONS

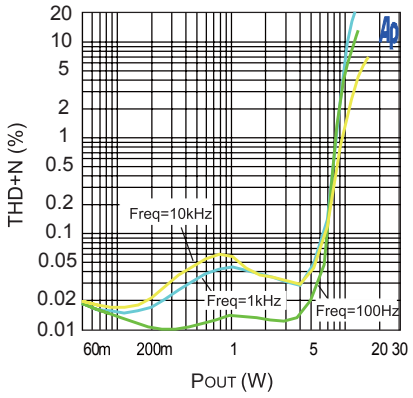
Pin #	Name	Description
1, 11, 16	NC	No Connect. Not internally connected
2	REF1	Amplifier 1 Reference. REF1 is the reference point for amplifier 1. Use a resistive voltage divider to set the voltage at REF1 to $V_{DD}/2$.
3	IN1	Amplifier 1 Input. IN1 is the inverting input for amplifier 1.
4, 5	AGND1	Analog Ground 1. Connect AGND1 to AGND2.
6	EN1	Enable Input 1. EN1 must be connected to EN2. Drive EN1 high to enable MP7745; low to disable it.
7	IN2	Amplifier 2 Input. IN2 is the inverting input for amplifier 2.
8	REF2	Amplifier 2 Reference. REF2 is the reference point for amplifier 2. Use a resistive voltage divider to set the voltage at REF2 to $V_{DD}/2$.
9	AGND2	Analog Ground 2. Connect AGND2 to AGND1.
10	EN2	Enable Input 2. EN2 must be connected to EN1. Drive high to enable MP7745, drive low to disable.
12	BS2	High-Side MOSFET Bootstrap Input for Amplifier 2. A capacitor from BS2 to SW2 supplies the gate drive current to the internal high-side MOSFET. Connect a 0.1μF~1μF capacitor from SW2 to BS2.
13	VDD2	Power Supply Input. Bypass VDD2 to PGND2 with a 1μF X7R capacitor (in addition to the main bulk capacitor), placed close to the IC PIN13 and PIN15.
14	SW2	Switched Power Output. SW2 is the output of Amplifier 2. Connect the LC filter to this pin.
15	PGND2	Power Ground for Amplifier 2. Connect PGND2 to PGND1.
17	BS1	High-Side MOSFET Bootstrap Input for Amplifier 1. A capacitor from BS1 to SW1 supplies the gate drive current to the internal high-side MOSFET. Connect a 0.1μF~1μF capacitor from SW1 to BS1. See Figure 1.
18	VDD1	Power Supply Input. Bypass VDD1 to PGND1 with a 1μF X7R capacitor (in addition to the main bulk capacitor), placed close to the IC PIN18 and PIN20.
19	SW1	Switched Power Output. SW1 is the output of Amplifier 1. Connect the LC filter to this pin. See Figure 1.
20	PGND1	Power Ground for Amplifier 1. Connect PGND1 to PGND2. See Figure 1.
	Exposed Pad	Connect exposed pad to GND plane for proper thermal performance.

TYPICAL PERFORMANCE CURVES

Circuit of Figure 1, V_{DD}=24V, V_{EN}=5V, A_V=8.25V/V, input signal frequency FREQ = 1kHz, T_A = +25°C, unless otherwise noted.

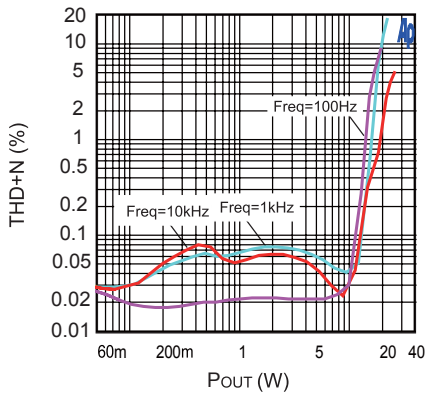
THD+N vs. P_{OUT}

V_{DD}=24V, R_{LOAD}=8Ω, A-wtd



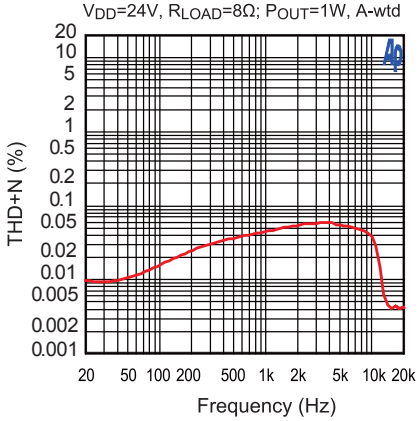
THD+N vs. P_{OUT}

V_{DD}=24V, R_{LOAD}=4Ω, A-wtd



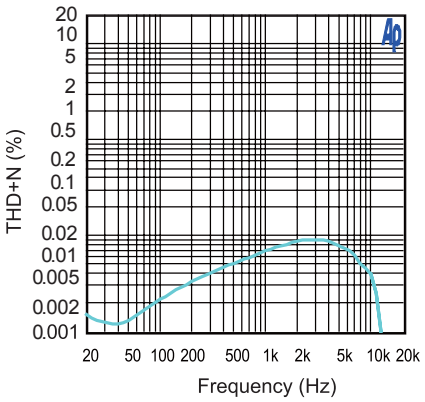
THD+N vs. Frequency

V_{DD}=24V, R_{LOAD}=8Ω; P_{OUT}=1W, A-wtd



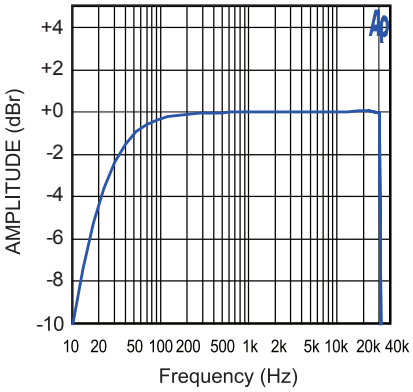
THD+N vs. Frequency

V_{DD}=24V, R_{LOAD}=4Ω, P_{OUT}=1W, A-wtd



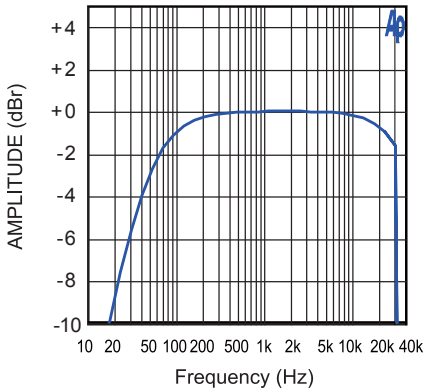
Frequency Response

V_{DD}=24V, R_{LOAD}=8Ω, P_{OUT}=1W



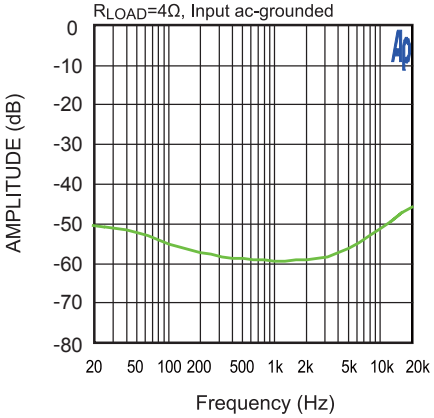
Frequency Response

V_{DD}=24V, R_{LOAD}=4Ω, P_{OUT}=1W



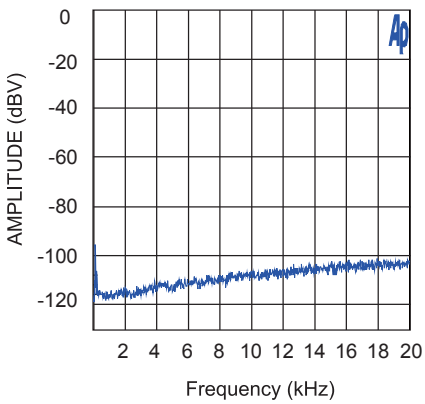
Power Supply Rejection Ratio

V_{DD}=24V, V_{RIPPLE}=0.2V_{PP}, C_R=100uF, R_{LOAD}=4Ω, Input ac-grounded



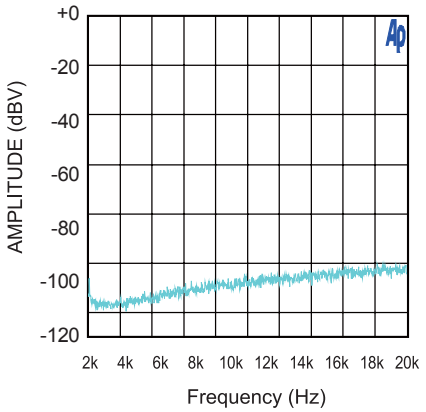
FFT Noise Floor

V_{DD}=24V, R_{LOAD}=4Ω



FFT Noise Floor

V_{DD}=24V,R_{LOAD}=8Ω

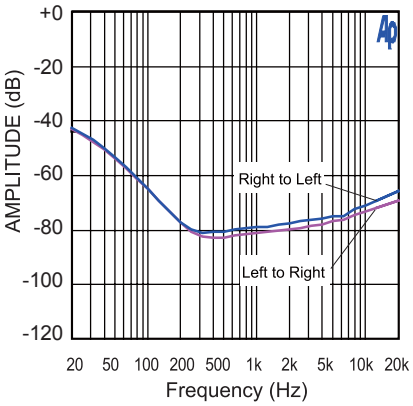


TYPICAL PERFORMANCE CURVES *(continued)*

Circuit of Figure 1, V_{DD}=24V, V_{EN}=5V, A_V=8.25V/V, input signal frequency FREQ = 1kHz, T_A = +25°C, unless otherwise noted.

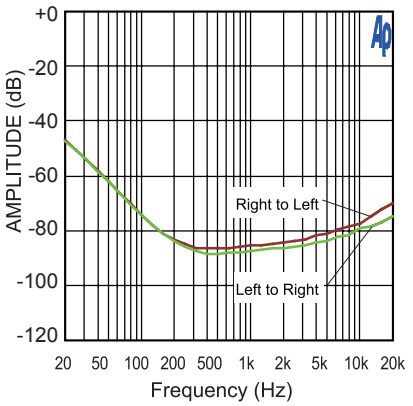
Cross Talk

V_{DD}=24V,R_{LOAD}=4Ω,P_{OUT}=5W



Cross Talk

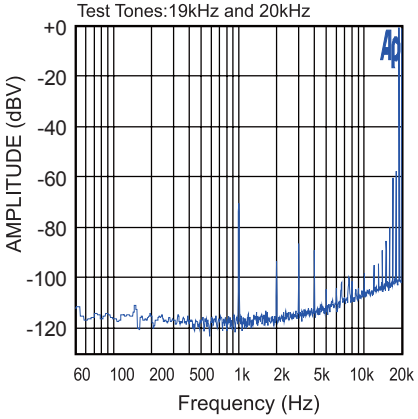
V_{DD}=24V,R_{LOAD}=8Ω,P_{OUT}=5W



IHF-IMD

V_{DD}=24V,R_{LOAD}=4Ω,P_{OUT}=1W

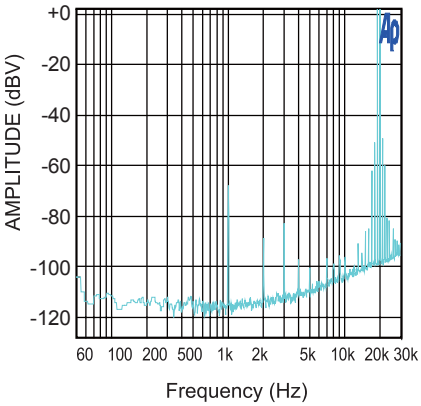
Test Tones:19kHz and 20kHz



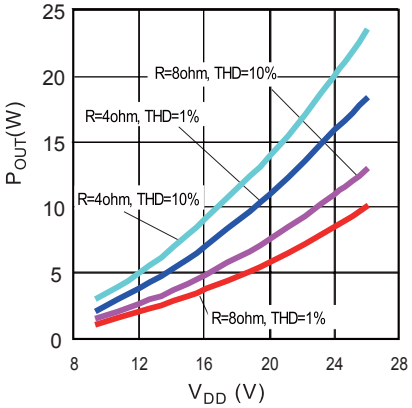
IHF-IMD

V_{DD}=24V,R_{LOAD}=8Ω,P_{OUT}=1W

Test Tones:19kHz and 20kHz

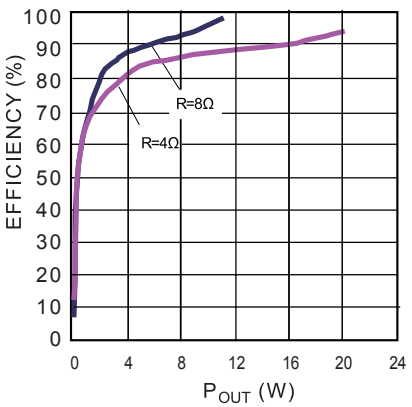


P_{OUT} vs. V_{DD}



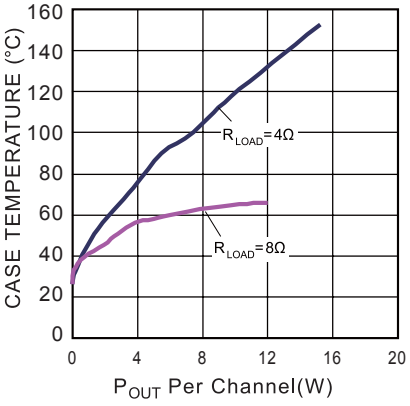
Efficiency vs. P_{OUT}

V_{DD}=24V



Thermal Rise vs. P_{OUT}

V_{DD}=24V, The same P_{OUT} for both channels



OPERATION

The MP7745 is a single-ended Class D audio amplifier. It uses the Monolithic Power Systems patented Analog Adaptive Modulation™ to convert the audio input signal into pulses. These pulses drive an internal high-current output stage and, when filtered through an external inductor-capacitor filter, reproduce the input signal across the load. Because of the switching Class D output stage, power dissipation in the amplifier is drastically reduced when compared to Class A, B or A/B amplifiers while maintaining high fidelity and low distortion.

The amplifier uses differential input to the modulator. PIN is the positive input and NIN is the negative input. The common mode voltage of the input is set to half the DC power supply input voltage (V_{DD}/2) through the resistive voltage divider. The input capacitor C_{IN} couple the AC signal at the input.

The amplifier voltage gain is set by the combination of the input resister R_{IN} and the feedback resistor R_{FB} and is calculated by the equation:

$$AV = \frac{-R_{FB}}{R_{IN}}$$

Where for Channel 1: R_{FB}=R_{FB1} and R_{IN}=R_{IN1} and for Channel 2: R_{FB}=R_{FB2} and R_{IN}=R_{IN2}.

The MP7745 includes four high-power MOSFETs wherein for each channel the output driver stage uses two 250mΩ N-Channel MOSFETs to deliver the pulses to the LC output filter which in turn drives the load. To fully enhance the high-side MOSFET, the gate is driven to a voltage higher than the source by the bootstrap capacitor between SW and BS. While the output is driven low, the bootstrap capacitor is charged from V_{DD} through an internal circuit on the MP7745. The gate of the high-side MOSFET is driven high from the voltage at BS, forcing the MOSFET gate to a voltage higher than V_{DD} and allowing the MOSFET to fully turn on, reducing power loss in the amplifier.

Pop Elimination

The capacitors C_{OUT1} and C_{OUT2} block the DC signal and pass only AC signals to the load. To insure that the amplifier passes low frequency signals, the time constant of C_{OUT}*R_{LOAD} is long. However, when EN is asserted, the capacitor charges over a long period and in a normal amplifier can result in a turn on and/or turn off "pop." The MP7745 includes integrated circuit that eliminate the turn on and turn off pop associated with the charging of the AC coupling capacitor.

Short Circuit/Overload Protection

The MP7745 has internal overload and short circuit protection. The currents in both the high-side and low-side MOSFETs are measured and if the current exceeds the 4.5A short circuit current limit, both MOSFETs are turned off. The MP7745 then restarts with the same power up sequence that is used for normal starting to prevent a pop from occurring after a short circuit condition is removed.

Two schottky diodes (for example, B340 manufactured by Diodes Inc) are required for short-circuit protection, with the cathode connected to SW and the anode connected to PGND. Please place the diode as close to the MP7745 as possible.

If short-circuit protection is not needed, the Schottky diode can be omitted.

Enable Function

The MP7745 EN input is an active high enable control. To enable the MP7745, drive EN with a 2.5V or greater voltage. To disable the amplifier, drive it below 0.8V. While the MP7745 is disabled, the VDD operating current is less than 100μA and the output driver MOSFETs are turned off.

APPLICATION INFORMATION

COMPONENT SELECTION

The MP7745 uses a minimum number of external components to complete a stereo Class D audio amplifier. The circuit of Figure 1 is optimized for a 24V power supply. This circuit should be suitable for most applications. However, if this circuit is not suitable, use the following sections to determine how to customize the amplifier for a particular application.

Setting the Voltage Gain

The maximum output voltage swing is limited by the power supply. To achieve the maximum power out of the MP7745 amplifier, set the gain such that the maximum input signal results in the maximum output voltage swing.

The maximum output voltage swing is $\pm V_{DD}/2$. For a given input signal voltage, where $V_{IN}(pk)$ is the peak input voltage, the maximum voltage gain is:

$$A_V(MAX) = \frac{V_{DD}}{2 \times V_{IN}(pk)}$$

This voltage gain setting results in the peak output voltage approaching it's maximum for the maximum input signal. In some cases the amplifier is allowed to overdrive slightly, allowing the THD to increase at high power levels, and so a higher gain than A_V (max) is required.

Setting the Switching Frequency

The idle switching frequency (the switching frequency when no audio input is present) is a function of several variables: the supply voltage V_{DD}, the timing capacitor C_{INT} and the feedback resistor R_{FB}. Lower switching frequencies result in more inductor ripple, causing more quiescent output voltage ripple and increasing the output noise and distortion. Higher switching frequencies result in more power loss. The optimum idle switching frequency is approximately 600KHz to 700KHz. It is recommended to set right channel idle switching frequency larger than left channel's with 50kHz difference by using different timing capacitor C_{INT}. Refer to the Operating Specifications for recommended values.

Table 1—Switching Frequency vs. V_{DD}, Timing Capacitor and Feedback Resistor (see Figure 1)

V_{DD} (V)	Gain (V/V)	R_{FB} (kΩ)	R_{IN} (kΩ)	Left Channel		Right Channel	
				C_{INT1} (nF)	F_{SW1} (kHz)	C_{INT2} (nF)	F_{SW2} (kHz)
12	5.6	56	10	4.7	560	3.3	700
12	8.2	39	4.7	5.6	620	4.7	700
12	12.0	56.4	4.7	4.7	530	3.3	670
12	17.6	56.4	3.2	4.7	530	3.3	670
12	25.5	56.4	2.2	4.7	530	3.3	670
12	30	60	2	4.7	520	3.3	650
24	5.6	56	10	10	540	8.2	650
24	8.2	82	10	5.6	610	4.7	690
24	12.0	120	10	4.7	530	3.3	660
24	17.4	82	4.7	5.6	610	4.7	690
24	25.5	120	4.7	4.7	530	3.3	660
24	30	120	4	4.7	530	3.3	660

Choosing the LC Filter

The Inductor-Capacitor (LC) filter converts the pulse train at SW to the output voltage that drives the speaker. Typical values for the LC filter are shown in Figure 1, 10μH inductor and 0.47μF capacitor.

The characteristic frequency of the LC filter needs to be high enough to allow high frequency audio to the output, yet needs to be low enough to filter out high frequency products of the pulses from SW. The characteristic frequency of the LC filter is:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

The voltage ripple at the output is approximated by the equation:

$$V_{RIPPLE} \cong V_{DD} \times \left(\frac{f_0}{f_{SW}}\right)$$

The quality factor (Q) of the LC filter is important. If this is too low, output noise will increase, if this is too high, then peaking may occur at high signal frequencies reducing the passband flatness. The circuit Q is set by the load resistance (speaker resistance, typically 4Ω or 8Ω). The Q is calculated as:

$$Q = \frac{R_{LOAD}}{\omega_0 \times L} = \frac{R_{LOAD}}{2\pi \times f_0 \times L}$$

ω_0 is the characteristic frequency in radians per second and f_0 is in Hz. Use an LC filter with Q between 0.7 and 1.

The actual output ripple and noise is greatly affected by the type of inductor and capacitor used in the LC filter. Use a film capacitor and an inductor with sufficient power handling capability to supply the output current to the load. The inductor should exhibit soft saturation characteristics. If the inductor exhibits hard saturation, it should operate well below the saturation current. Gapped ferrite, MPP, Powdered Iron, or similar type toroidal cores are recommended. If open or shielded bobbin ferrite cores are used for multi-channel designs, make sure that the start windings of each inductor line up (all starts going toward SW pin, or all starts going toward the output) to prevent crosstalk or other channel-to-channel interference.

Output Coupling Capacitor

The output AC coupling capacitor C_{OUT} serves to block DC voltages and thus passes only the amplified AC signal from the LC filter to the load. The combination of the coupling capacitor, C_{OUT} and the load resistance results in a first-order high-pass filter. The value of C_{OUT} should be selected such that the required minimum frequency is still allowed to pass. The output corner frequency (-3dB point), f_{OUT}, can be calculated as:

$$f_{OUT} = \frac{1}{2 \times \pi \times R_{LOAD} \times C_{OUT}}$$

Set the output corner frequency (f_{OUT}) at or below the minimum required frequency.

The output coupling capacitor carries the full load current, so a capacitor should be chosen such that its ripple current rating is greater than the maximum load current. Low ESR aluminum electrolytic capacitors are recommended.

Input Coupling Capacitor

The input coupling capacitors C_{IN1} and C_{IN2} are used to pass only the AC signal at the input. In a typical system application, the source input signal is typically centered around the circuit ground, while the MP7745 input is at half the power supply voltage (V_{DD}/2). The input coupling capacitor transmits the AC signal from the source to the MP7745 while blocking the DC voltage. Choose an input coupling capacitor such that the corner frequency (f_{IN}) is less than the passband frequency. The corner frequency is calculated as:

$$f_{IN} = \frac{1}{2 \times \pi \times R_{IN} \times C_{IN}}$$

Power Source

For maximum output power, the amplifier circuit requires a regulated external power source to supply the power to the amplifier. The higher the power supply voltage, the more power can be delivered to a given load resistance, however if the power source voltage exceeds the maximum voltage of 26V, the MP7745 may sustain damage. The power supply rejection of the MP7745 is excellent (typically -59dB), however noise at the power supply can get to the output, so care must be taken to minimize power supply noise within the pass-band frequencies. Bypass the power supply with a large capacitor (typically aluminum electrolytic) along with a smaller 1μF ceramic capacitor at the MP7745 V_{DD} supply pins.

PCB Layout

The circuit layout is critical for optimum performance and low output distortion and noise. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines and take Figure 2 for references.

1) Place the following components as close to the MP7745 as possible:

Bootstrap Cap

C_{BS1} and C_{BS2} are used to supply the gate drive current to the internal high-side MOSFET. Place C_{BS1} as close to pins 17 and 19 as possible. Likewise, place C_{BS2} as close to pins 12 and 14 as possible.

Power Supply Bypass, C_{BYP}

C_{BYP1} and C_{BYP2} carry the transient current for the switching power stage. To prevent overstressing of the MP7745 and excessive noise at the output, place C_{BYP1} as close to pins 18 (VDD1) and 20 (PGND1) as possible and also place C_{BYP2} as close to pins 13 (VDD2) and 15 (PGND2) as possible.

Timing Capacitors

C_{INT1} and C_{INT2} are used to set the amplifier switching frequencies and are typically on the order of a few nF. Place C_{INT1} as close to pins 2 and 3 as possible to reduce distortion and noise. Likewise, place C_{INT2} as close to pins 7 and 8 as possible.

Reference Bypass Capacitors

C_{R1} and C_{R2} filter the ½ V_{DD} reference voltages. Place C_{R1} and C_{R2} as close to the IC as possible to improve power supply rejection and reduce distortion and noise at the output.

2) The Inductor-Capacitor (LC) filter converts the pulse train at SW to the output voltage that drives the speaker. Please keep the filter capacitor close to the inductor.

3) When laying out the PCB, use two separate ground planes, analog ground (AGND) and power ground (PGND), and connect the two grounds together at a single point (usually around the bulk bypass capacitor) to prevent noise injection into the amplifier input to reduce distortion.

4) Keep the sensitive feedback signal trace on the input side and shield the trace with the AGND plane. Make sure that any traces carrying the switch node (SW) voltages are separated far from any input signal traces. If it is required to run the SW trace near the input, shield the input with a ground plane between the traces. For multiple channel applications, make sure that each channel is physically separated to prevent crosstalk. Make sure that all inductors used on a single circuit board have the same orientation.
Also, make sure that the power supply is routed from the source to each channel individually, not serially. This prevents channel-to-channel coupling through the power supply input.

Electro-Magnetic Interference (EMI) Considerations

Due to the switching nature of the Class D amplifier, care must be taken to minimize the effects of electromagnetic interference from the amplifier. However, with proper component selection and careful attention to circuit layout, the effects of the EMI due to the amplifier switching can be minimized.

The power inductors are a potential source of radiated emissions. For the best EMI performance, use toroidal inductors, since the magnetic field is well contained inside the core. However toroidal inductors can be expensive to wind. For a more economical solution, use shielded gapped ferrite or shielded ferrite bobbin core inductors. These inductors typically do not contain the field as well toroidal inductors, but usually can achieve a better balance of good EMI performance with low cost.

The size of high-current loops that carry rapidly changing currents needs to be minimized. To do this, make sure that the V_{DD} bypass capacitors are as close to the MP7745 as possible.

Nodes that carry rapidly changing voltage, such as SW, need to be made as small as possible. If sensitive traces run near a trace connected to SW, place a ground shield between the traces.

TYPICAL APPLICATION CIRCUITS

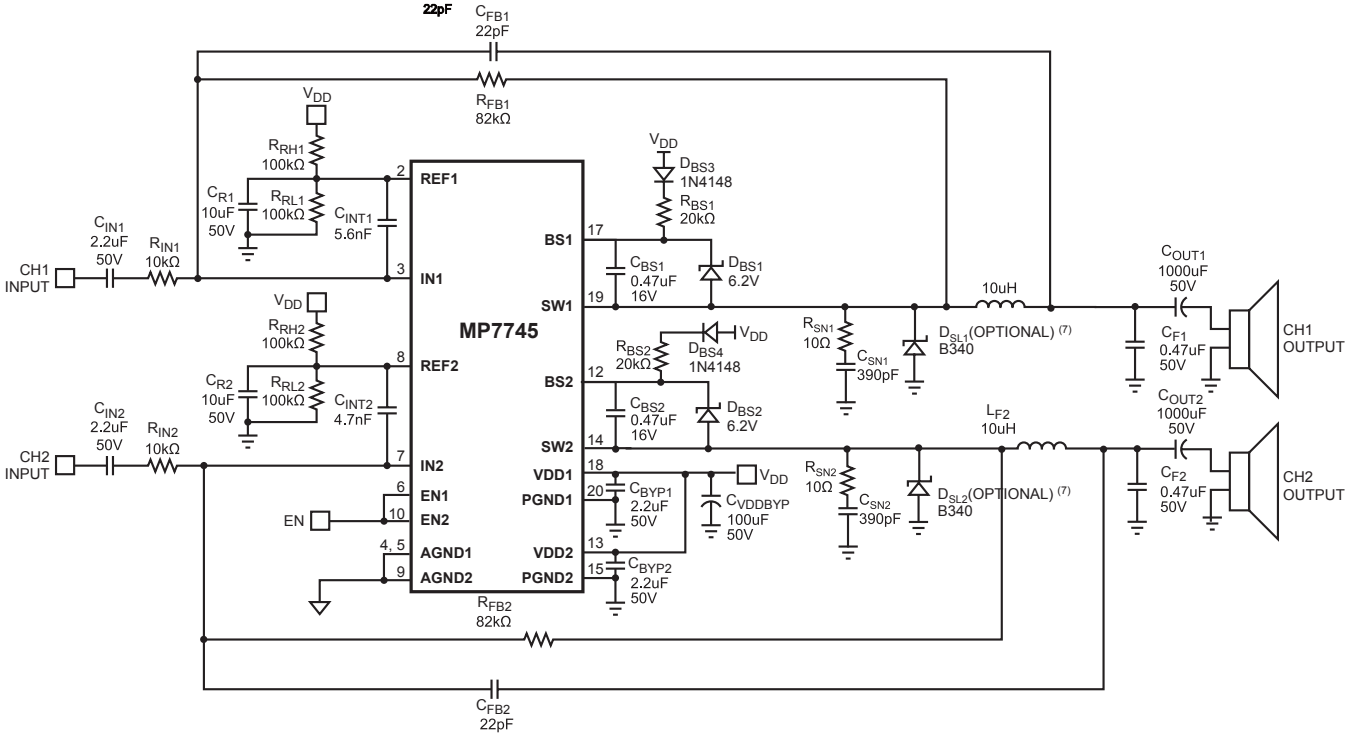
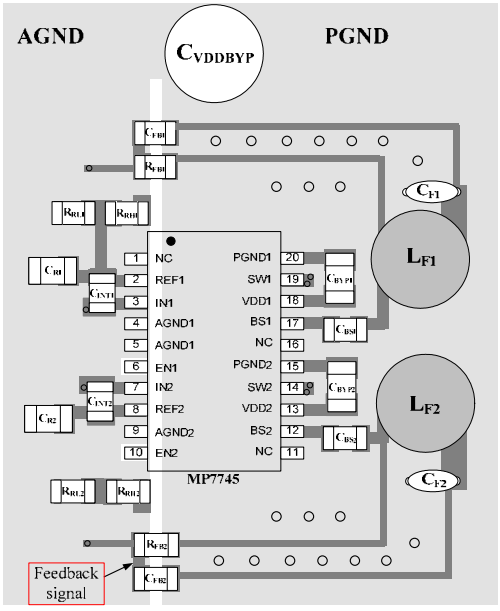
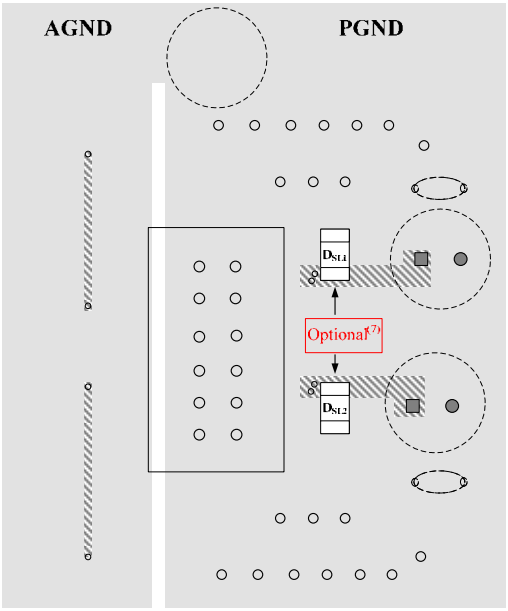


Figure 1—2 x 20W Stereo Typical Application Circuit



a) Top Layer Shown



b) Bottom Layer Shown

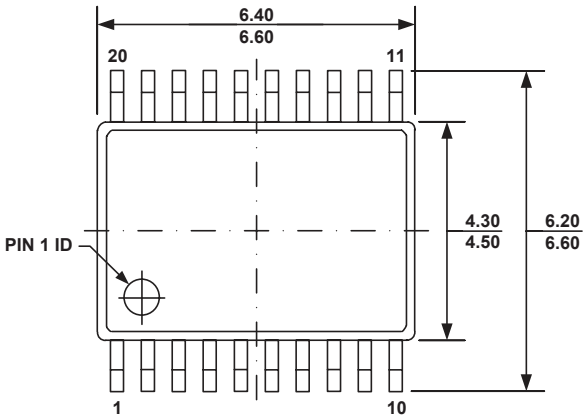
Figure 2—Reference PCB Layout

Note:

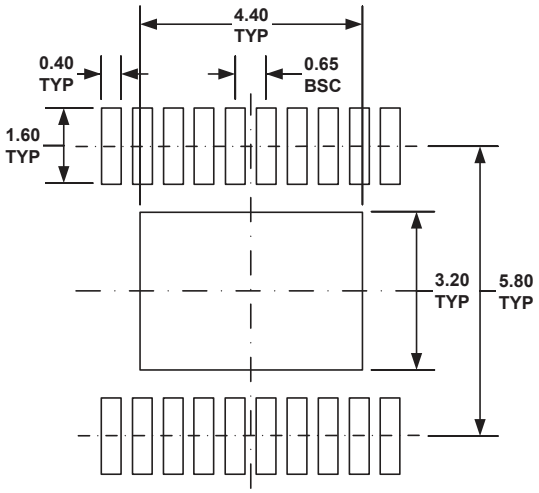
8) Schottky diodes D_{SL1} &D_{SL2} only be required for short circuit protection. Detailed see SHORT CIRCUIT/OVERLOAD PROTECTION section in Operation Information.

PACKAGE INFORMATION

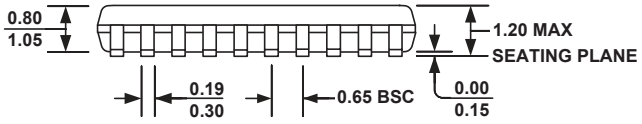
TSSOP20F
(EXPOSED PAD)



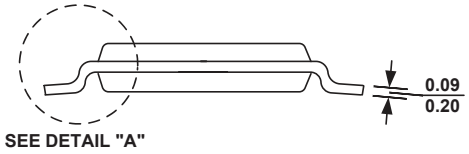
TOP VIEW



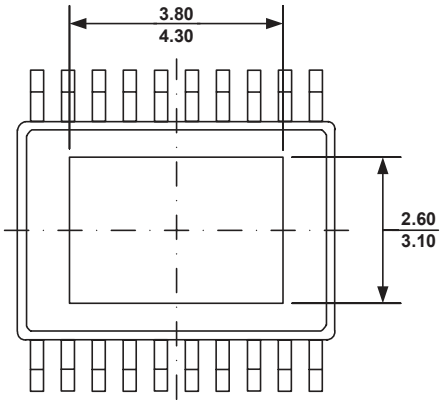
RECOMMENDED LAND PATTERN



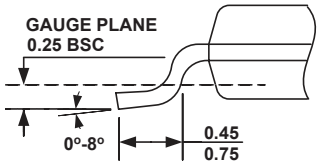
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ACT.
6) DRAWING IS NOT TO SCALE.