

STRUCTURE: Silicon Monolithic integrated circuit

PRODUCT NAME: Servo signal processor for compact disc player

TYPE NAME: **BU9540KV**

FEATURES: The BU9540KV is a servo signal processor complete with built-in pre-servo amplifier and anti-shock memory controller for application to compact disc player.

○ Absolute maximum ratings (Ta=25°C)

Items	Symbol	Ratings	Unit
Power supply voltage	V _{DD}	4.5	V
Power dissipation	P _d	0.9 *1	W
Operating temp. range	T _{opr}	-25 ~ +75	°C
Storage temp. range	T _{stg}	-55 ~ +125	°C

*1 Use of this processor at Ta = 25°C and over is subject to reduction of 9mW per 1°C.

* Operation is not guaranteed.

○ Recommendation Operating range (Ta=-25 ~ +75°C)

Items	Symbol	Ratings	Unit
Power supply voltage	V _{DD}	2.5 ~ 3.3	V

* This product is not designed for protection against radioactive rays.

○ Electrical characteristics (Digital system)

V_{DD}=3.0V (Unless otherwise specified Ta = 25°C)

Items		Symbol	Limit			Unit	Conditions
			MIN	TYP	MAX		
Input voltage	H-level voltage	V _{IH}	2.4	-	-	V	
	L-level voltage	V _{IL}	-	-	0.6	V	
Hysteresis input voltage	H-level voltage	V _{IH}	2.1	-	-	V	
	L-level voltage	V _{IL}	-	-	0.9	V	
Input L current to Pull-up resistor		I _{IL}	-35	-80	-150	μA	V _{IN} =0V
Input current		I _I	-	-	±1	μA	V _{IN} =0~3V
Output voltage	H-level voltage	V _{OH}	2.5	-	-	V	I _O =-0.6mA
	L-level voltage	V _{OL}	-	-	0.4	V	I _O =0.6mA

Status of this document

The Japanese version of this document is the formal specification.

A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document, formal version takes priority.

The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys).

Should you intend to use this product with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.

○ Electrical Characteristics (Analog system 1/2)

 $V_{DD}=3.0V$ (Unless otherwise specified $T_a = 25^{\circ}C$, $R_L=10k\Omega$, standard V_C)

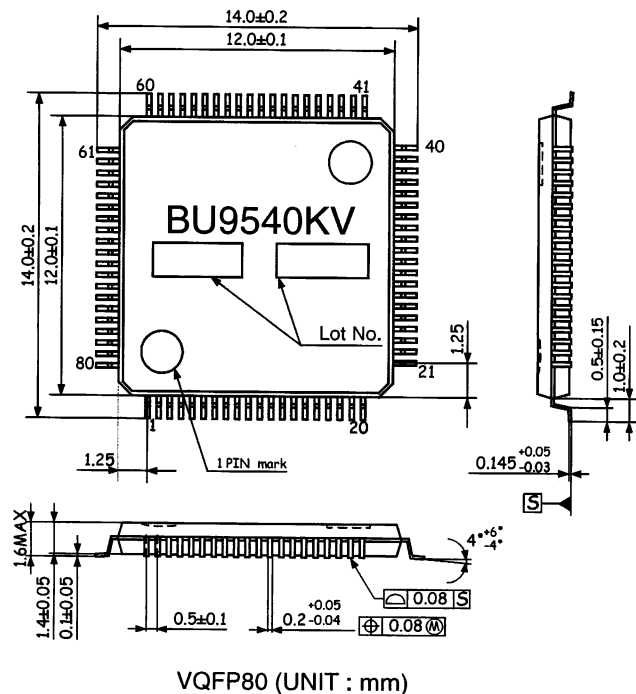
Item	Symbol	Limit			Unit	Applicable pins, conditions
		MIN	TYP	MAX		
Total						
Circuit current	I _Q	-	24	37	mA	AVDD1,AVDD2,DVDD
PLL (VCO)						
Max. oscillation Frequency	f _{VCOH}	4.6	6.5	-	MHz	1/4 of A13 and VCO outputs
Min. oscillation Frequency	f _{VCOL}	-	1.1	1.7	MHz	1/4 of A13 and VCO outputs
FC DAC						
Offset voltage	V _{FCOF}	-50	-	50	mV	FCO
Max. output voltage	V _{FCH}	0.2	0.5	-	V	FCO
Min. output voltage	V _{FCL}	-	-0.5	-0.2	V	FCO
PCO						
L-level output voltage	V _{PCH}	-	-1.0	-0.6	V	PCO
H-level output voltage	V _{PCL}	0.6	1.0	-	V	PCO
Audio DAC						
Distortion rate	THD	-	0.01	-	%	LDACO,RDACO,0dB 1kHz sine
Dynamic range	DR	-	90	-	dB	LDACO,RDACO,-60dB 1kHz sine
S/N ratio	S/N	-	96	-	dB	LDACO,RDACO
Max. output level	V _{SMAX}	0.75	0.85	0.95	V _{rms}	LDACO,RDACO,0dB 1kHz sine
EFM comparator						
Threshold level	V _{EFM}	-200	-	200	mV	RFI,ANA_MONI0,A12
Servo ADC						
Offset voltage	V _{ADOF}	-140	-	140	mV	SD_IN,ANA_MONI0,ANA_MONI1
Max. conversion level	V _{ADH}	1.0	1.2	1.4	V	SD_IN,ANA_MONI0,ANA_MONI1
Min. conversion level	V _{ADL}	-1.4	-1.2	-1.0	V	SD_IN,ANA_MONI0,ANA_MONI1
Servo DAC						
Offset voltage	V _{DAOF}	-80	-	80	mV	FDOUT,TDOUT,SDOUT,CLVOUT
Max. output voltage	V _{DAH}	0.8	1.2	-	V	FDOUT,TDOUT,SDOUT,CLVOUT
Min. output voltage	V _{DAL}	-	-1.2	-0.8	V	FDOUT,TDOUT,SDOUT,CLVOUT
Bias amplifier						
Max. output current	I _{BO}	-	±1.5	-	mA	VBIAS and BIAS fluctuation to be 200mV MAX.
RF amplifier						
Offset voltage	V _{RFOF}	-	0	-	mV	AC,BD,EQO
Max. output voltage	V _{RFH}	1.0	1.2	-	V	AC,BD,EQO
Min. output voltage	V _{RFL}	-	-1.3	-1.1	V	AC,BD,EQO

○ Electrical Characteristics (Analog system 2/2)

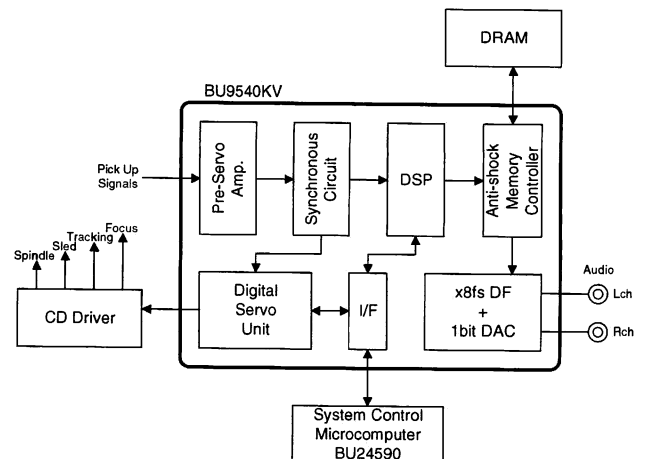
$V_{DD}=3.0V$ (Unless otherwise specified $T_a = 25^{\circ}C$, $R_L=10k\Omega$, standard V_C)

Item	Symbol	Limit			Unit	Applicable pins, conditions
		MIN	TYP	MAX		
FE amplifier						
Offset voltage	V _{FEOF}	-	0	-	mV	AC,BD,ANA_MONI0,ANA_MONI1
Max. output voltage	V _{FEH}	1.0	1.4	-	V	AC,BD,ANA_MONI0,ANA_MONI1
Min. output voltage	V _{FEL}	-	-1.4	-1.0	V	AC,BD,ANA_MONI0,ANA_MONI1
TE amplifier						
Offset voltage	V _{TEOF}	-	70	-	mV	E,F,ANA_MONI0,ANA_MONI1
Max. output voltage	V _{TEH}	1.0	1.4	-	V	E,F,ANA_MONI0,ANA_MONI1
Min. output voltage	V _{TEL}	-	-1.4	-1.0	V	E,F,ANA_MONI0,ANA_MONI1
Asymmetric amplifier						
Offset voltage	V _{ASYOF}	-	0	-	mV	ASY=V _C ,RFI,ANA_MONI0(ASY_TEST)
Max. output voltage	V _{ASYH}	1.1	1.4	-	V	ASY,RFI,ANA_MONI0(ASY_TEST)
Min. output voltage	V _{ASYL}	-	-1.4	-1.1	V	ASY,RFI,ANA_MONI0(ASY_TEST)
APC						
Output voltage1	V _{APC1}	2.4	2.8	-	V	PD="H",LD,ANA_MONI0(APCREF)
Output voltage2	V _{APC2}	-	0.1	0.5	V	PD="L",LD,ANA_MONI0(APCREF)
Max. reference voltage	V _{APCH}	-	195	-	mV	PD,LD,ANA_MONI0(APCREF)
Min. reference voltage	V _{APCL}	-	126	-	mV	PD,LD,ANA_MONI0(APCREF)

○ Package Outline, Appearance marking diagram



○ Block diagram



O Description of Terminal

No.	Name	Description of terminals
1	AVDD1	Analog power supply
2	AC	A + C voltage input
3	BD	B + D voltage input
4	VBIAS	Bias level (VDD/2)
5	AC_GAIN	LPF of FE amplifier (AC gain)
6	BD_GAIN	LPF of FE amplifier (BD gain)
7	E	E voltage input
8	F	F voltage input
9	PD	Photo detector input
10	LD	Laser drive output
11	ASY	Asymmetric correction
12	PCO	PCO output
13	FCO	FCO-DAC output
14	AGND1	Analog GND
15	FDOUT	Focus drive output
16	TDOUT	Tracking drive output
17	SDIN	Sled drive input
18	SDOUT	Sled drive output
19	CLVOUT	CLV drive output
20	CLK88	Clock output for driver IC
21	CLK	Output for various clocks
22	SUBSYQ	Sub code synchronous signal
23	MCK	Command transfer clock input
24	DIN/DOUT	Command data input/output
25	R/W	Command read/write signal
26	RESETX	"L" → reset condition
27	BUSY	Busy signal output
28	RCLK	Reference clock output
29	RCKE	Clock enable output
30	A13	Address output
31	A12	Address output
32	A11	Address output
33	A10	Address output
34	A09	Address output
35	A08	Address output
36	A07	Address output
37	A06	Address output
38	A05	Address output
39	A04	Address output
40	A03	Address output

No.	Name	Description of terminals
41	A02	Address output
42	A01	Address output
43	A00	Address output
44	RASX	Row address strobe signal
45	CASX	Column address strobe signal
46	WEX	Write enable output
47	DQ07	Data input/output
48	DQ06	Data input/output
49	DQ05	Data input/output
50	DQ04	Data input/output
51	DQ03	Data input/output
52	DQ02	Data input/output
53	DQ01	Data input/output
54	DQ00	Data input/output
55	DQ15	Data input/output
56	DQ14	Data input/output
57	DQ13	Data input/output
58	DQ12	Data input/output
59	DQ11	Data input/output
60	DQ10	Data input/output
61	DQ09	Data input/output
62	DQ08	Data input/output
63	C2FX	Flag of C2 output
64	YFLAG	Writing stop signal for DRAM
65	DVDD	Digital power supply
66	XI	X'tal connecting (input) terminal
67	XO	X'tal connecting terminal
68	DGND	Digital GND
69	AVDD2	Audio analog power supply
70	LDACO	Audio Lch output
71	VCDAC	Audio reference voltage
72	RDACO	Audio Rch output
73	AGND2	Audio system analog GND
74	AD_MONI0	Monitor signal output
75	AD_MONI1	Monitor signal output
76	TEST	Test signal input
77	ANA_MONI0	Analog monitor signal output
78	ANA_MONI1	Analog monitor signal output
79	RFI	RF data re-input terminal
80	EQO	After-RF-equalizer output

O Cautions

(1) ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur and break mode (open or short) can not be specified if power supply, operating temperature, and those of ABSOLUTE MAXIMUM RATINGS are exceeded. If such a special condition is expected, components for safety such as fuse must be used.

(2) Power Supply

Power and Ground line must be designed as low impedance in the PCB. Print patterns if digital power supply and analog power supply must be separated even if these have same voltage level. Print patterns for ground must be designed as same as power supply. These considerations avoid analog circuits from the digital circuit noise. All pair of power supply and ground must have their own de-coupling capacitor. Those capacitor should be checked about their specification, etc. (nominal electrolytic capacitor degrades its capacity at low temperature) and choose the constant of an electrolytic capacitor.

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