April 2004

National Semiconductor

LM2743
N-Channel FET Synchronous Buck Regulator Controller for Conversion from 3.3V

General Description

The LM2743 is a high-speed, N-Channel synchronous buck regulator controller with a 2%, 0.6V feedback reference voltage intended to make down conversion from 3.3V to as low as 0.6V easy. A fixed-frequency voltage-mode PWM control architecture is used, that is adjustable from 50kHz to 2MHz through an external resistor. This wide range of PWM frequencies gives the power supply designer the flexibility to make tradeoffs among component size, cost, noise and efficiency. The power MOSFETs can run on a separate 1V to 16V (Input Voltage, V_{IN}) (Note 2) rail while the regulator is biased from a 3V to 6V (IC Input Voltage, V_{CC}), 2mA rail. A power-good flag, precision shutdown threshold and soft start features make power supply tracking and sequencing easy. The LM2743 employs output under-voltage and over-voltage flag, and current limit. Current limit is achieved by monitoring the voltage drop across the on resistance of the low-side MOSFET. The adaptive non-overlapping MOSFET gate drivers help avoid potential shoot-through problems while maintaining high efficiency. Both high-side and low-side MOSFETs are the lower cost N-Channel type, and the IC can accept a bootstrap structure to saturate the high-side MOSFET for highest efficiency.

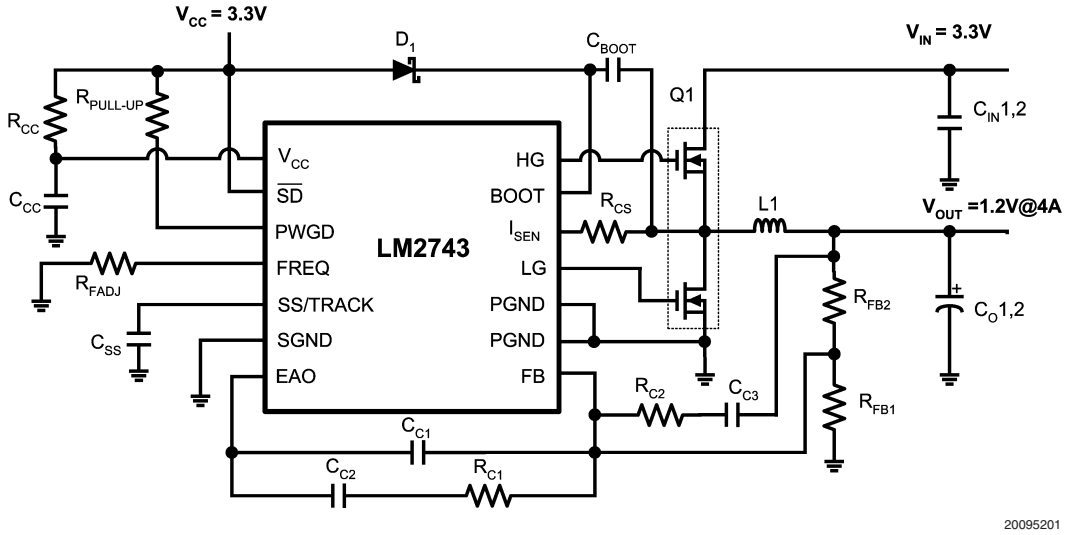
Features

- MOSFET input voltage (V_{IN}) from 1V to 16V (Note 2)
- IC input voltage (V_{CC}) from 3V to 6V
- Output voltage adjustable down to 0.6V
- Power good flag and output enable
- Output over-voltage and under-voltage flag
- FB voltage: 2% over temperature
- Current limit without series sense resistor
- Adjustable soft start
- Tracking and sequencing with shutdown and soft start pins
- Switching frequency from 50 kHz to 2 MHz
- TSSOP-14 package

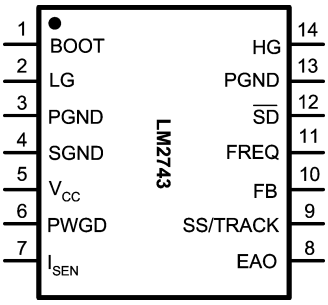
Applications

- 3.3V Buck Regulation
- Set-Top Boxes/ Home Gateways
- Core Logic Regulators
- High-Efficiency Buck Regulation

Typical Application



Connection Diagram



20095202

14-Lead Plastic TSSOP
θ_{JA} = 155˚C/W
NS Package Number MTC14

Pin Description

BOOT (Pin 1) - Supply rail for the N-channel MOSFET gate drive. The voltage should be at least one gate threshold ($V_{GS(th)}$) above the regulator input voltage (V_{IN}) to properly turn on the high-side FET.

LG (Pin 2) - Gate drive for the low-side N-channel MOSFET. This signal is interlocked with HG (Pin 14) to avoid a shoot-through problem.

PGND (Pins 3, 13) - Ground for low-side FET drive circuitry. Connect to system ground.

SGND (Pin 4) - Ground for signal level circuitry. Connect to system ground.

V_{CC} (Pin 5) Supply rail for the controller.

PWGD (Pin 6) - Power good pin. This is an open drain output. The pin is pulled low when the chip is in under-voltage flag (UVF), over-voltage flag (OVF), or UVLO mode. During normal operation, this pin is connected to V_{CC} or other low voltage source through a pull-up resistor ($R_{PULL-UP}$).

I_{SEN} (Pin 7) - Current limit threshold setting. This sources a fixed 40µA current. A resistor of appropriate value should be connected between this pin and the drain of the low-side FET.

EAO (Pin 8) - Output of the error amplifier. The voltage level on this pin is compared with an internally generated ramp signal to determine the duty cycle. This pin is necessary for compensating the control loop.

SS (Pin 9) - Soft start and track pin. A 10 µA current is sourced from this pin. This pin is connected to the non-inverting input of the error amplifier during soft start, or any time the voltage is below the reference. To track power supplies connect a resistor divider (smaller than 10kΩ for better precision) from the output of the master supply directly to the SS pin. To limit the inrush current of a single power supply, place a capacitor to ground (see Application Information/Start Up for appropriate capacitance value). This pin should not be forced before $\overline{SD}$ or V_{CC} (above the UVLO).

FB (Pin 10) - This is the inverting input of the error amplifier, which is used for sensing the output voltage and compensating the control loop. The FB current is negligible.

FREQ (Pin 11) - The switching frequency (F_{OSC}) is set by connecting a resistor (R_{FADJ}) between this pin and ground.

$\overline{SD}$ (Pin 12) - IC shutdown pin. To assure proper IC start-up the $\overline{SD}$ pin should not be left floating. When this pin is pulled low the chip turns both, high and low, sides off. While this pin is low, the IC will not start up. This pin features a precision threshold for power supply sequencing, as well as a lower threshold to ensure minimal quiescent current.

HG (Pin 14) - Gate drive for the high-side N-channel MOSFET. This signal is interlocked with LG (Pin 2) to avoid a shoot-through problem.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC}	7V
BOOT Voltage	21V
All other pins	V_{CC} + 0.3V
Junction Temperature	150˚C
Storage Temperature	–65˚C to 150˚C
Soldering Information	
Lead Temperature (soldering, 10sec)	260˚C
Infrared or Convection (20sec)	235˚C
ESD Rating (Note 3)	2 kV

Operating Ratings

IC Input Voltage (V_{CC})	3V to 6V
Junction Temperature Range	–40˚C to +125˚C
Thermal Resistance (θ_{JA})	155˚C/W

Electrical Characteristics

V_{CC} = 3.3V unless otherwise indicated. Typicals and limits appearing in plain type apply for T_A= T_J= +25˚C. Limits appearing in boldface type apply over full Operating Temperature Range. Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{FB}	FB Pin Voltage	V_{CC} = 3.3V	**0.612**	0.6	**0.588**	V
		V_{CC} = 5V	**0.612**	0.6	**0.588**	
V_{ON}	UVLO Thresholds	Rising Falling		2.76 2.42		V
I_{Q_VCC}	Operating V_{CC} Current	V_{CC} = 3.3V, SD = 3.3V Fsw = 600kHz	**1**	1.5	**2.1**	mA
		V_{CC} = 5V, SD = 3.3V Fsw = 600kHz	**1**	1.7	**2.1**	
	Shutdown V_{CC} Current (Note 4)	V_{CC} = 3.3V, SD = 0V	0	110	185	µA
t_{PWGD1}	PWGD Pin Response Time	FB Voltage Going Up		6		µs
t_{PWGD2}	PWGD Pin Response Time	FB Voltage Going Down		6		µs
I_{SS-ON}	SS Pin Source Current	SS Voltage = 0V	**7**	10	**14**	µA
I_{SS-OC}	SS Pin Sink Current During Over Current	SS Voltage = 0V		90		µA
I_{SEN-TH}	I_{SEN} Pin Source Current Trip Point		**25**	40	**55**	µA
ERROR AMPLIFIER						
GBW	Error Amplifier Unity Gain Bandwidth			9		MHz
G	Error Amplifier DC Gain			106		dB
SR	Error Amplifier Slew Rate			3.2		V/µs
I_{EAO}	EAO Pin Current Sourcing and Sinking Capability	V_{EAO} = 1.5, FB = 0.55V V_{EAO} = 1.5, FB = 0.65V		2.6 9.2		mA
V_{EA}	Error Amplifier Maximum Swing	Minimum Maximum		0 2		V

Electrical Characteristics (Continued)

V_{CC} = 3.3V unless otherwise indicated. Typicals and limits appearing in plain type apply for $T_A = T_J = +25^{\circ}C$. Limits appearing in boldface type apply over full Operating Temperature Range. Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
GATE DRIVE						
$I_{Q\text{-}BOOT}$	BOOT Pin Quiescent Current	BOOTV = 12V, EN = 0		18	**90**	µA
R_{DS1}	Top FET Driver Pull-Up ON resistance	BOOT-SW = 5V@350mA		3		Ω
R_{DS2}	Top FET Driver Pull-Down ON resistance			2		Ω
R_{DS3}	Bottom FET Driver Pull-Up ON resistance			3		Ω
R_{DS4}	Bottom FET Driver Pull-Down ON resistance			2		Ω
OSCILLATOR						
F_{OSC}	PWM Frequency	R_{FADJ} = 813.2kΩ		50		kHz
		R_{FADJ} = 117.6kΩ		300		
		R_{FADJ} = 54.4kΩ	**475**	600	**725**	
		R_{FADJ} = 18.8kΩ		1400		
		R_{FADJ} = 10.8kΩ		2000		
D	Max Duty Cycle	f_{PWM} = 300kHz f_{PWM} = 600kHz		90 85		%
LOGIC INPUTS AND OUTPUTS						
$V_{STBY\text{-}IH}$	Standby High Trip Point	FB = 0.575V, BOOTV = 3.3V, EN = 0V to 3.3V		0.756	**1.1**	V
$V_{STBY\text{-}IL}$	Standby Low Trip Point	FB = 0.575V, BOOTV = 3.3V, EN = 3.3V to 0V	**0.232**	0.562		V
$V_{\overline{SD}\text{-}IH}$	$\overline{SD}$ Pin Logic High Trip Point	FB = 0.575V, BOOTV = 3.3V, EN = 0V to 3.3V		1	**1.3**	V
$V_{\overline{SD}\text{-}IL}$	$\overline{SD}$ Pin Logic Low Trip Point	FB = 0.575V, BOOTV = 3.3V, EN = 3.3V to 0V	**0.8**	1.1		V
$V_{PWGD\text{-}TH\text{-}LO}$	PWGD Pin Trip Points	FB Voltage Going Down	**0.408**	0.434	**0.457**	V
$V_{PWGD\text{-}TH\text{-}HI}$	PWGD Pin Trip Points	FB Voltage Going Up	**0.677**	0.710	**0.742**	V
$V_{PWGD\text{-}HYS}$	PWGD Hysteresis	FB Voltage Going Down FB Voltage Going Up		60 90		mV

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. **Operating ratings** indicate conditions for which the device operates correctly. **Opearting Ratings** do not imply guaranteed performance limits.

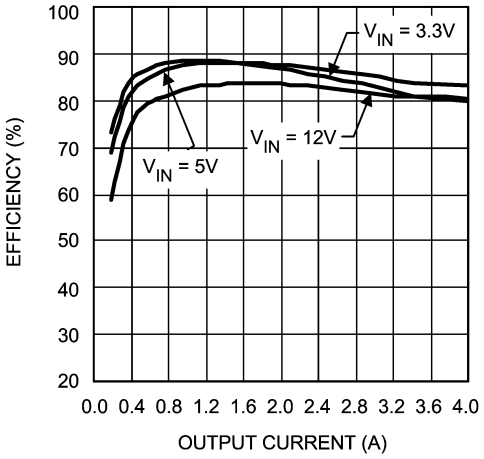
Note 2: The power MOSFETs can run on a separate 1V to 16V rail (Input voltage, V_{IN}). Low range of V_{IN} greatly depends on selection of the external MOSFET.

Note 3: The human body model is a 100pF capacitor discharged through a 1.5k resistor into each pin.

Note 4: Shutdown V_{CC} current goes to zero amps after 20 seconds.

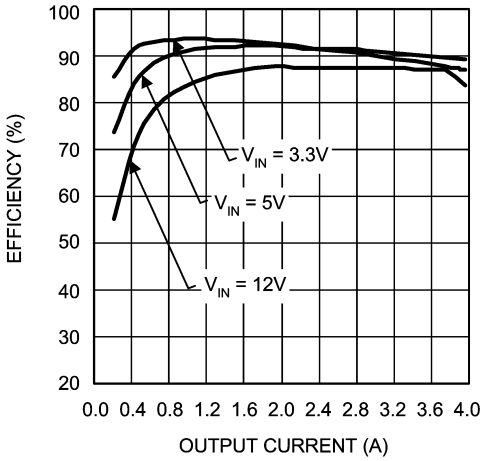
Typical Performance Characteristics

Efficiency (V_{OUT} = 1.2V)
V_{CC} = 3.3V, F_{SW} = 300kHz



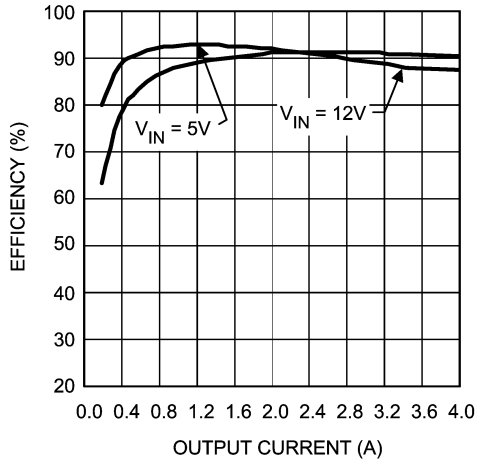
20095240

Efficiency (V_{OUT} = 2.5V)
V_{CC} = 3.3V, F_{SW} = 300kHz



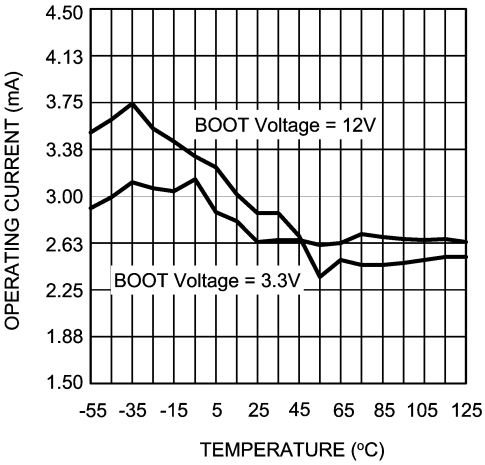
20095257

Efficiency (V_{OUT} = 3.3V)
V_{CC} = 5V, F_{SW} = 300kHz



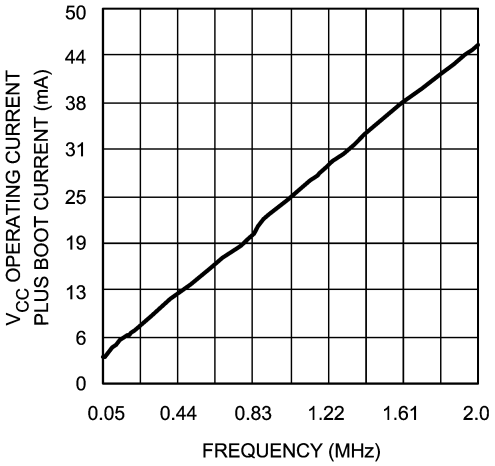
20095241

V_{CC} Operating Current vs Temperature



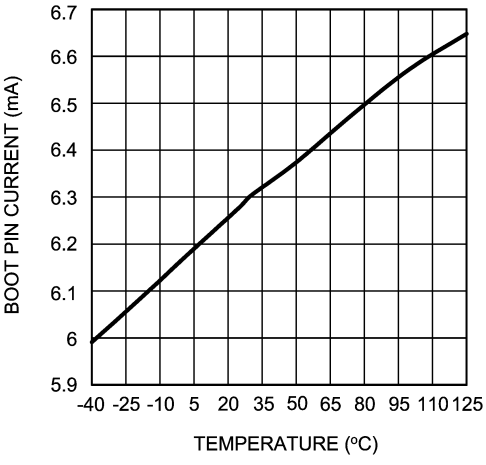
20095261

V_{CC} Operating Current plus BOOT Current vs Frequency
FDS689A FET (T_A = 25˚C)



20095245

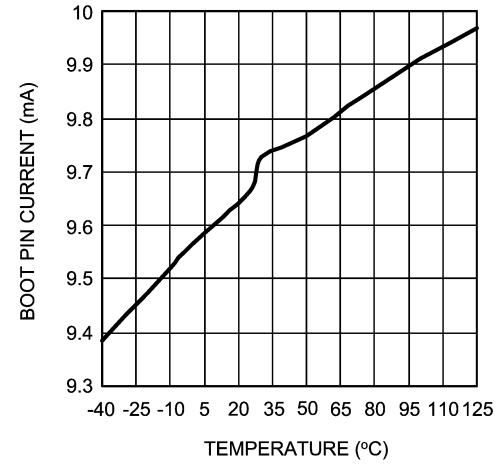
BOOT Pin Current vs Temperature for
BOOT Voltage = 3.3V
F_{SW} = 300kHz, FDS689A FET, No-Load



20095242

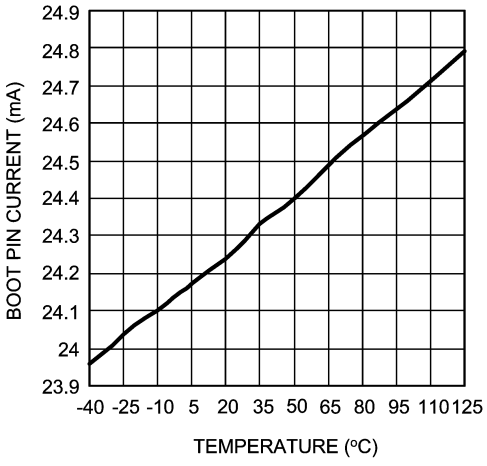
Typical Performance Characteristics (Continued)

BOOT Pin Current vs Temperature for BOOT Voltage = 5V F_{SW} = 300kHz, FDS689A FET, No-Load



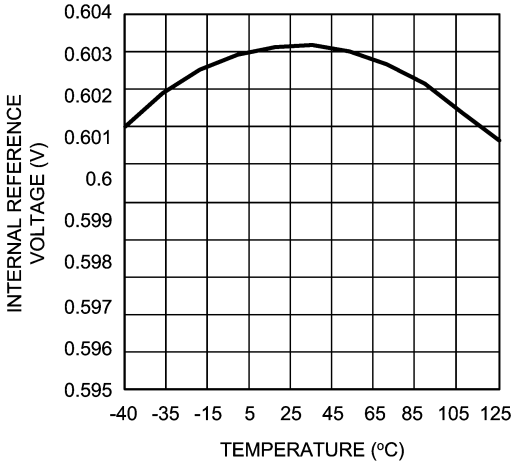
20095243

BOOT Pin Current vs Temperature for BOOT Voltage = 12V F_{SW} = 300kHz, FDS689A FET, No-Load



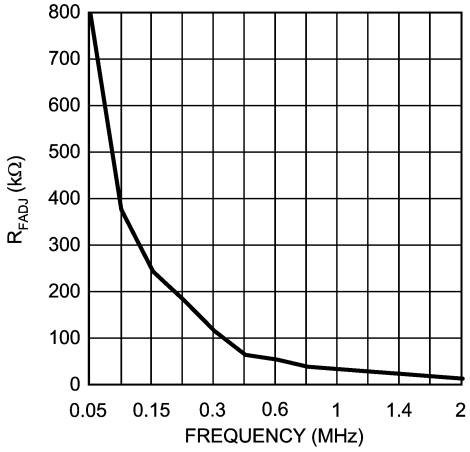
20095244

Internal Reference Voltage vs Temperature



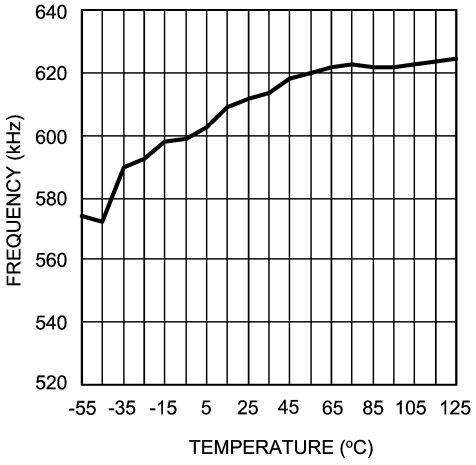
20095258

R_{FADJ} vs Frequency 50kHz to 2MHz, T_A = 25˚C



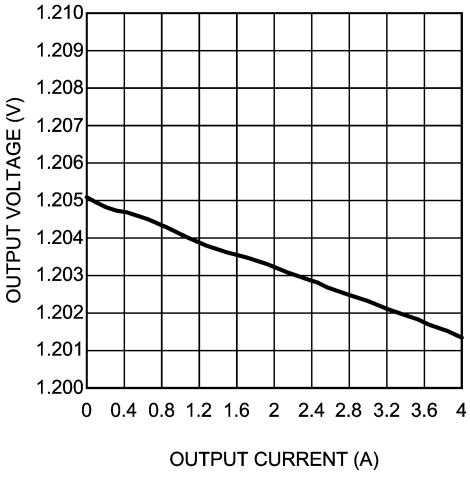
20095259

Frequency vs Temperature



20095260

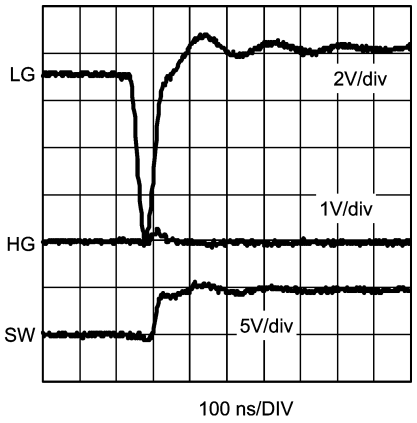
Output Voltage vs Output Current



20095256

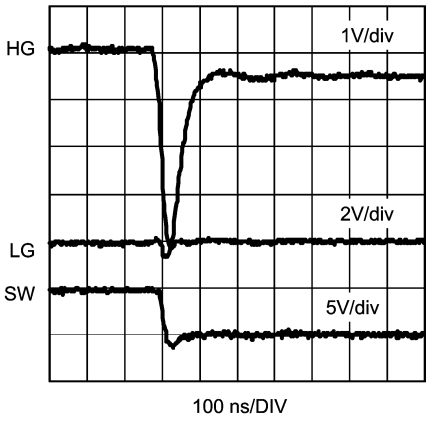
Typical Performance Characteristics (Continued)

Switch Waveforms (HG Rising)
V_{CC} = 3.3V, V_{IN} = 5V, V_{OUT} = 1.2V
I_{OUT} = 4A, C_{SS} = 12nF, F_{SW} = 300kHz



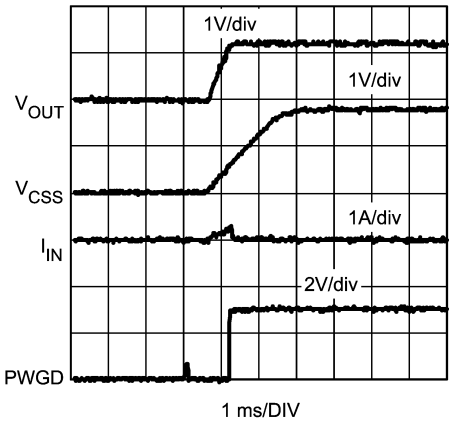
20095246

Switch Waveforms (HG Falling)
V_{CC} = 3.3V, V_{IN} = 5V, V_{OUT} = 1.2V
I_{OUT} = 4A, C_{SS} = 12nF, F_{SW} = 300kHz



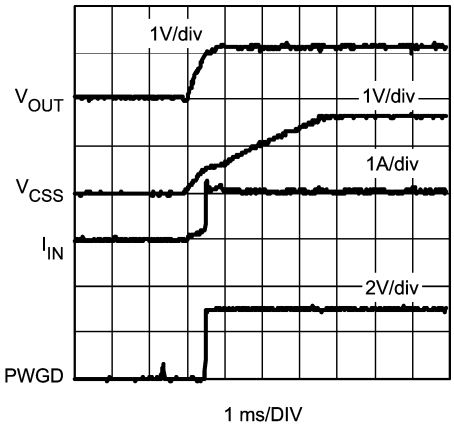
20095247

Start-Up (No-Load)
V_{CC} = 3.3V, V_{IN} = 5V, V_{OUT} = 1.2V
I_{OUT} = 4A, C_{SS} = 12nF, F_{SW} = 300kHz



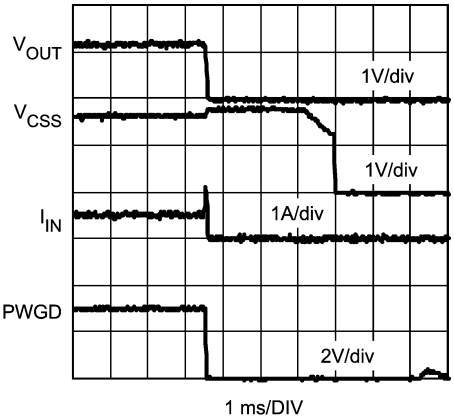
20095248

Start-Up (Full-Load)
V_{CC} = 3.3V, V_{IN} = 5V, V_{OUT} = 1.2V
I_{OUT} = 4A, C_{SS} = 12nF, F_{SW} = 300kHz



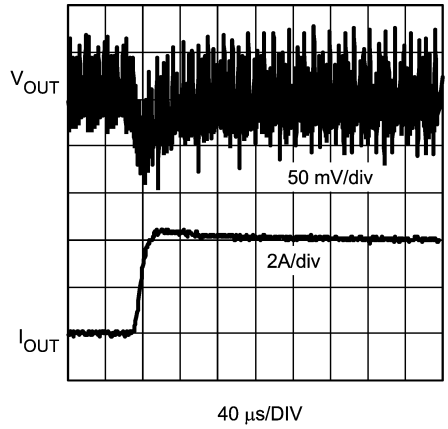
20095249

Shutdown (Full-Load)
V_{CC} = 3.3V, V_{IN} = 5V, V_{OUT} = 1.2V
I_{OUT} = 4A, C_{SS} = 12nF, F_{SW} = 300kHz



20095250

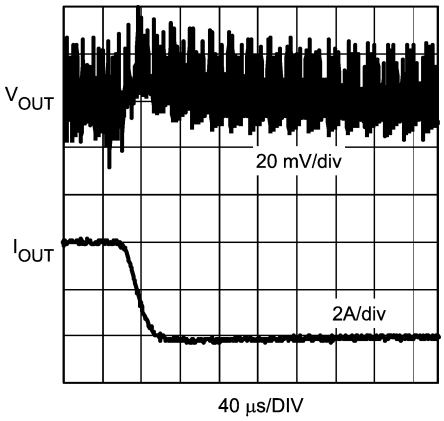
Load Transient Response (I_{OUT} = 0A to 4A)
V_{CC} = 3.3V, V_{IN} = 5V, V_{OUT} = 1.2V
C_{SS} = 12nF, F_{SW} = 300kHz



20095251

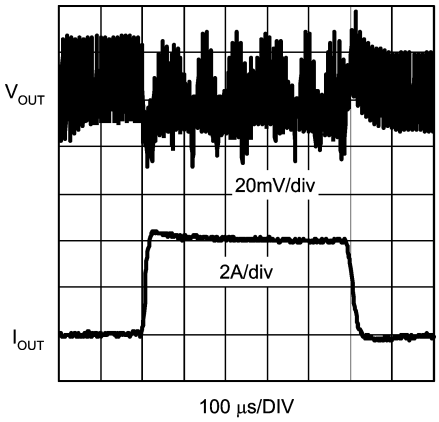
Typical Performance Characteristics (Continued)

Load Transient Response (I_{OUT} = 4A to 0A)
V_{CC} = 3.3V, V_{IN} = 5V, V_{OUT} = 1.2V
C_{SS} = 12nF, F_{SW} = 300kHz



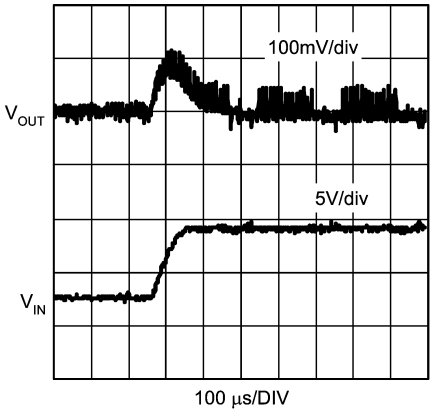
20095252

Load Transient Response
V_{CC} = 3.3V, V_{IN} = 5V, V_{OUT} = 1.2V
C_{SS} = 12nF, F_{SW} = 300kHz



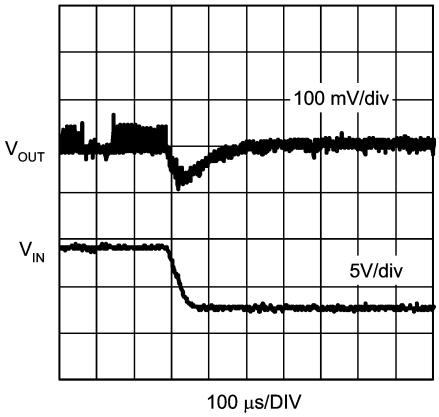
20095253

Line Transient Response (V_{IN} = 3V to 6V)
V_{CC} = 3.3V, V_{OUT} = 1.2V
I_{OUT} = 2A, F_{SW} = 300kHz



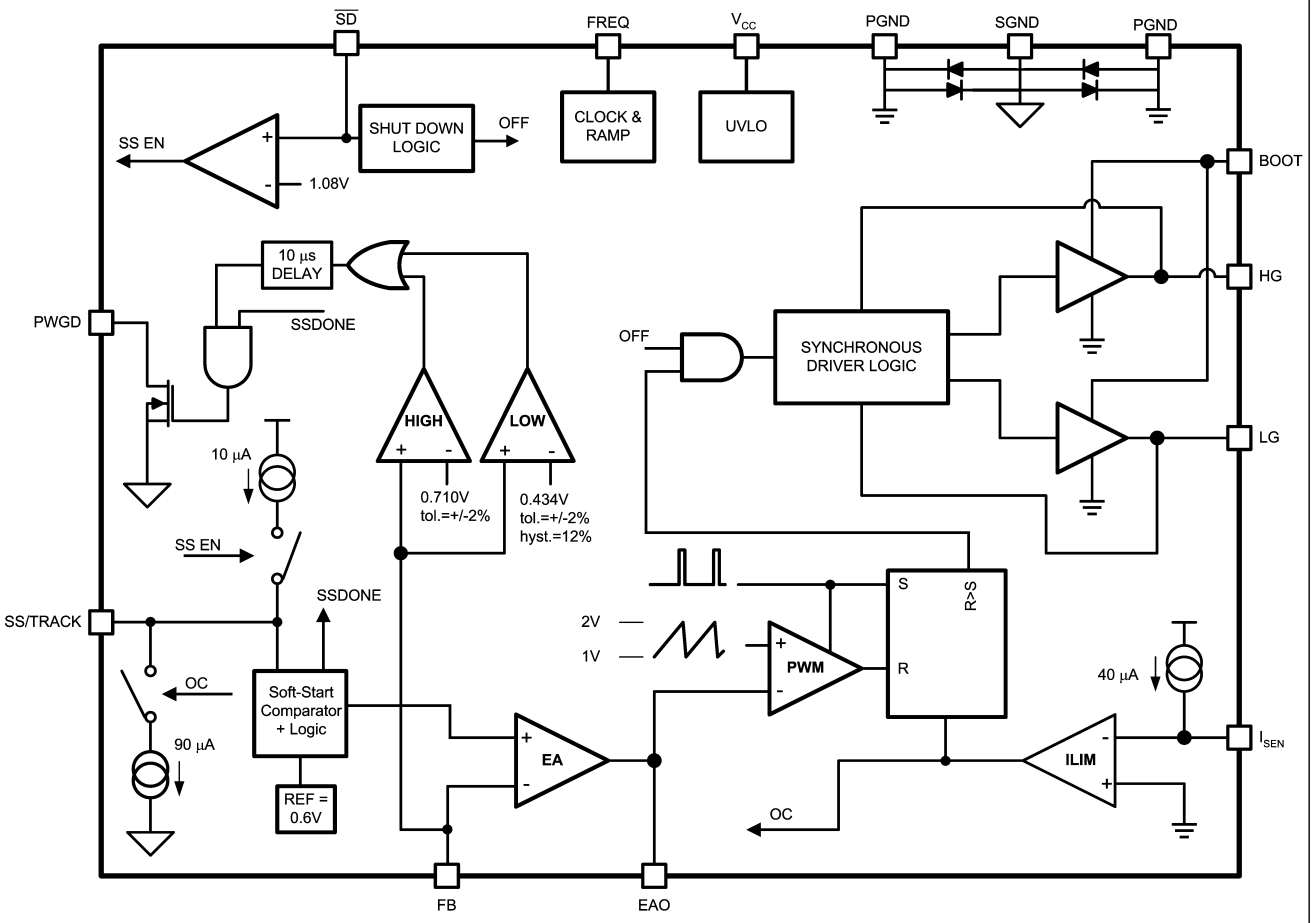
20095254

Line Transient Response (V_{IN} = 6V to 3V)
V_{CC} = 3.3V, V_{OUT} = 1.2V
I_{OUT} = 2A, F_{SW} = 300kHz



20095255

Block Diagram



20095203

Application Information

THEORY OF OPERATION

The LM2743 is a voltage-mode, high-speed synchronous buck regulator with a PWM control scheme. It is designed for use in set-top boxes, thin clients, DSL/Cable modems, and other applications that require high efficiency buck converters. It has power good (PWGD) flag, output shutdown ($\overline{SD}$), UVLO mode, and over-voltage flag (OVF) and under- voltage flag (UVF) features. The over-voltage and under-voltage signals are OR gated to drive the power good signal. If this signal is pulled low, the high side is off and low side if on, but only if the duty cycle is less then maximum. Current limit is achieved by sensing the voltage V_{DS} across the low side FET. During current limit the high side gate is turned off and the low side gate is turned on. A 90µA source discharges the soft start capacitor (reducing max. duty cycle) until the current is under control.

START UP

When V_{CC} exceeds 2.76V and the shutdown pin ($\overline{SD}$) sees a logic high, the internal fixed 10µA source begins charging the soft start capacitor. During this time the output of the error amplifier is allowed to rise with the voltage of the soft start capacitor. This capacitor, C_{SS}, determines soft start time, and can be calculated approximately by:

$$C_{SS} = \frac{t_{SS}}{4 \times 10^4}$$

During soft start the power good flag is forced low and it is released when the voltage reaches a set value as shown in *Figure 1*. At this point the chip enters normal operation mode, the power good flag is released, and the OVF and UVF functions begin to monitor V_{OUT}.

Application Information (Continued)

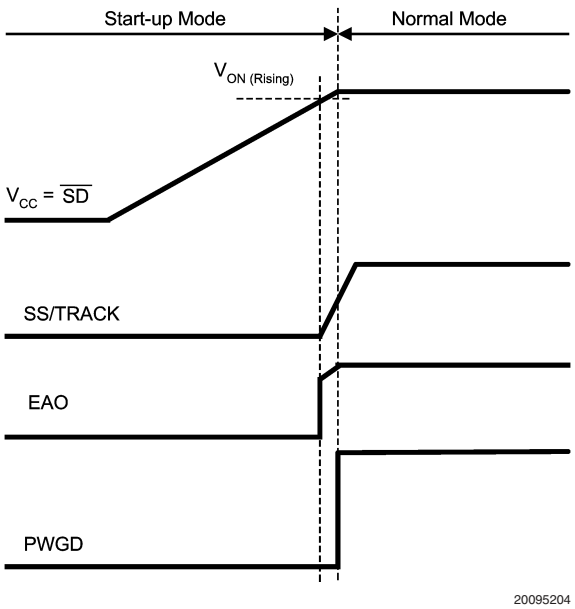


FIGURE 1. Start-Up Behavior

NORMAL OPERATION

While in normal operation mode, the LM2743 regulates the output voltage by controlling the duty cycle of the high side and low side FETs.

The equation governing output voltage is:

$$0.6 = \frac{R_{FB1}}{R_{FB1} + R_{FB2}} V_{OUT}$$

The PWM frequency is adjustable between 50kHz and 2MHz and is set by an external resistor, R_{FADJ}, between the FREQ pin and ground. The resistance needed for a desired frequency is approximately:

$$R_{FADJ} = 10^{12} a_2 \left(\frac{1}{F_{OSC}(Hz)}\right)^2 + 10^7 a_1 \left(\frac{1}{F_{OSC}(Hz)}\right) + 10^2 a_0 \ [k\Omega]$$

where a_2 = 0.206375, a_1 = 3.691525, a_0 = (-0.076875) are the coefficients, F_{OSC} is the frequency in Hz, and R_{FADJ} is the resistance in kΩ.

SS/TRACK

When the LM2743 is used for sequencing purposes, some care has to be taken. Once the shutdown voltage goes above $V_{STBY-IH}$, a 17µA pull-up current is activated as shown in *Figure 2*. This current is used to create an internal hysteresis (170mV); however, high external impedances will affect the $\overline{SD}$ pin level as well. The external impedance must be lower than 10kΩ to work properly without glitching the quiescent current of the chip. In that scenario the SS current will turn on and off during the glitching or most likely no switching will occur at all, due to the SS voltage being very low.

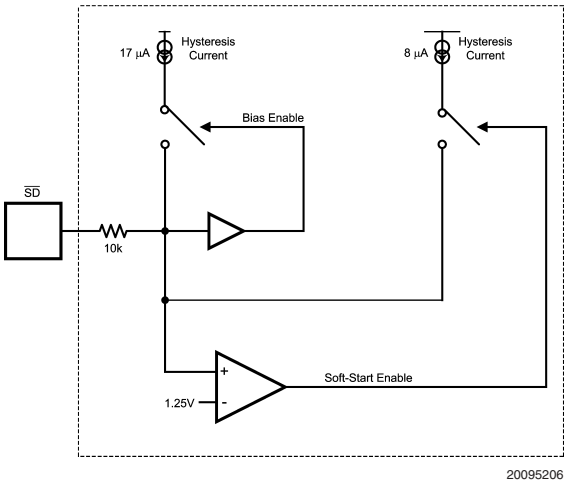


FIGURE 2. $\overline{SD}$ Pin Logic

The LM2743 is also adequate for tracking purposes through the SS/TRACK pin. The tracking circuit, in the design examples below, contains a Master Power Supply with V_{OUT1} = 5V and an LM2743 with V_{OUT2}=1.8V.

Three cases are described:

1. Both output voltages, V_{OUT1} and V_{OUT2}, rise together, reaching their final values at the same time,
2. Both output voltages rise together at the same rate until V_{OUT2} = 1.8V, and finally
3. Output voltage V_{OUT2} starts rising 3.24ms after V_{OUT1} starts.

The calculation of the feedback resistors *Figure 3* for all cases is based on the Tracking Equation. Since V_{FB}=0.6V, V_{OUT2}=1.8V, and R_{FB2}=10kΩ, then the R_{FB1} becomes 5kΩ.

Case 1: Rise together

Both, V_{OUT1} and V_{OUT2}, start rising, and reach their nominal values at the same time as shown in *Figure 4*. This means that V_{OUT2} rises at slower rate then V_{OUT1}.

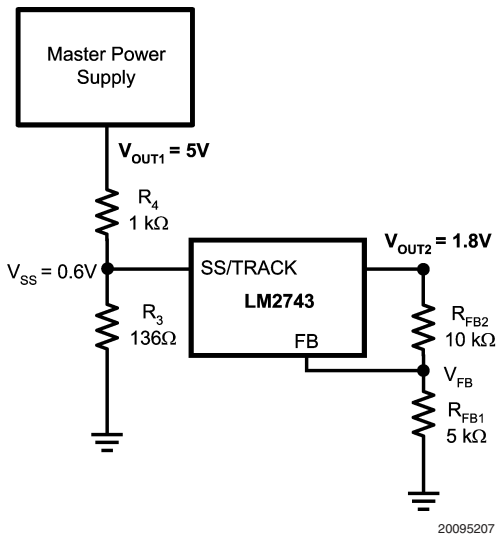


FIGURE 3. Block Diagram of Case 1

$$V_{SS} = V_{OUT1} * (R_3/(R_3+R_4))$$

Application Information (Continued)

$$V_{FB} = V_{OUT2} * (R_{FB2}/(R_{FB1}+R_{FB2}))$$

Since $V_{SS} = V_{FB}$=0.6V, then

Tracking Equation

$$V_{OUT2} = V_{OUT1} \times \frac{R_3}{R_3 + R_4} \times \frac{R_{FB1} + R_{FB2}}{R_{FB2}}$$

The total value of the track resistor divider (*Figure 3*), R_3 and R_4, should be set below 10kΩ for better precision. Let R4=1K, for V_{OUT1}= 5V and V_{OUT2}=1.8V, R_3=136Ω.

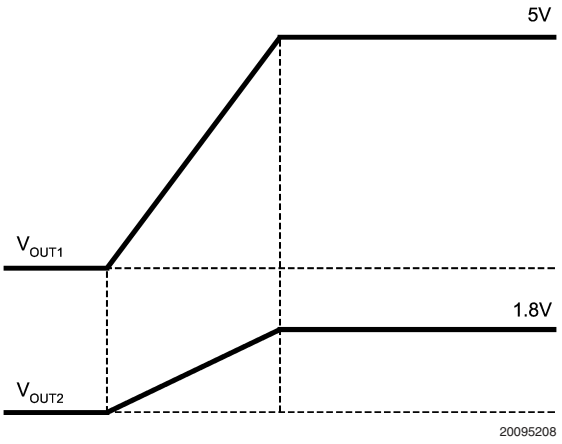


FIGURE 4. Timing Behavior of Case 1

Case 2: Rise together until V_{OUT2}=1.8V

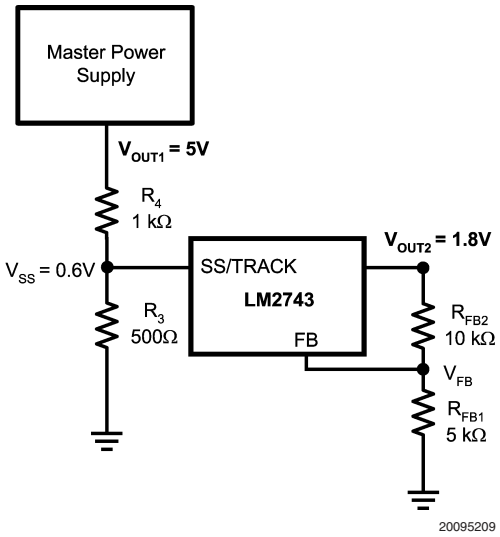


FIGURE 5. Block Diagram of Case 2

$V_{SS} = V_{FB}$= 0.6V,
$V_{OUT1} = V_{OUT2}$ = 1.8V
For R_4=1kΩ, R_3=500Ω (from Tracking Equation).
The soft start reaches 0.6V at V_{OUT1} equal 1.8V.
For V_{OUT1}>1.8V, V_{OUT2} stays in regulation at 1.8V.

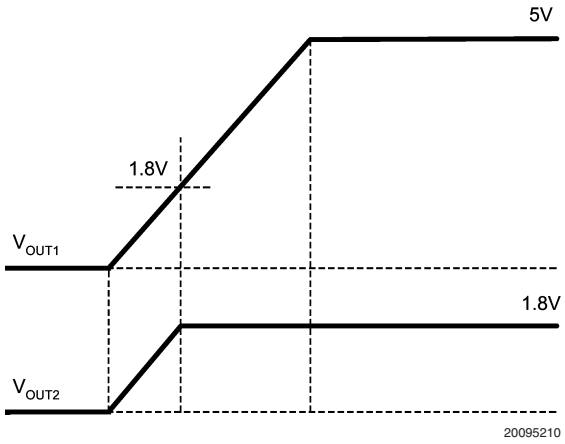


FIGURE 6. Timing Behavior of Case 2

Case 3: V_{OUT2} starts rising 3.0ms after V_{OUT1}

Assuming V_{OUT1} slew rate SR_{VSD} = 1V/ms and voltage divider ratio 1:3 (R_3 = 500Ω and R_4 = 1kΩ), the V_{SD} slew rate equals SR_{VSD} = 0.333V/ms. During the delay time V_{SD} raises to 1.0V ($V_{\overline{SD}\text{-}IH}$) as shown in *Figure 8*. The delay time is calculated from :

$$t_{DELAY} = V_{\overline{SD}\text{-}IH} / SR_{VSD}$$

$$t_{DELAY}$$= 1.0(V) / 0.333(V/ms) = 3.0ms

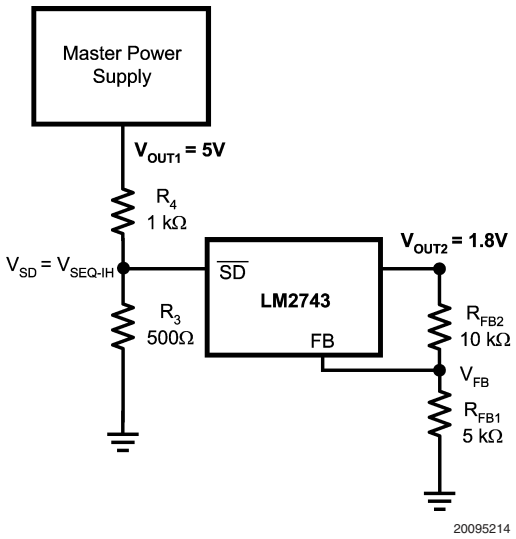


FIGURE 7. Block Diagram of Case 3

Application Information (Continued)

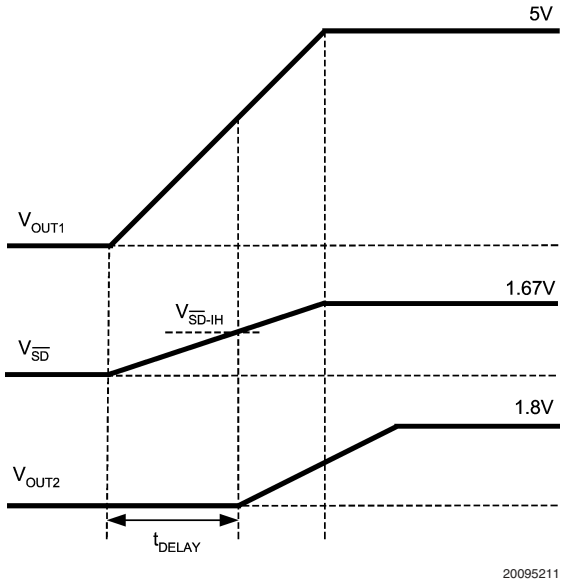


FIGURE 8. Timing Behavior of Case 3

If the tracking through SS/TRACK pin is not used, a capacitor to ground is needed to limit the inrush current.

MOSFET GATE DRIVERS

The LM2743 has two gate drivers designed for driving N-channel MOSFETs in a synchronous mode. Power for the drivers is supplied through the BOOT pin. For the high side gate (HG), to fully turn the top FET on, the BOOT voltage must be at least one $V_{GS(th)}$ greater than V_{IN} ($V_{BOOT} \geq 2V + V_{IN}$). This voltage can be supplied from a separate voltage source or from a local charge pump structure, the bootstrap.

A charge pump can be built using a diodes and small capacitors, as shown in the below figures. The capacitor serves to maintain enough voltage between the top FET gate and source to control the device even when the top FET is on and its source has risen up to the input voltage level.

The LM2743 gate drives use a BiCMOS design. Unlike some other bipolar control ICs, the gate drivers have rail-to-rail swing, ensuring no spurious turn-on due to capacitive coupling.

The LM2743 can operate its internal circuitry at the V_{CC} range from 3.0V to 6.0V. However, the external FETs may operate more efficiently with higher gate drive voltage. *Figure 9* shows a typical bootstrap method where the voltage applied to the FETs is $V_{CC} - V_D$.

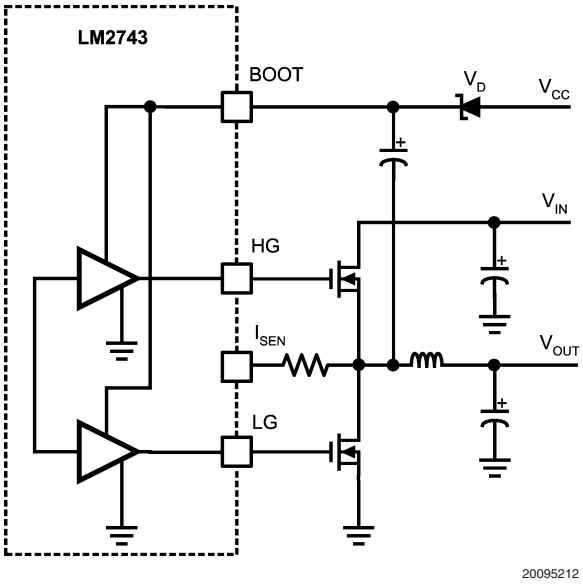


FIGURE 9. Bootstrap Configuration 1

This means that if V_{CC} is 3.0V, the gate drive for the FETs is approximately 2.5V. This voltage could be too low to fully turn the FET on. As a result I^2R losses could be higher than expected.

In the next bootstrap configuration (*Figure 10*) the voltage applied to the high side FET is $V_{CC} - 2V_D$ and to the low side FET is $\mathbf{V_{CC} - 2V_D + V_{IN}}$.

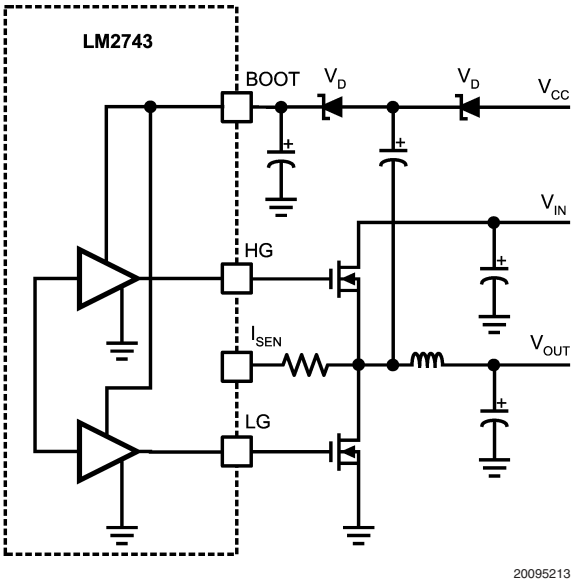


FIGURE 10. Bootstrap Configuration 2

If V_{CC} and V_{IN} are both 3.0V, then 5V is developed at BOOT pin and the low side FET can be driven fully on. The high side FET however may have difficulty turning on since the applied gate drive is only 2V in this case.

The *Figure 11* shows next example of bootstrap configuration. In this case the low gate drive voltage on the top FET is resolved. Now the gate drive on both, the low and high, side FETs is $\mathbf{V_{CC} - 3V_D + V_{IN}}$.

Application Information (Continued)

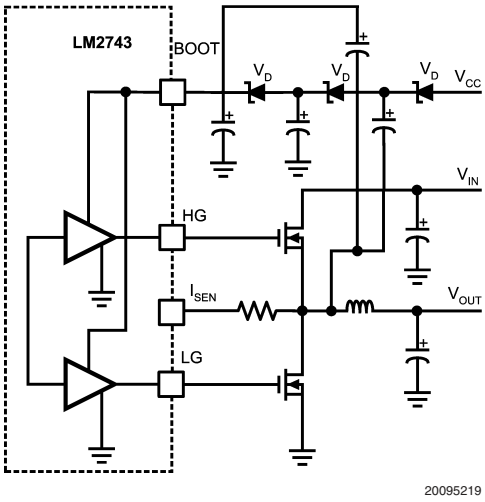


FIGURE 11. Bootstrap Configuration 3

At an input voltage of 3V both, the high and low, side FETs are driven with about 4.5V.

The decision on which configuration to use depends on the desired output current and operating frequency. At high currents and low frequencies, configuration 3 (*Figure 11*) is recommended. For low currents and high frequencies, configuration 1 (*Figure 9*) may work well.

POWER GOOD SIGNAL

The power good signal is the OR-gated flag representing over-voltage and under-voltage conditions. If the feedback pin (FB) voltage is about 18% over its nominal value ($V_{PWGD-TH-HI}$ = 0.710V) or falls about 30% below its nominal value ($V_{PWGD-TH-LO}$ = 0.434V) the power good flag goes low. At about 118% of V_{FB} the converter turns off the high side gate and turns on the low side gate. However, at about 70% of V_{FB} the converter goes to maximum duty cycle and the high and low sides are still switching. The power good flag will return to logic high whenever the feedback pin voltage is between 70% and 118% of 0.6V.

UVLO

The 2.76V turn-on threshold on V_{CC} has a built in hysteresis of 400mV. Therefore, if V_{CC} drops below 2.42V, the chip enters UVLO mode. UVLO consists of turning off the top and bottom FETs, and remaining in that condition until V_{CC} rises above 2.76V. As with shutdown, the soft start capacitor is discharged through a FET, ensuring that the next start-up will be smooth.

CURRENT LIMIT

Current limit is realized by sensing the voltage across the low side FET while it is on. The $R_{DS(ON)}$ of the FET is a known value, and the voltage across the FET can be found from:

$$V_{DS} = I_{DS} * R_{DS(ON)}$$

The current limit is determined by an external resistor, R_{CS}, connected between the switch node and the I_{SEN} pin. A constant current of 40µA is forced through R_{CS}, causing a fixed voltage drop. This fixed voltage is compared against V_{DS} and if the latter is higher, the current limit of the chip has been reached. The R_{CS} can be found by using the following:

$$R_{CS} = R_{DS(ONLOW)}\ (\Omega) \times \frac{I_{LIM}(A)}{40\ \mu(A)}$$

where resistance $R_{DS(ON)}$ is taken from MOSFET's datasheet ($R_{DS(ON\ LOW)}$ =13mΩ) and current limit (I_{LIM}) value is calculated from equation.

$$I_{LIM} = I_{OUT} + 0.5\ \frac{(V_{CC} - V_{OUT}) \times V_{OUT}}{L \times V_{CC} \times F_{OSC}}$$

where: L is the inductance and F_{OSC} is the PWM frequency.

Because current sensing is done across the low side FET, no minimum high side on-time is necessary. In the current limit mode the LM2743 will turn the high side off and the keep low side on for a time as long as necessary. The chip also discharges the soft start capacitor through a fixed 90µA source. This way, smooth ramping up of the output voltage as with a normal soft start is ensured. The output of the LM2743 internal error amplifier is limited by the voltage on the soft start capacitor. Hence, discharging the soft start capacitor reduces the maximum duty cycle (D) of the controller. During severe current limit, this reduction in duty cycle will reduce the output voltage if the current limit conditions last for an extended period of time.

UVF/OVF

The output under-voltage flag (UVF) and over-voltage flag (OVF) mechanisms engage at about 70% and 118% of the target output voltage, respectively. In the UVF case, the LM2743 will turn off the high side switch and turn on the low side switch and dischrage the soft start capacitor through the MOSFET switch. However, in the OVF the converter goes to maximum duty cycle and the high and low sides are still switching. The chip remains in this state until the shutdown pin has been pulled to a logic low and then released. The UVF function is masked only during the initial charge of the soft start capacitor, when voltage is first applied to the V_{CC} pin. The power good flag goes low during this time, giving a logic-level warning signal.

SHUT DOWN

To assure proper IC start-up, shutdown pin ($\overline{SD}$) should not be left floating. For Normal Operation this pin should be connected to V_{CC} or other low voltage source (see Electrical Characteristics table).

If the shutdown pin $\overline{SD}$ is pulled low, the LM2743 discharges the soft start capacitor through a MOSFET switch. The high and the low side switches are turned off. The LM2743 remains in this state until $\overline{SD}$ is released.

DESIGN CONSIDERATIONS

The following is a design procedure for all the components needed to create the Typical Application Circuit. The designed 3.3V (V_{CC}) to 1.2V (V_{OUT}) converter is capable of delivering 4A with an efficiency of 89% at switching frequency of 300kHz. The same procedures can be followed to create many other designs with varies input and output voltages, and load current.

Application Information (Continued)

Input Capacitor

The input capacitors in a Buck switching converter are subjected to high stress due to the input current square waveform. Hence input capacitors are selected for their ripple current capability and their ability to withstand the heat generated as that ripple current runs through their ESR. Input rms ripple current is approximately:

$$I_{RMS\_RIP} = I_{OUT} \times \sqrt{D(1 - D)}$$

where D is the duty cycle.

The power dissipated by each input capacitor is:

$$P_{CAP} = \frac{(I_{RMS\_RIP})^2 \times ESR}{n^2}$$

where, n is the number of capacitors, and ESR is the equivalent series resistance of C_{IN1}.

The equation indicates that power loss in each capacitor decreases rapidly as the number of input capacitors increases. The worst-case ripple for a Buck converter occurs during full load and when the duty cycle (D) is 0.5. For design 3.3V (V_{CC}) to 1.2V (V_{OUT}) the duty cycle is 0.364. With a 4A maximum load the ripple current is around 2A. The Sanyo 20SP120M aluminum electrolytic capacitor works fine here. It has a ripple current rating of 3A and maximum ESR of 24mΩ at 100kHz. The power dissipated by the Sanyo's capacitor is then 0.088W. Other options for input and output capacitors include MLCC, Tantalum, OSCON, SP, and POSCAPS.

Support Components: Capacitors (C_{IN2}, C_{CC}, C_{BOOT}, C_{SS}), Resistors (R_{CC}, R_{CS}, R_{FADJ}, $R_{PULL-UP}$), and Schottky Diode (D_1)

C_{IN2} - the MOSFET's input capacitor is high frequency bypass device designed to filter harmonics of the switching frequency and input noise. 0.1µF - 1µF ceramic capacitor with a sufficient voltage rating will work well in almost any case.

R_{CC}, C_{CC}, and C_{BOOT} - bypass resistor and bypass capacitors are standard filter components designed to ensure smooth DC voltage for the chip supply and for the bootstrap structure, if it is used. Recommended values: R_{CC}= 10Ω, C_{CC}= 0.1µF, and C_{BOOT} = 0.1µF.

$R_{PULL-UP}$ – this is a standard pull-up resistor for the open-drain power good signal (PWGD). The recommended value: 100Ω: connected to V_{CC}. If this feature is not necessary, the resistor can be omitted.

D_1 - Schottky diode should be used for the bootstrap. It allows the minimum drop for both, high and low side drivers. The MBR0520 works well here.

R_{CS} - resistor used to set the current limit. Since the design calls for a peak current magnitude (I_{OUT}+0.5*ΔI_{OUT}) of 4.8A, a safe setting would be 6A. (This is below the saturation current of the output inductor, which is 7.8 A.) Following the equation from the Current Limit section, use a 1.5kΩ resistor.

R_{FADJ} - this resistor is used to set the switching frequency (F_{OSC}) of the chip. The resistor value is calculated from equation in Normal Operation section. To obtain the switching frequency of 300kHz, 110kΩ, 1% resistor is needed.

C_{SS} - the soft start capacitor depends on the user requirements and is calculated based on the equation from the Start Up section. For a 7ms delay, a 12nF capacitor will be suitable.

Output Inductor

The output inductor forms the first half of the power stage in a Buck converter. It is responsible for smoothing the square wave created by the switching action and for controlling the output current ripple (ΔI_{OUT}). The inductance is chosen by selecting between tradeoffs in efficiency and response time. The smaller the output inductor, the more quickly the converter can respond to transients in the load current. However, as shown in the efficiency calculations, a smaller inductor requires a higher switching frequency to maintain the same level of output current ripple. An increase in frequency can mean increasing loss in the FETs due to the charging and discharging of the gates. Generally the switching frequency is chosen so that conduction loss outweighs switching loss. The equation for output inductor selection is:

$$L = \frac{V_{CC} - V_{OUT}}{\Delta I_{OUT} \times F_{OSC}} \times D$$

$$L = \frac{3.3V - 1.2V}{0.4A \times 4A \times 300\ kHz} \times \frac{1.2V}{3.3V}$$

L = 16µH

Plugging in the values for output current ripple, input voltage, output voltage, switching frequency, and assuming a 40% peak-to-peak output current ripple yields an inductance of 1.6µH. The output inductor must be rated to handle the peak current (also equal to the peak switch current), which is (I_{OUT} + 0.5*ΔI_{OUT}) 4.8A for a 4A design. The Coilcraft DO3316P-222P is 2.2µH, is rated to 7.4A rms, and has a direct current resistance (DCR_{IOUT}) of 11mΩ.

Output Capacitor

The output capacitor forms the second half of the power stage of a Buck switching converter. It is used to control the output voltage ripple (ΔV_{OUT}) and to supply load current during fast load transients.

In this example the output current is 4A and the expected type of capacitor is an aluminum electrolytic, as with the input capacitors. Other possibilities include ceramic, tantalum, and solid electrolyte capacitors, however the ceramic type often do not have the large capacitance needed to supply current for load transients, and tantalums tend to be more expensive than aluminum electrolytic. Aluminum capacitors tend to have very high capacitance and fairly low ESR, meaning that the ESR zero, which affects system stability, will be much lower than the switching frequency. The large capacitance means that at switching frequency, the ESR is dominant, hence the type and number of output capacitors is selected on the basis of ESR. One simple formula to find the maximum ESR based on the desired output voltage ripple, ΔV_{OUT} and the designed output current ripple, ΔI_{OUT}, is:

$$ESR_{MAX} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}}$$

Application Information (Continued)

In this example, in order to maintain a 2% peak-to-peak output voltage ripple and a 40% peak-to-peak inductor current ripple, the required maximum ESR is 15mΩ.The Sanyo 4SP560M aluminum electrolytic capacitor will give an equivalent ESR of 14mΩ. The capacitance of 560µF is enough to supply even severe load transients.

MOSFETs

MOSFETs are the critical parts of any switching controller. Both, the control high side FET and the synchronous low side FET, have a direct impact on the system efficiency.

In this case the target efficiency for typical application circuit is about 89%. This variable will determine which MOSFET is acceptable to use for the design.

Loss from the capacitors, inductors, and IC come to about 0.27W. This leaves about 0.33W for the FET switching, conduction, and gate charging losses to meet the target efficiency. All the losses are detailed in the Efficiency section.

The switching loss is particularly difficult to estimate because it depends on many factors. When the load current is more than about 1 or 2 amps, conduction losses outweigh the switching and gate charging losses. This allows FET selection based on the $R_{DS(ON)}$ of the FET. After adding the FET switching and gate charging losses about 0.27W leaves for conduction losses. When plugged MOSFET, the FDS6898A with a typical $R_{DS(ON)}$ of 13mΩ, into the equation from Efficiency section for P_{CND} the loss come to be about 0.27W.

Control Loop Components

The Typical Application Circuit has been compensated to improve the DC gain and bandwidth. The result of this compensation is better line and load transient responses. For the LM2743, the top feedback divider resistor, R_{FB2}, is also a part of the compensation. For the 3.3V to 1.2V at 4A design, the values are:

C_{C1} = 27pF, C_{C2} = 1200nF, C_{C3} = 3300pF, R_{C1} = 40.2kΩ, R_{C2} = 2.55kΩ, R_{FB2} = 10kΩ.

These values give a phase margin of 53˚ and a bandwidth of 80kHz.

EFFICIENCY CALCULATIONS

A reasonable estimation of the efficiency of a switching buck controller can be obtained by adding together the Output Power (P_{OUT}) loss and the Total Power (P_{TOTAL}) loss:

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{TOTAL}} \times 100\%$$

The Output Power (P_{OUT}) for theTypical Application Circuit design is (1.2V * 4A) = 4.8W. The Total Power (P_{TOTAL}), with an efficiency calculation to complement the design, is shown below.

The majority of the power losses are due to low and high side of MOSFET's losses. The losses in any MOSFET are group of switching (P_{SW}) and conduction losses(P_{CND}).

$$P_{FET} = P_{SW} + P_{CND} = 61.38mW + 270mW$$
$$P_{FET} = 331.4mW$$

FET Switching Loss (P_{SW})

$$P_{SW} = P_{SW(ON)} + P_{SW(OFF)}$$
$$P_{SW} = 0.5 * V_{CC} * I_{OUT} * (t_r + t_f) * F_{OSC}$$
$$P_{SW} = 0.5 \times 3.3V \times 4A \times 300kHz \times 31ns$$
$$P_{SW} = 61.38mW$$

The FDS6898A has a typical turn-on rise time t_r and turn-off fall time t_f of 15ns and 16ns, respectively. The switching losses for this type of dual N-Channel MOSFETs are 0.061W.

FET Conduction Loss (P_{CND})

$$P_{CND} = P_{CND1} + P_{CND2}$$
$$P_{CND1} = I^2_{OUT} \times R_{DS(ON)} \times k \times D$$
$$P_{CND2} = I^2_{OUT} \times R_{DS(ON)} \times k \times (1-D)$$

$R_{DS(ON)}$ = 13mΩ and the factor is a constant value (k = 1.3) to account for the increasing $R_{DS(ON)}$ of a FET due to heating.

$$P_{CND1} = (4A)^2 \times 13m\Omega \times 1.3 \times 0.364$$
$$P_{CND2} = (4A)^2 \times 13m\Omega \times 1.3 \times (1 - 0.364)$$
$$P_{CND} = 98.42mW + 172mW = 270mW$$

There are few additional losses that are taken into account:

IC Operating Loss (P_{IC})

$$P_{IC} = I_{Q\_VCC} \times V_{CC},$$

where $I_{Q\text{-}VCC}$ is the typical operating V_{CC} current

$$P_{IC} = 1.5mA * 3.3V = 4.95mW$$

FET Gate Charging Loss (P_{GATE})

$$P_{GATE} = n * V_{CC} * Q_{GS} * F_{OSC}$$
$$P_{GATE} = 2 \times 3.3V \times 3nC \times 300kHz$$
$$P_{GATE} = 5.94mW$$

The value n is the total number of FETs used and Q_{GS} is the typical gate-source charge value, which is 3nC. For the FDS6898A the gate charging loss is 5.94mW.

Input Capacitor Loss (P_{CAP})

$$P_{CAP} = \frac{(I_{RMS\_RIP})^2 \times ESR}{n^2}$$

Where,

$$I_{RMS\_RIP} = I_{OUT} \times \sqrt{D(1 - D)}$$

n is the number of capacitors, and ESR is equivalent series resistance.

$$P_{CAP} = \frac{(1.924A)^2 \times 24m\Omega}{I^2}$$

$$P_{CAP} = 88.8mW$$

Output Inductor Loss (P_{IND})

$$P_{IND} = I^2_{OUT} * DCR_{IOUT},$$

where DCR_{IOUT} is the direct current resistance

$$P_{IND} = (4A)^2 \times 11m\Omega$$
$$P_{IND} = 176mW$$

Total System Efficiency

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{TOTAL}} \times 100\%$$

$$\eta = \frac{4.8W}{4.8W + 0.6W} = 89\%$$

Example Circuits

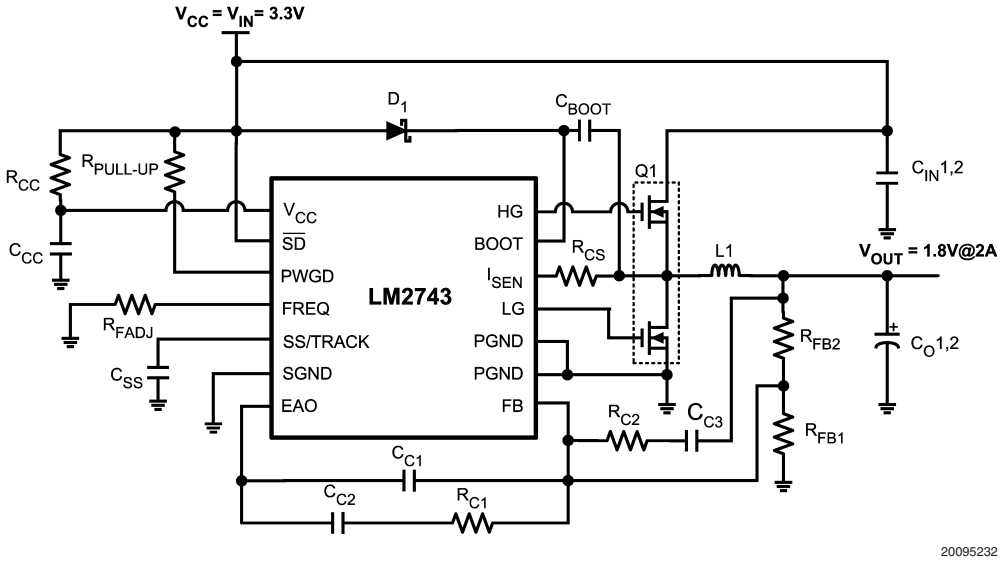


FIGURE 12. 3.3V to 1.8V @ 2A, F_{SW} = 300kHz

PART	PART NUMBER	TYPE	PACKAGE	DESCRIPTION	VENDOR
U_1	LM2743	Synchronous Controller	TSSOP-14		NSC
Q_1	FDS6898A	Dual N-MOSFET	SO-8	20V, 10mΩ@ 4.5V, 16nC	Fairchild
D_1	MBR0520LTI	Schottky Diode	SOD-123		
L_1	DO3316P-472	Inductor		4.7µH, 4.8Arms 18mΩ	Coilcraft
$C_{IN}1$	16SP100M	Aluminum Electrolytic		100µF, 16V, 2.89Arms	Sanyo
C_O1	6SP220M	Aluminum Electrolytic		220µF, 6.3V 3.1Arms	Sanyo
C_{CC}, C_{BOOT}, $C_{IN}2$, C_O2	VJ1206Y104KXXA	Capacitor	1206	0.1µF, 10%	Vishay
C_{C3}	VJ805Y332KXXA	Capacitor	805	3300pF, 10%	Vishay
C_{SS}	VJ0805Y123KXXA	Capacitor	805	12nF, 10%	Vishay
C_{C2}	VJ1805A821KXAA	Capacitor	805	820pF 10%	Vishay
C_{C1}	VJ0805A220KXAA	Capacitor	805	22pF, 10%	Vishay
R_{FB2}	CRCW08051002F	Resistor	805	10.0kΩ 1%	Vishay
R_{FB1}	CRCW08054991F	Resistor	805	4.99kΩ1%	Vishay
R_{FADJ}	CRCW08051103F	Resistor	805	110kΩ 1%	Vishay
R_{C2}	CRCW08052101F	Resistor	805	2.1kΩ 1%	Vishay
R_{CS}	CRCW08057500F	Resistor	805	750Ω 1%	Vishay
R_{CC}	CRCW080510R0F	Resistor	805	10.0Ω 1%	Vishay
R_{C1}	CRCW08055492F	Resistor	805	54.9kΩ 1%	Vishay
$R_{PULL-UP}$	CRCW08051003J	Resistor	805	100kΩ 5%	Vishay

Example Circuits (Continued)

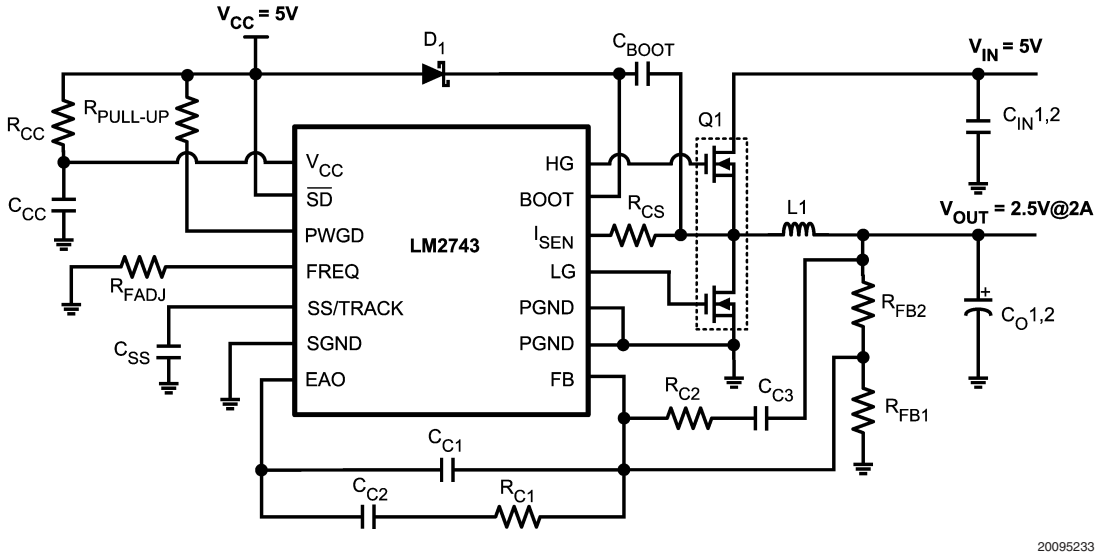


FIGURE 13. 5V to 2.5V @ 2A, F_{SW} = 300kHz

PART	PART NUMBER	TYPE	PACKAGE	DESCRIPTION	VENDOR
U_1	LM2743	Synchronous Controller	TSSOP-14		NSC
Q_1	FDS6898A	Dual N-MOSFET	SO-8	20V, 10mΩ@ 4.5V, 16nC	Fairchild
D_1	MBR0520LTI	Schottky Diode	SOD-123		
L_1	DO3316P-682	Inductor		6.8µH, 4.4Arms, 27mΩ	Coilcraft
C_{IN}1	16SP100M	Aluminum Electrolytic		100µF, 16V, 2.89Arms	Sanyo
C_O1	10SP56M	Aluminum Electrolytic		56µF, 10V 1.7Arms	Sanyo
C_{CC}, C_{BOOT}, C_{IN}2, C_O2	VJ1206Y104KXXA	Capacitor	1206	0.1µF, 10%	Vishay
C_{C3}	VJ0805A182KXAA	Capacitor	805	1800pF, 10%	Vishay
C_{SS}	VJ0805Y123KXXA	Capacitor	805	12nF, 10%	Vishay
C_{C2}	VJ1805A821KXAA	Capacitor	805	820pF 10%	Vishay
C_{C1}	VJ0805A330KXAA	Capacitor	805	33pF, 10%	Vishay
R_{FB2}	CRCW08051002F	Resistor	805	10.0kΩ 1%	Vishay
R_{FB1}	CRCW08053161F	Resistor	805	3.16kΩ 1%	Vishay
R_{FADJ}	CRCW08051103F	Resistor	805	110kΩ 1%	Vishay
R_{C2}	CRCW08051301F	Resistor	805	1.3kΩ 1%	Vishay
R_{CS}	CRCW08057870F	Resistor	805	787Ω 1%	Vishay
R_{CC}	CRCW080510R0F	Resistor	805	10.0Ω 1%	Vishay
R_{C1}	CRCW08053322F	Resistor	805	33.2kΩ 1%	Vishay
$R_{PULL-UP}$	CRCW08051003J	Resistor	805	100kΩ 5%	Vishay

Example Circuits (Continued)

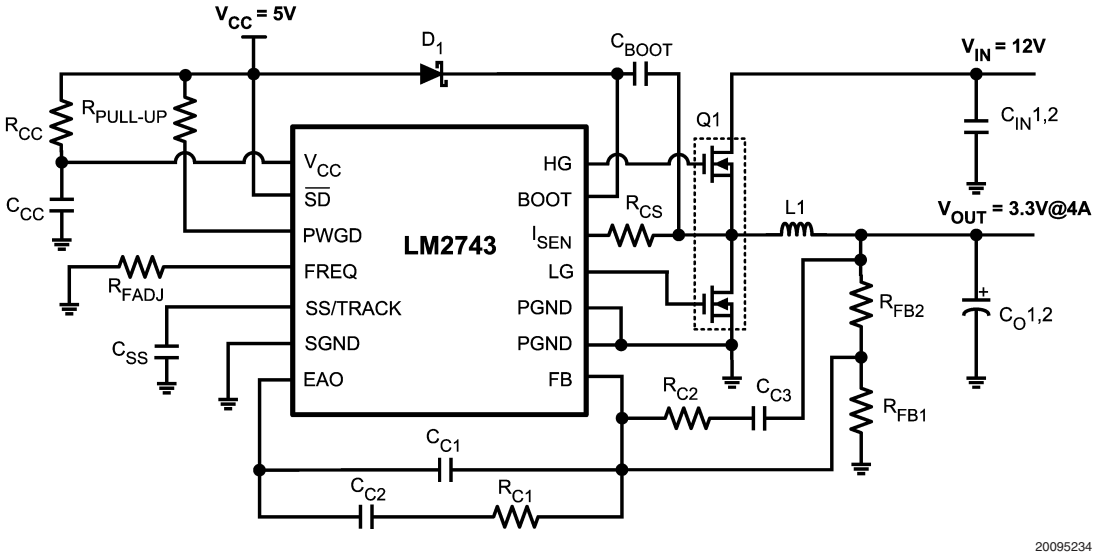


FIGURE 14. 5V to 3.3V @ 4A, F_{SW} = 300kHz

PART	PART NUMBER	TYPE	PACKAGE	DESCRIPTION	VENDOR
U_1	LM2743	Synchronous Controller	TSSOP-14		NSC
Q_1	FDS6898A	Dual N-MOSFET	SO-8	20V, 10mΩ@ 4.5V, 16nC	Fairchild
D_1	MBR0520LTI	Schottky Diode	SOD-123		
L_1	DO3316P-332	Inductor		3.3µH, 5.4Arms 15mΩ	Coilcraft
C_{IN}1	16SP100M	Aluminum Electrolytic		100µF, 16V	Sanyo
				2.89Arms	
C_O1	6SP220M	Aluminum Electrolytic		220µF, 6.3V 3.1Arms	Sanyo
C_{CC}, C_{BOOT}, C_{IN}2, C_O2	VJ1206Y104KXXA	Capacitor	1206	0.1µF, 10%	Vishay
C_{C3}	VJ805Y222KXXA	Capacitor	805	2200pF, 10%	Vishay
C_{SS}	VJ0805Y123KXXA	Capacitor	805	12nF, 10%	Vishay
C_{C2}	VJ805Y332KXXA	Capacitor	805	3300pF 10%	Vishay
C_{C1}	VJ0805A820KXAA	Capacitor	805	82pF, 10%	Vishay
R_{FB2}	CRCW08051002F	Resistor	805	10.0kΩ 1%	Vishay
R_{FB1}	CRCW08052211F	Resistor	805	2.21kΩ 1%	Vishay
R_{FADJ}	CRCW08051103F	Resistor	805	110kΩ 1%	Vishay
R_{C2}	CRCW08052611F	Resistor	805	2.61kΩ 1%	Vishay
R_{CS}	CRCW08057870F	Resistor	805	787Ω 1%	Vishay
R_{CC}	CRCW080510R0F	Resistor	805	10.0Ω 1%	Vishay
R_{C1}	CRCW08051272F	Resistor	805	12.7kΩ 1%	Vishay
$R_{PULL-UP}$	CRCW08051003J	Resistor	805	100kΩ 5%	Vishay

Evaluation Board Schematic

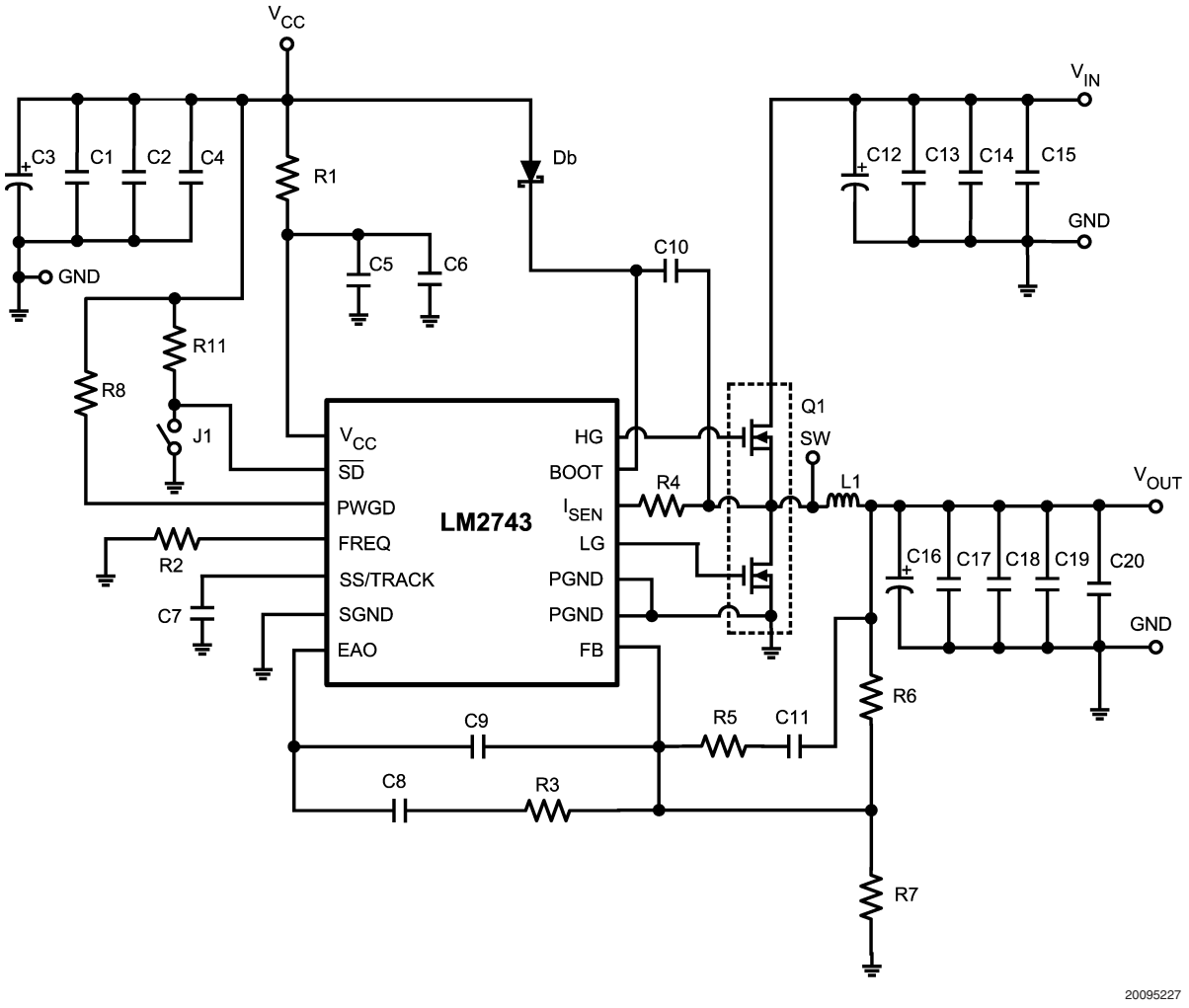


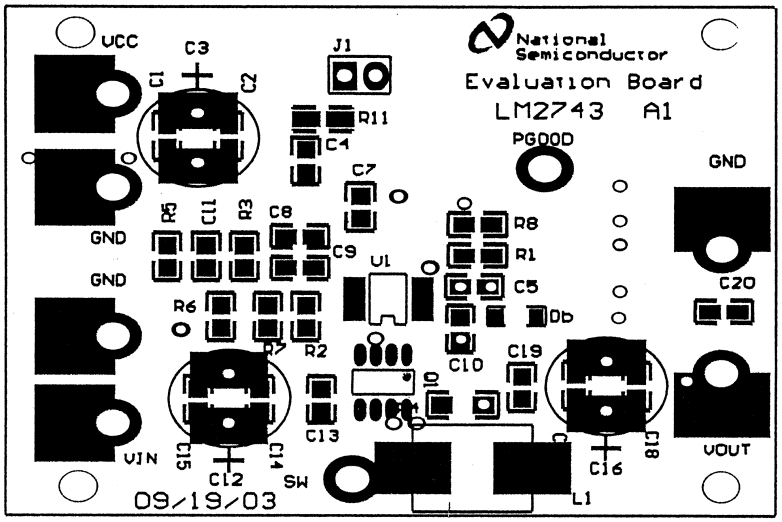
FIGURE 15. 3.3V to 1.2V @ 4A, F_{SW} = 300kHz

PART	PART NUMBER	TYPE	PACKAGE	DESCRIPTION	VENDOR
U_1	LM2743	Synchronous Controller	TSSOP-14		NSC
Q_1	FDS6898A	Dual N-MOSFET	SO-8	20V, 10mΩ@ 4.5V, 16nC	Fairchild
D_1	MBR0520LTI	Schottky Diode	SOD-123		
L_1	DO3316P-222	Inductor		2.2µH, 6.1Arms 12mΩ	Coilcraft
J_1	NOT USED				
C12	20SP120M	Aluminum Electrolytic		120µF, 20V 3.1Arms	Sanyo
C16	4SP560M	Aluminum Electrolytic		560µF, 4V 4Arms	Sanyo
C4,C5,C10, C13,C19	VJ1206Y104KXXA	Capacitor	1206	0.1µF, 10%	Vishay
C11	VJ805Y332KXXA	Capacitor	805	3300pF 10%	Vishay
C7	VJ0805Y123KXXA	Capacitor	805	12nF, 10%	Vishay

Evaluation Board Schematic (Continued)

PART	PART NUMBER	TYPE	PACKAGE	DESCRIPTION	VENDOR
C8	VJ1206Y122KXXA	Capacitor	1206	1200pF 10%	Vishay
C9	VJ0805A270KXAA	Capacitor	805	27pF, 10%	Vishay
C1, C2, C3, C6, C14, C15, C17, C18, C20	NOT USED				
R6	CRCW08051002F	Resistor	805	10.0kΩ 1%	Vishay
R7	CRCW08051002F	Resistor	805	10.0kΩ1%	Vishay
R2	CRCW08051103F	Resistor	805	110kΩ 1%	Vishay
R5	CRCW08052551F	Resistor	805	2.55kΩ 1%	Vishay
R4	CRCW08051501F	Resistor	805	1.50kΩ 1%	Vishay
R1	CRCW080510R0F	Resistor	805	10.0Ω 1%	Vishay
R3	CRCW08054022F	Resistor	805	40.2kΩ 1%	Vishay
R11	CRCW08050R00F	Resistor	805	0Ω 1%	Vishay
R8	CRCW08051003J	Resistor	805	100kΩ 5%	Vishay

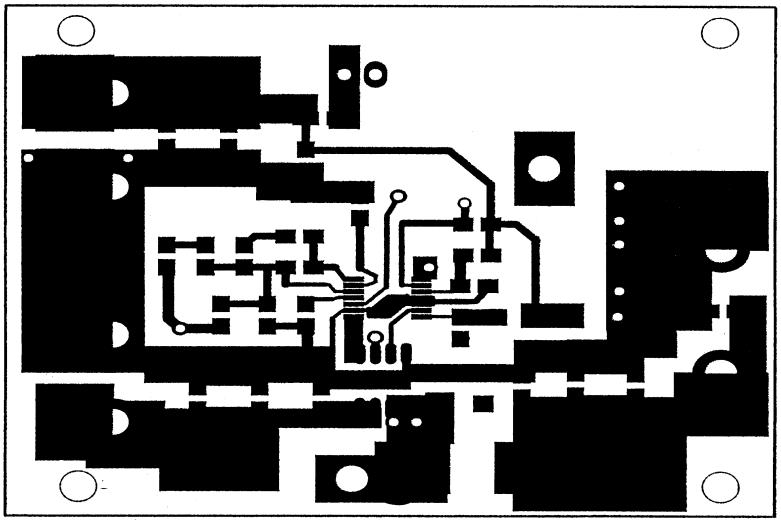
PCB Layout for the Evaluation Board



20095236

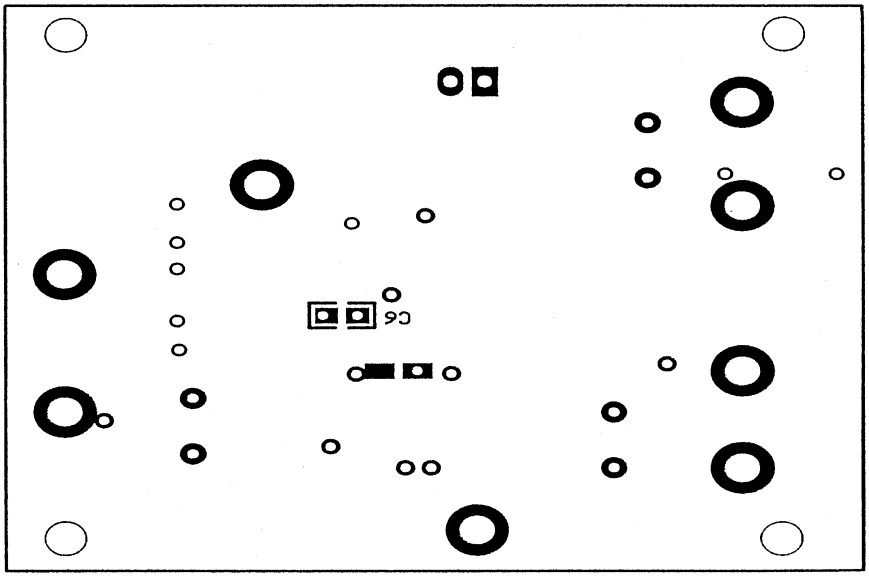
Top Silkscreen

PCB Layout for the Evaluation Board (Continued)



20095237

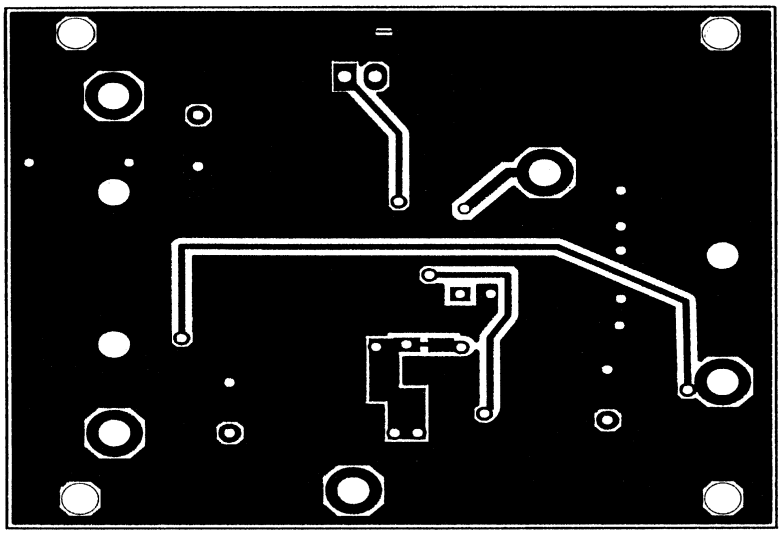
Top Copper



20095238

Bottom Silkscreen

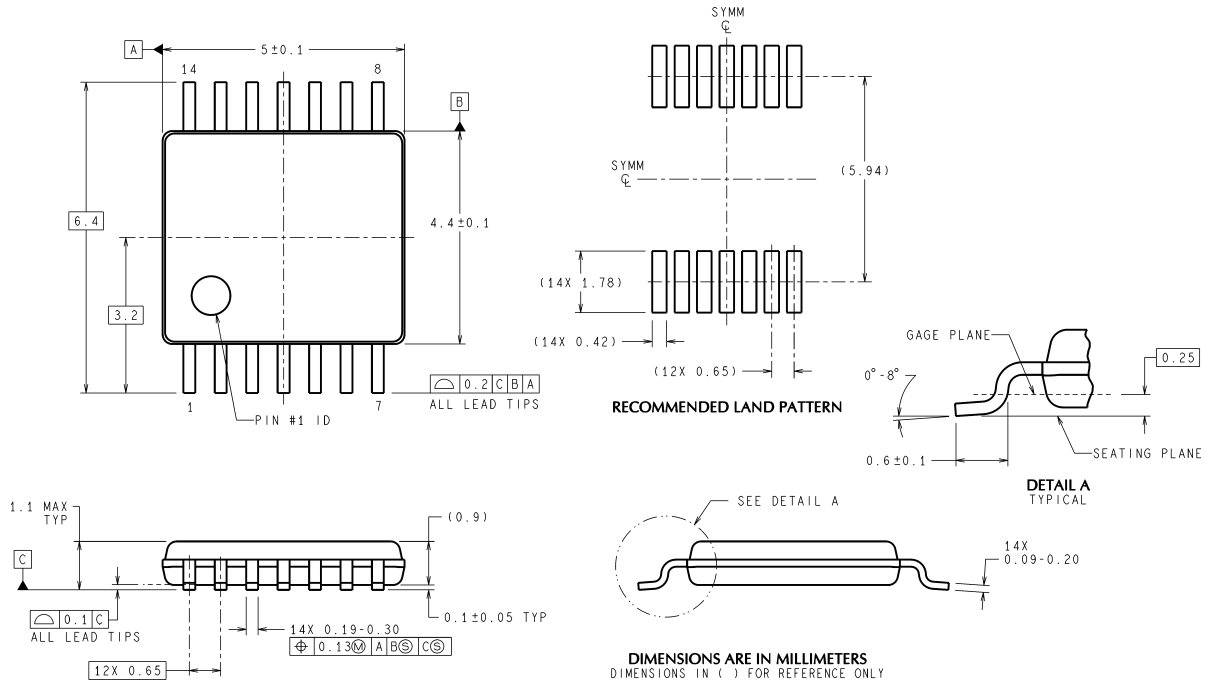
PCB Layout for the Evaluation Board (Continued)



20095239

Bottom Copper

Physical Dimensions inches (millimeters) unless otherwise noted



MTC14 (Rev D)

TSSOP-14 Pin Package
NS Package Number MTC14

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE

National Semiconductor certifies that the products and packing materials meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no "Banned Substances" as defined in CSP-9-111S2.

National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560