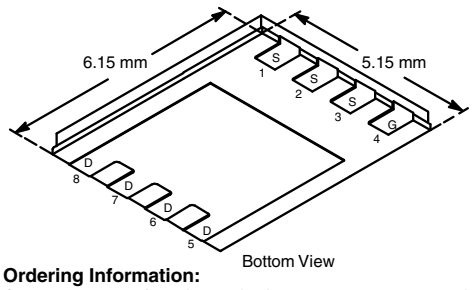
SiR403EDP

Vishay Siliconix

P-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω) Max.	I_D [a, e]	Q_g (Typ.)
- 30	0.0065 at V_{GS} = - 10 V	- 40	66 nC
	0.0082 at V_{GS} = - 6 V	- 40	
	0.0115 at V_{GS} = - 4.5 V	- 40	

PowerPAK® SO-8



Bottom View

Ordering Information:
SiR403EDP-T1-GE3 (Lead (Pb)-free and Halogen-free)

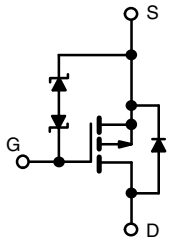
FEATURES

- Extended V_{GS} range (± 25 V) for adaptor switch applications
- Extremely low $R_{DS(on)}$
- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested
- Typical ESD Performance: 4000 V (HBM)
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Adaptor Switch, Load Switch
- Power Management
- Notebook Computers and Portable Battery Packs



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	- 30	V
Gate-Source Voltage		V_{GS}	± 25	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	- 40[e]	A
	T_C = 70 °C		- 40[e]	
	T_A = 25 °C		- 21.9[b,c]	
	T_A = 70 °C		- 17.5[b,c]	
Pulsed Drain Current (t = 300 µs)		I_{DM}	- 60	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	- 40[e]	
	T_A = 25 °C		- 4.2[b, c]	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	- 40	
Single Pulse Avalanche Energy		E_{AS}	80	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	56.8	W
	T_C = 70 °C		36.4	
	T_A = 25 °C		5[b,c]	
	T_A = 70 °C		3.2[b,c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) [f,g]			260	

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[b, d]	t ≤ 10 s	R_{thJA}	20	25	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.7	2.2	

Notes:
a. Based on T_C = 25 °C.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. Maximum under steady state conditions is 68 °C/W.
e. Package Limited
f. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
g. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

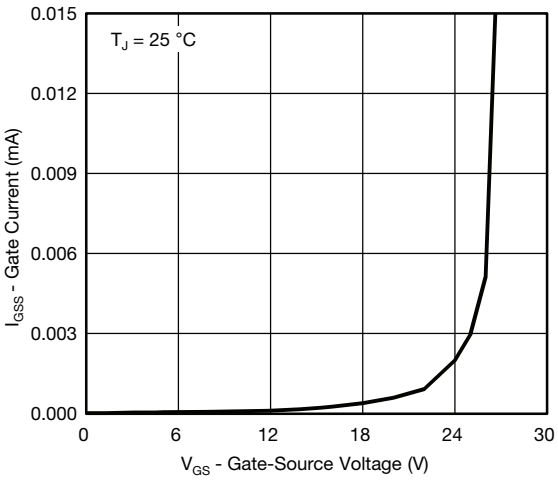
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 250 µA		- 24		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = - 250 µA	- 1.2		- 2.8	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 25 V			± 150	µA
		V_{DS} = 0 V, V_{GS} = ± 20 V			± 15	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 30 V, V_{GS} = 0 V			- 1	
		V_{DS} = - 30 V, V_{GS} = 0 V, T_J = 55 °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq$ - 5 V, V_{GS} = - 10 V	- 20			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 13 A		0.0054	0.0065	Ω
		V_{GS} = - 6 V, I_D = - 10 A		0.0068	0.0082	
		V_{GS} = - 4.5 V, I_D = - 8 A		0.0093	0.0115	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 15 V, I_D = - 13 A		44		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 15 V, V_{GS} = 0 V, f = 1 MHz		4620		pF
Output Capacitance	C_{oss}			880		
Reverse Transfer Capacitance	C_{rss}			820		
Total Gate Charge	Q_g	V_{DS} = - 15 V, V_{GS} = - 10 V, I_D = - 17.3 A		102	153	nC
		V_{DS} = - 15 V, V_{GS} = - 5 V, I_D = - 17.3 A		66	80	
Gate-Source Charge	Q_{gs}			16		
Gate-Drain Charge	Q_{gd}			28		
Gate Resistance	R_g	f = 1 MHz	0.3	1.3	2.6	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 0 V, R_L = 1.5 Ω $I_D \cong$ - 10 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		70	105	ns
Rise Time	t_r			70	105	
Turn-Off Delay Time	$t_{d(off)}$			45	68	
Fall Time	t_f			27	41	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 15 V, R_L = 1.5 Ω $I_D \cong$ - 10 A, V_{GEN} = - 10 V, R_g = 1 Ω		18	30	
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(off)}$			52	80	
Fall Time	t_f			14	25	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			- 5.8	A
Pulse Diode Forward Current	I_{SM}				- 60	
Body Diode Voltage	V_{SD}	I_S = - 10 A, V_{GS} = 0 V		- 0.78	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 10 A, dI/dt = 100 A/µs, T_J = 25 °C		35	53	ns
Body Diode Reverse Recovery Charge	Q_{rr}			25	38	nC
Reverse Recovery Fall Time	t_a			19		ns
Reverse Recovery Rise Time	t_b			16		

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing.

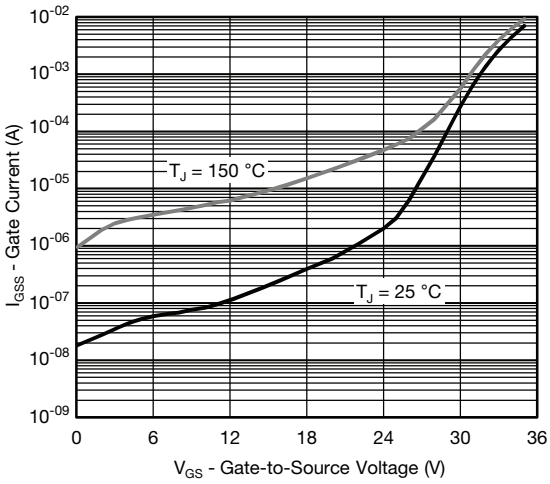
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

For technical questions, contact: pmostechsupport@vishay.com
Document Number: 66744
S13-0302-Rev. A, 11-Feb-13

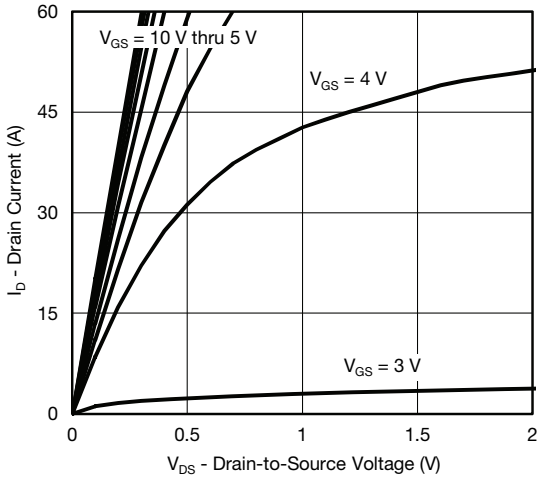
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



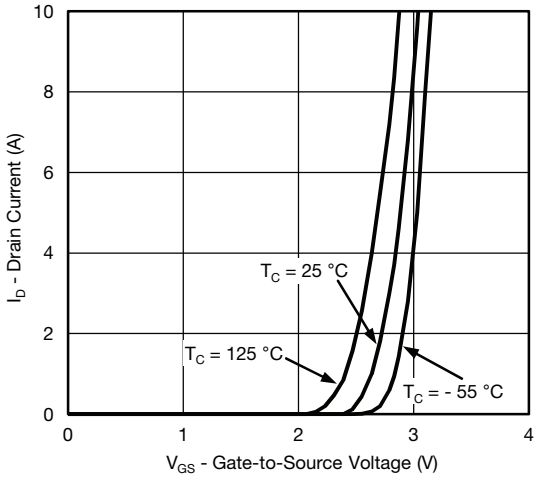
Gate Current vs. Gate-Source Voltage



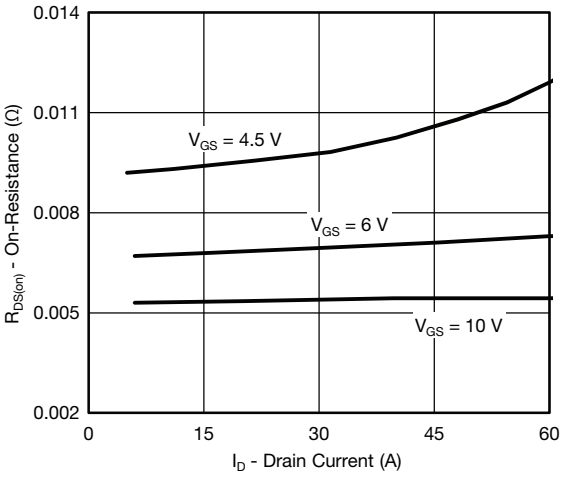
Gate Current vs. Gate-Source Voltage



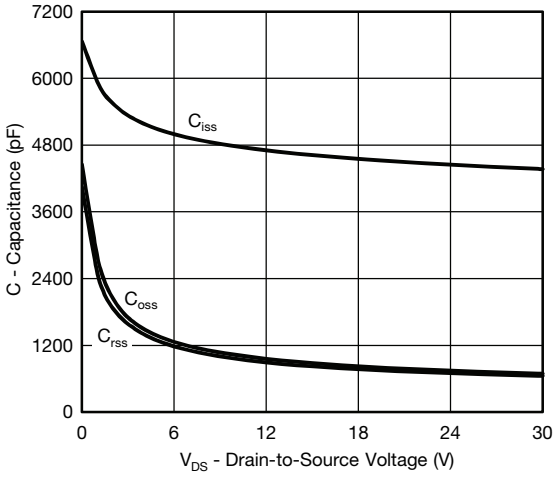
Output Characteristics



Transfer Characteristics

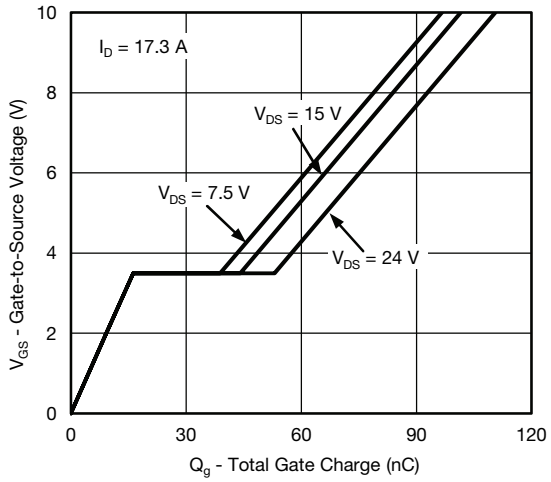


On-Resistance vs. Drain Current

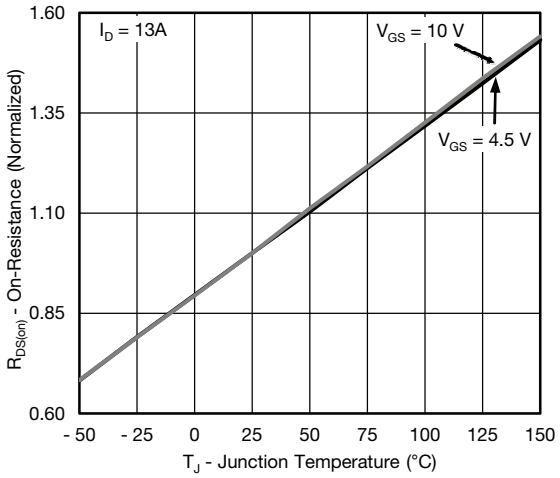


Capacitance

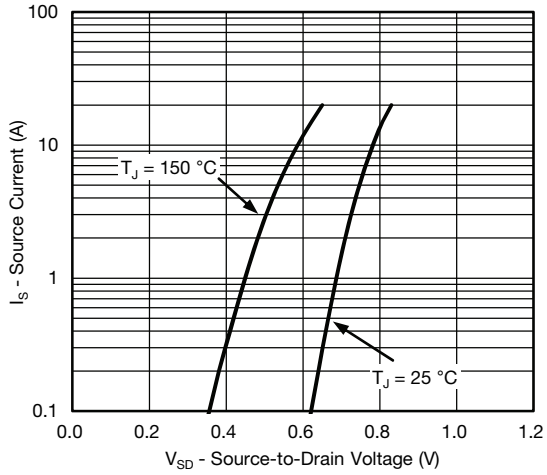
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



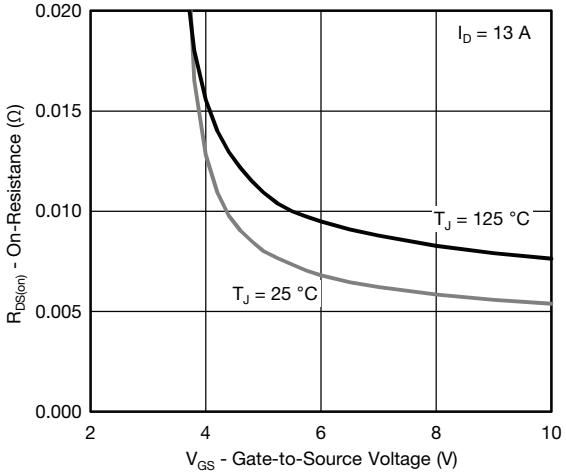
Gate Charge



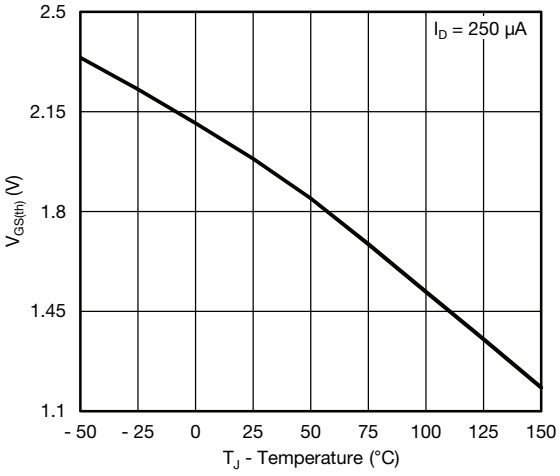
On-Resistance vs. Junction Temperature



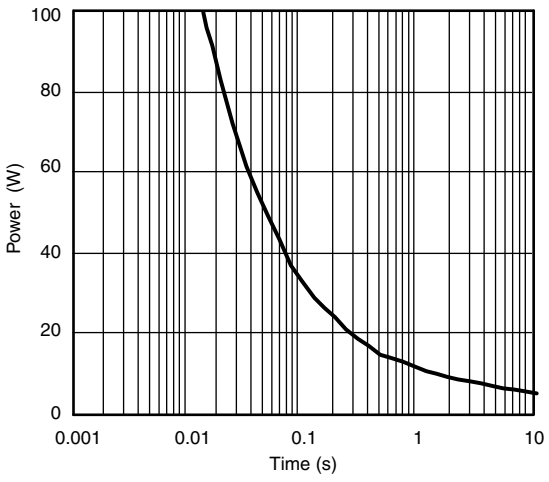
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

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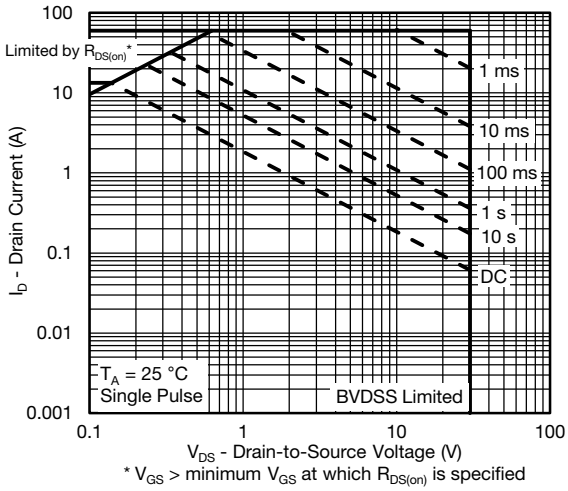
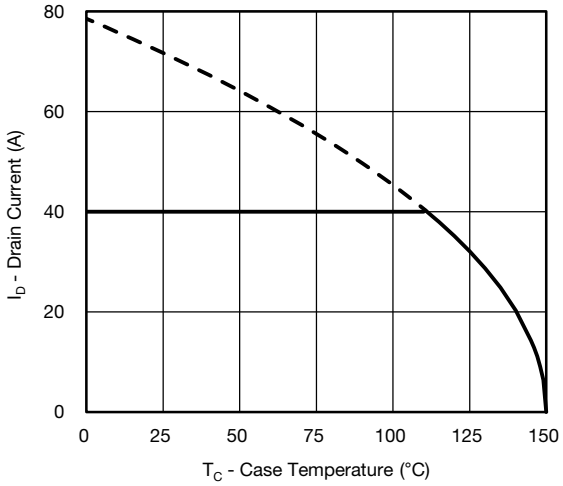
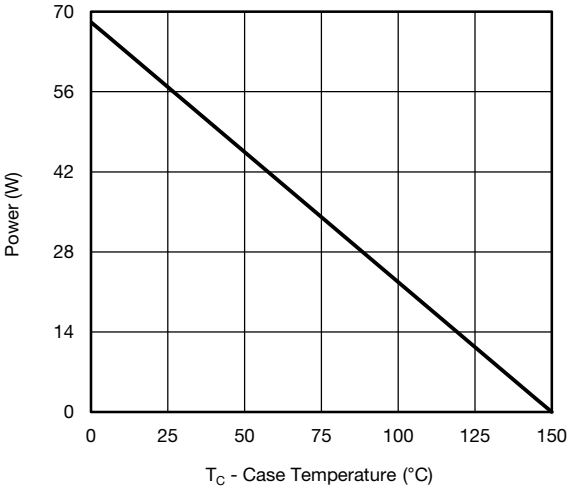
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



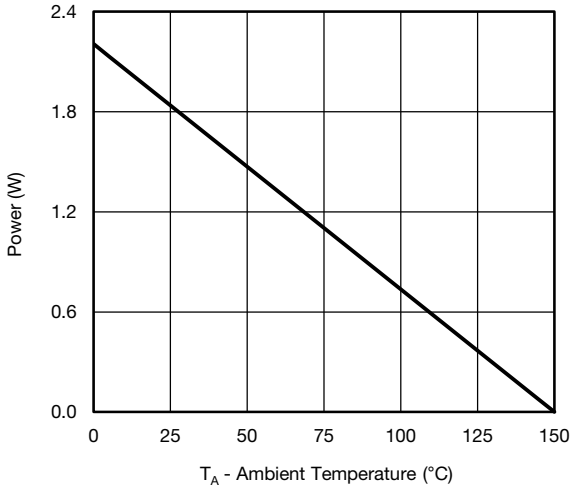
Safe Operating Area, Junction-to-Ambient



Current Derating*



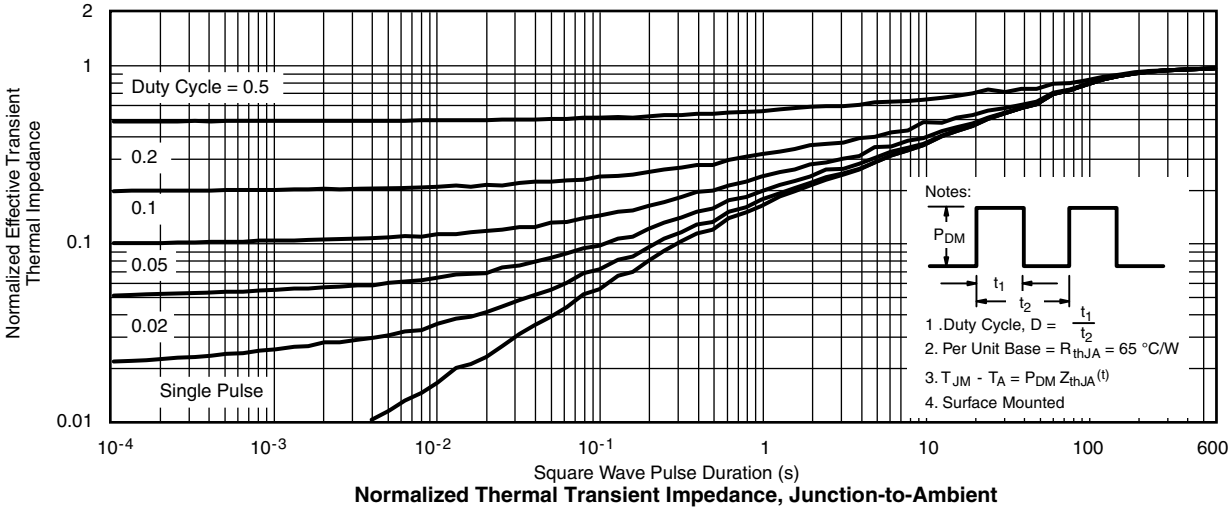
Power Junction-to-Case



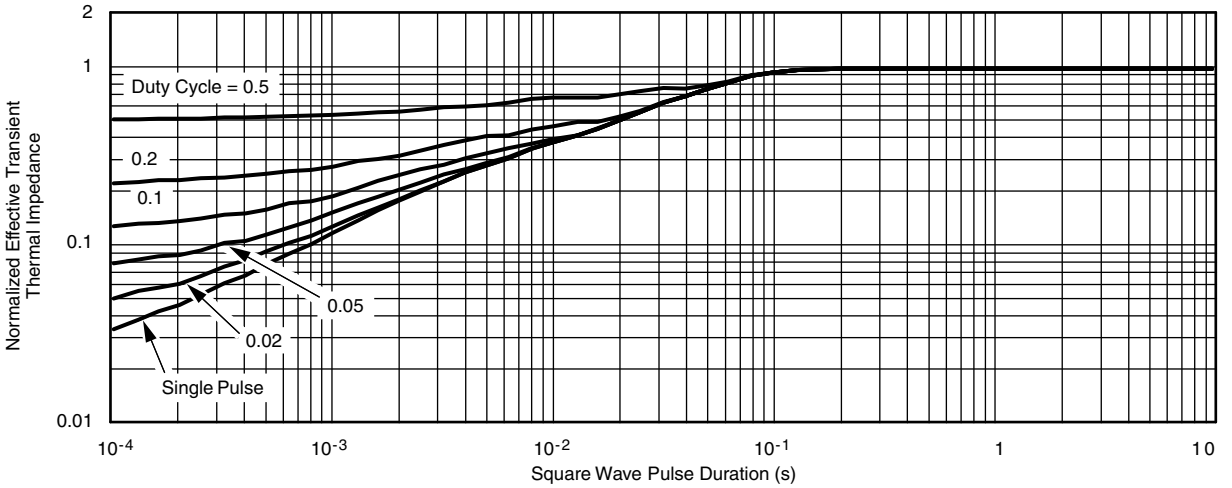
Power Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



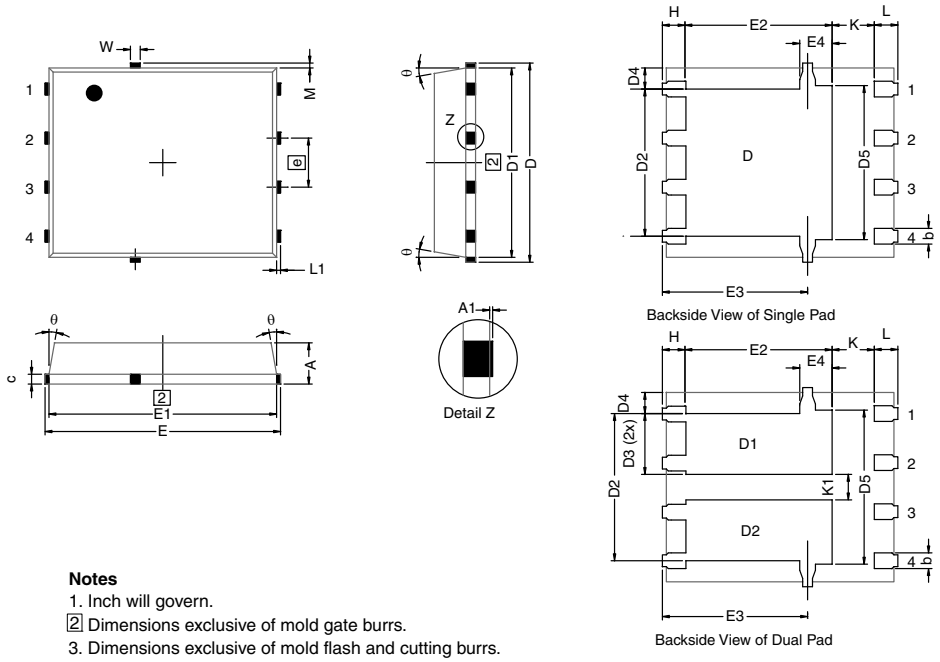
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?66744.

PowerPAK® SO-8, (Single/Dual)

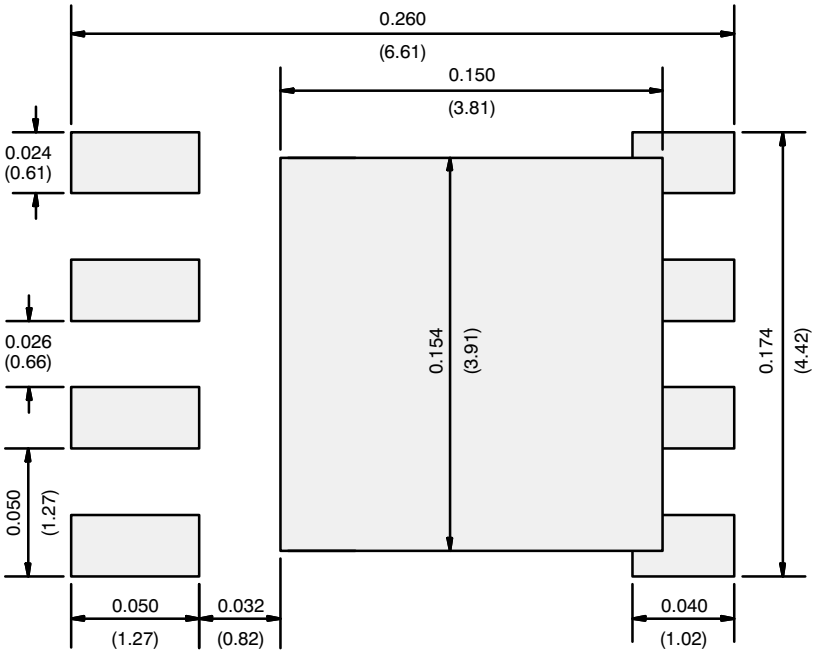


Notes

1. Inch will govern.
2. Dimensions exclusive of mold gate burrs.
3. Dimensions exclusive of mold flash and cutting burrs.

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1		-	0.05	0	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4		0.57 typ.			0.0225 typ.	
D5		3.98 typ.			0.157 typ.	
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2 (for AL product)	3.30	3.48	3.66	0.130	0.137	0.144
E2 (for other product)	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4 (for AL product)		0.58 typ.			0.023 typ.	
E4 (for other product)		0.75 typ.			0.030 typ.	
e		1.27 BSC			0.050 BSC	
K (for AL product)		1.45 typ.			0.057 typ.	
K (for other product)		1.27 typ.			0.050 typ.	
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	0.028
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M		0.125 typ.			0.005 typ.	
ECN: C13-0702-Rev. K, 20-May-13 DWG: 5881						

RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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