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REVISION HISTORY

5/04—Data Sheet Changed from Rev. E to Rev. F.

Changes to Specifications	2
Replaced Figure 18	10
Updated Outline Dimensions	16
Changes to Ordering Guide	16

4/03—Data Sheet Changed from Rev. D to Rev. E.

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11/02—Data Sheet Changed from Rev. C to Rev. D.

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SPECIFICATIONS

Table 1. @25°C ±5 V supplies, ac-coupled with 1 kHz sine wave input applied, unless otherwise noted. Specifications in bold are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Parameter	Conditions	AD736J/AD736A			AD736K/AD736B			Unit
		Min	Typ	Max	Min	Typ	Max	
TRANSFER FUNCTION		$V_{OUT} = \sqrt{\text{Avg}(V_{IN}^2)}$						
CONVERSION ACCURACY	1 kHz sine wave							
Total Error, Internal Trim ¹	Using C _c							
All Grades	0 mV rms–200 mV rms		0.3/0.3	0.5/0.5		0.2/0.2	0.3/0.3	±mV/±% of Reading
	200 mV to 1 V rms		–1.2	±2.0		–1.2	±2.0	% of Reading
T _{MIN} to T _{MAX}								
A and B Grades	@ 200 mV rms		0.7/0.7				0.5/0.5	±mV/±% of Reading
J and K Grades	@ 200 mV rms		0.007			0.007		±% of Reading/°C
vs. Supply Voltage								
@ 200 mV rms Input	V _S = ±5 V to ±16.5 V	0	+0.06	+0.1	0	+0.06	+0.1	%/V
	V _S = ±5 V to ±3 V	0	–0.18	–0.3	0	–0.18	–0.3	%/V
DC Reversal Error, DC-Coupled	@ 600 mV dc		1.3	2.5		1.3	2.5	% of Reading
Nonlinearity ² , 0 mV–200 mV	@ 100 mV rms	0	0.25	0.35	0	0.25	0.35	% of Reading
Total Error, External Trim	0 mV rms–200 mV rms		0.1/0.5			0.1/0.3		±mV/±% of Reading
ERROR VS. CREST FACTOR ³								
Crest Factor = 1 to 3	C _{AV} , C _F = 100 μF		0.7			0.7		% Additional Error
Crest Factor = 5	C _{AV} , C _F = 100 μF		2.5			2.5		% Additional Error
INPUT CHARACTERISTICS								
High Impedance Input (Pin 2)								
Signal Range								
Continuous rms Level	V _S = +2.8 V, –3.2 V			200			200	mV rms
	V _S = ±5 V to ±16.5 V			1			1	V rms
Peak Transient Input	V _S = +2.8 V, –3.2 V	±0.9			±0.9			V
	V _S = ±5 V		±2.7			±2.7		V
	V _S = ±16.5 V	±4.0			±4.0			V
Input Resistance			10 ¹²			10 ¹²		Ω
Input Bias Current	V _S = ±3 V to ±16.5 V		1	25		1	25	pA
Low Impedance Input (Pin 1)								
Signal Range								
Continuous rms Level	V _S = +2.8 V, –3.2 V			300			300	mV rms
	V _S = ±5 V to ±16.5 V			1			1	V rms
Peak Transient Input	V _S = +2.8 V, –3.2 V		±1.7			±1.7		V
	V _S = ±5 V		±3.8			±3.8		V
	V _S = ±16.5 V		±11			±11		V
Input Resistance		6.4	8	9.6	6.4	8	9.6	kΩ
Maximum Continuous Nondestructive Input	All supply voltages			±12			±12	V p-p
Input Offset Voltage ⁴								
J and K Grades				±3			±3	mV
A and B Grades				±3			±3	mV
vs. Temperature			8	30		8	30	μV/°C
vs. Supply	V _S = ±5 V to ±16.5 V		50	150		50	150	μV/V
	V _S = ±5 V to ±3 V		80			80		μV/V

¹ Accuracy is specified with the AD736 connected as shown in Figure 18 with capacitor C_c.

²Nonlinearity is defined as the maximum deviation (in percent error) from a straight line connecting the readings at 0 mV rms and 200 mV rms. Output offset voltage is adjusted to zero.

³Error versus crest factor is specified as additional error for a 200 mV rms signal. Crest factor = V_{PEAK}/V rms.

⁴ DC offset does not limit ac resolution.

AD736

Parameter	Conditions	AD736J/AD736A			AD736K/AD736B			Unit
		Min	Typ	Max	Min	Typ	Max	
OUTPUT CHARACTERISTICS								
Output Offset Voltage								
J and K Grades			±0.1	±0.5		±0.1	±0.3	mV
A and B Grades				±0.5			±0.3	mV
vs. Temperature			1	20		1	20	μV/°C
vs. Supply	V _S = ±5 V to ±16.5 V		50	130		50	130	μV/V
	V _S = ±5 V to ±3 V		50			50		μV/V
Output Voltage Swing								
2 kΩ Load	V _S = +2.8 V, −3.2 V	0–1.6	1.7		0–1.6	1.7		V
	V _S = ±5 V	0–3.6	3.8		0–3.6	3.8		V
	V _S = ±16.5 V	0–4	5		0–4	5		V
No Load	V _S = ±16.5 V	0–4	12		0–4	12		V
Output Current		2			2			mA
Short-Circuit Current			3			3		mA
Output Resistance	@ dc		0.2			0.2		Ω
FREQUENCY RESPONSE								
High Impedance Input (Pin 2) for 1% Additional Error	Sine wave input							
V _{IN} = 1 mV rms			1			1		kHz
V _{IN} = 10 mV rms			6			6		kHz
V _{IN} = 100 mV rms			37			37		kHz
V _{IN} = 200 mV rms			33			33		kHz
±3 dB Bandwidth	Sine wave input							
V _{IN} = 1 mV rms			5			5		kHz
V _{IN} = 10 mV rms			55			55		kHz
V _{IN} = 100 mV rms			170			170		kHz
V _{IN} = 200 mV rms			190			190		kHz
Low Impedance Input (Pin 1) for 1% Additional Error	Sine wave input							
V _{IN} = 1 mV rms			1			1		kHz
V _{IN} = 10 mV rms			6			6		kHz
V _{IN} = 100 mV rms			90			90		kHz
V _{IN} = 200 mV rms			90			90		kHz
±3 dB Bandwidth	Sine wave input							
V _{IN} = 1 mV rms			5			5		kHz
V _{IN} = 10 mV rms			55			55		kHz
V _{IN} = 100 mV rms			350			350		kHz
V _{IN} = 200 mV rms			460			460		kHz
POWER SUPPLY								
Operating Voltage Range		+2.8, −3.2 ±5	±16.5		+2.8, −3.2 ±5	±16.5		V
Quiescent Current	Zero signal	160	200		160	200		μA
200 mV rms, No Load	Sine wave input	230	270		230	270		μA
TEMPERATURE RANGE								
Operating, Rated Performance								
Commercial	0°C to 70°C	AD736JN, AD736JR			AD736KN, AD736KR			
Industrial	−40°C to +85°C	AD736AQ, AD736AR			AD736BQ, AD736BR			

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	± 16.5 V
Internal Power Dissipation ⁵	200 mW
Input Voltage	$\pm V_S$
Output Short-Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range (Q)	-65°C to $+150^{\circ}\text{C}$
Storage Temperature Range (N, R)	-65°C to $+125^{\circ}\text{C}$
Lead Temperature Range (Soldering 60 sec)	300°C
ESD Rating	500 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

⁵ 8-Lead PDIP Package: $\theta_{JA} = 165^{\circ}\text{C/W}$
 8-Lead CERDIP Package: $\theta_{JA} = 110^{\circ}\text{C/W}$
 8-Lead SOIC Package: $\theta_{JA} = 155^{\circ}\text{C/W}$

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

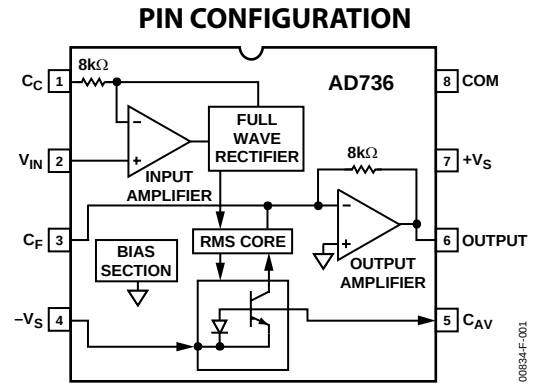


Figure 2. Pin Configuration for 8-Lead PDIP (N-8), 8-Lead SOIC (RN-8), and 8-Lead CERDIP (Q-8) Packages



TYPICAL PERFORMANCE CHARACTERISTICS

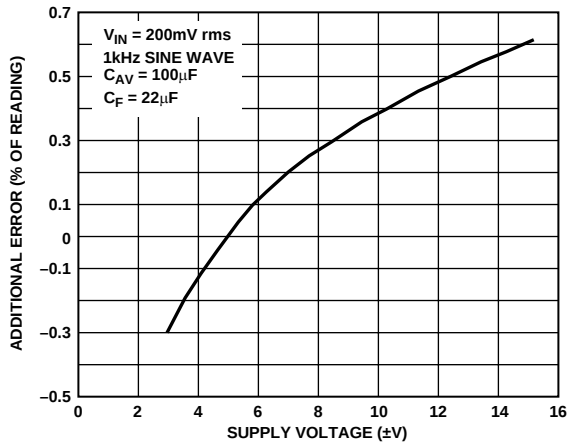


Figure 3. Additional Error vs. Supply Voltage

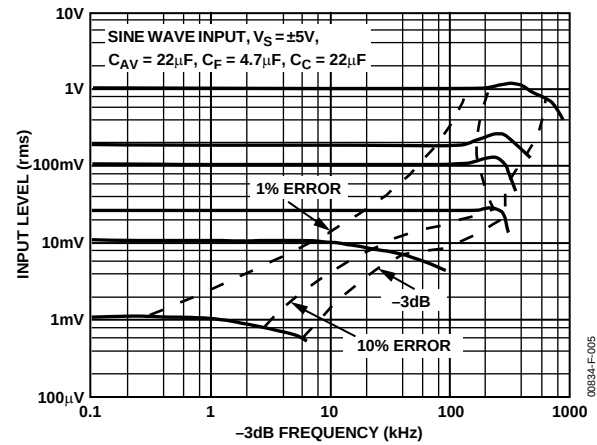


Figure 6. Frequency Response Driving Pin 1

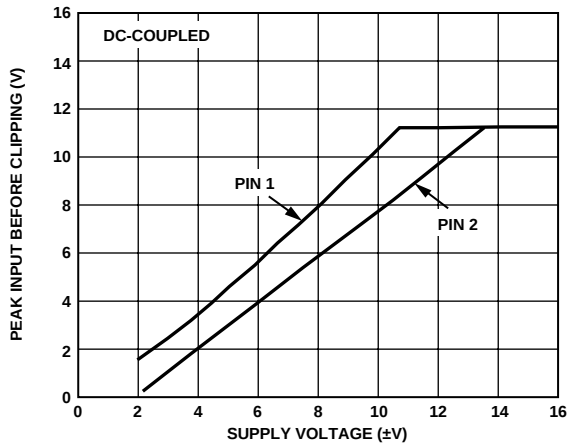


Figure 4. Maximum Input Level vs. Supply Voltage

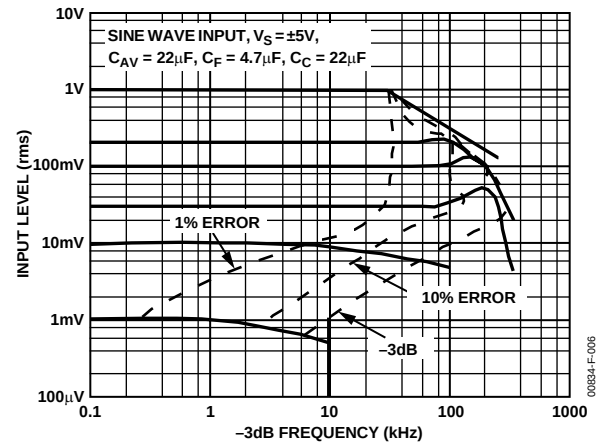


Figure 7. Frequency Response Driving Pin 2

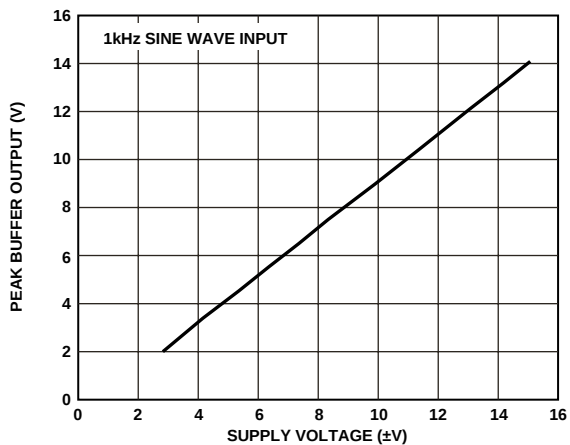
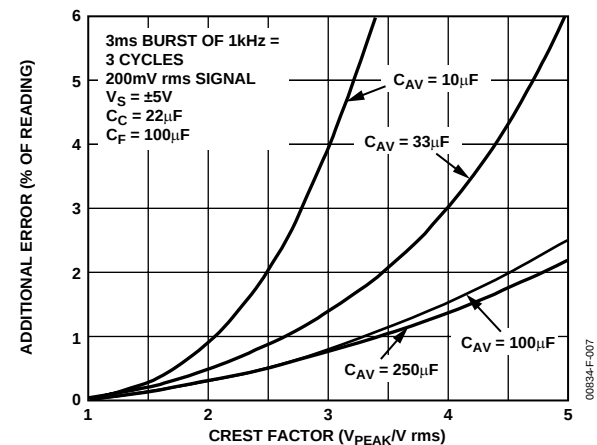


Figure 5. Peak Buffer Output vs. Supply Voltage

Figure 8. Additional Error vs. Crest Factor vs. C_{AV}

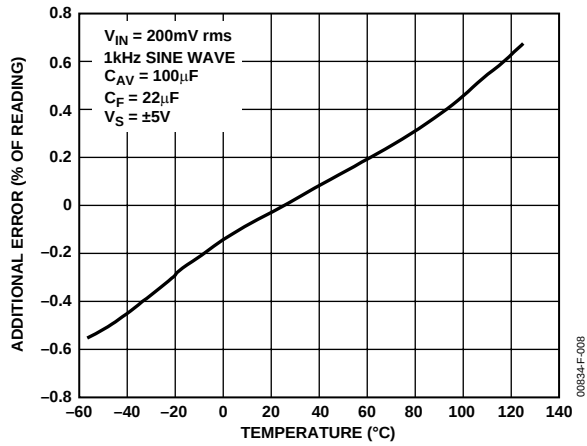


Figure 9. Additional Error vs. Temperature

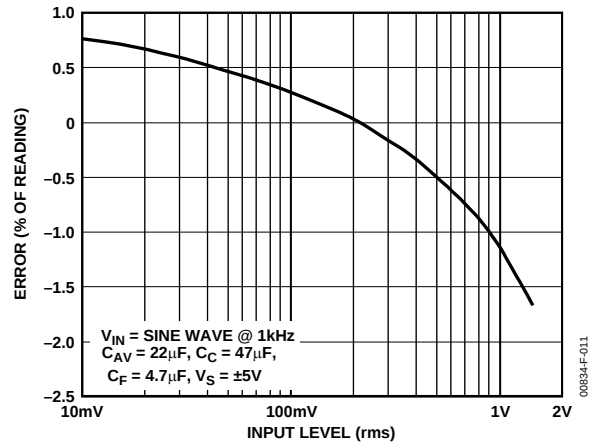


Figure 12. Error vs. RMS Input Voltage (Pin 2), Output Buffer Offset Is Adjusted to Zero

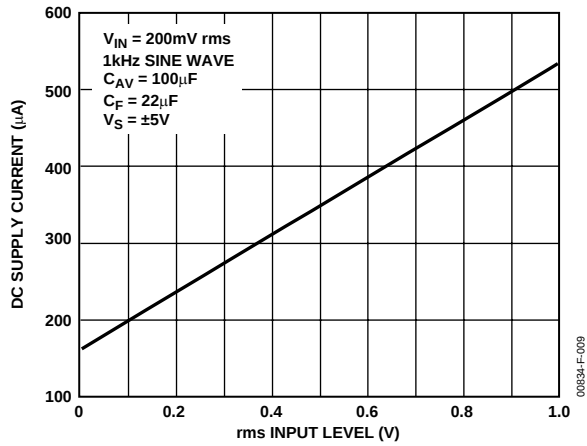


Figure 10. DC Supply Current vs. RMS Input Level

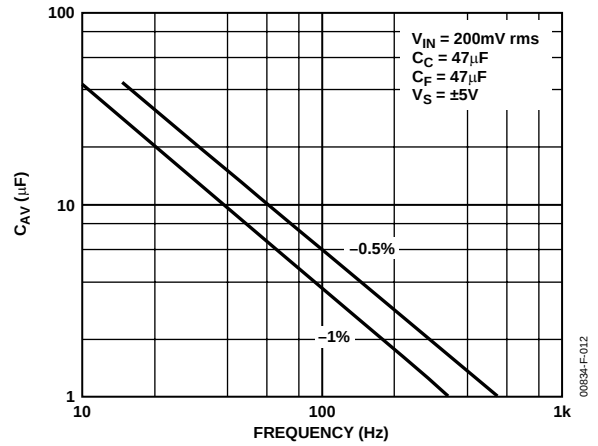


Figure 13. C_{AV} vs. Frequency for Specified Averaging Error

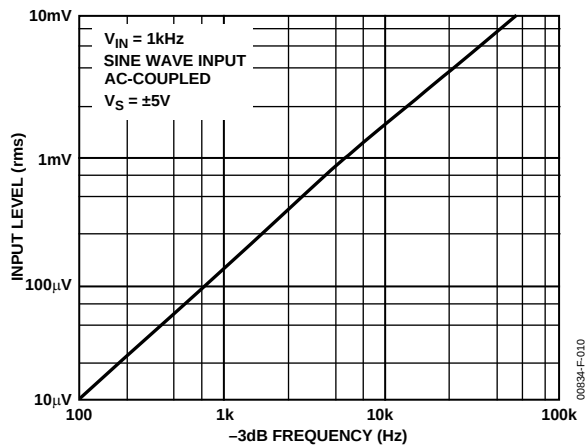


Figure 11. -3 dB Frequency vs. RMS Input Level (Pin 2)

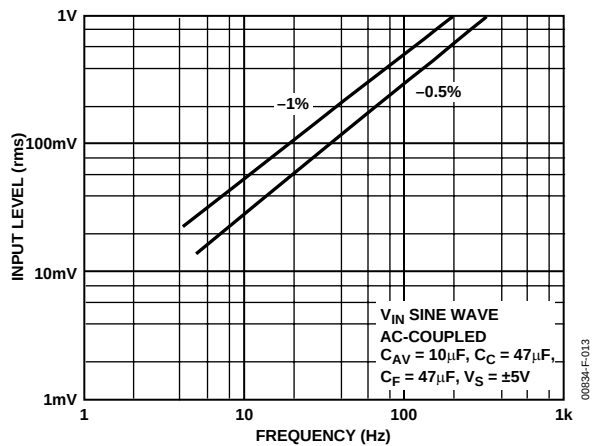


Figure 14. RMS Input Level vs. Frequency for Specified Averaging Error

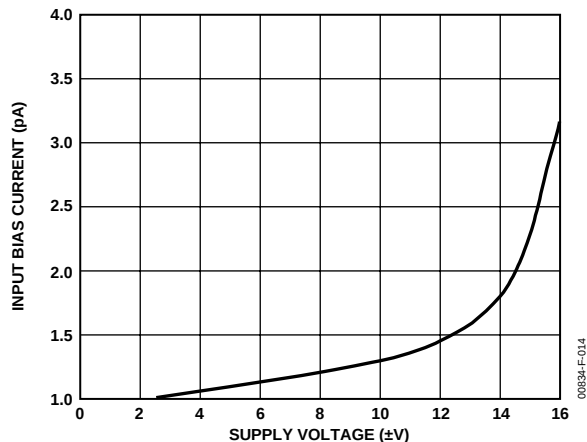


Figure 15. Pin 2 Input Bias Current vs. Supply Voltage

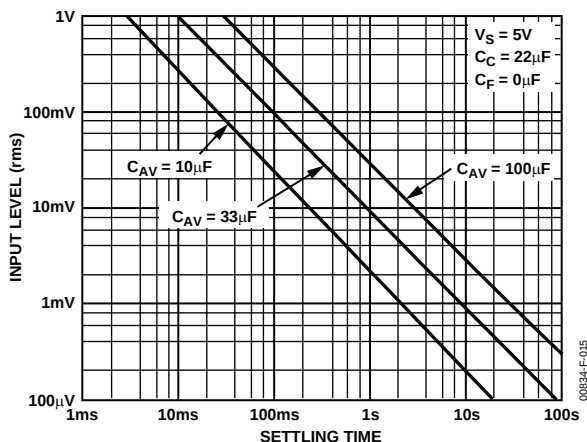
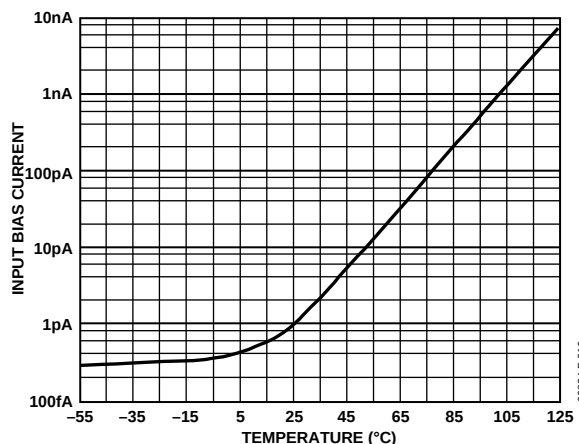
Figure 16. Settling Time vs. RMS Input Level for Various Values of C_{AV} 

Figure 17. Pin 2 Input Bias Current vs. Temperature

CALCULATING SETTTLING TIME USING FIGURE 16

Figure 16 may be used to closely approximate the time required for the AD736 to settle when its input level is reduced in amplitude. The net time required for the rms converter to settle is the difference between two times extracted from the graph—the initial time minus the final settling time. As an example, consider the following conditions: a 33 μF averaging capacitor, a 100 mV initial rms input level, and a final (reduced) 1 mV input level. From Figure 16, the initial settling time (where the 100 mV line intersects the 33 μF line) is approximately 80 ms.

The settling time corresponding to the new or final input level of 1 mV is approximately 8 seconds. Therefore, the net time for the circuit to settle to its new value is 8 seconds minus 80 ms, which is 7.92 seconds. Note that because of the smooth decay characteristic inherent with a capacitor/diode combination, this is the total settling time to the final value (i.e., not the settling time to 1%, 0.1%, and so on, of the final value). Also, this graph provides the worst-case settling time since the AD736 settles very quickly with increasing input levels.

TYPES OF AC MEASUREMENT

The AD736 is capable of measuring ac signals by operating as either an average responding converter or a true rms-to-dc converter. As its name implies, an average responding converter computes the average absolute value of an ac (or ac and dc) voltage or current by full-wave rectifying and low-pass filtering the input signal; this approximates the average. The resulting output, a dc average level, is then scaled by adding (or reducing) gain; this scale factor converts the dc average reading to an rms equivalent value for the waveform being measured. For example, the average absolute value of a sine wave voltage is 0.636 times that of V_{PEAK} ; the corresponding rms value is 0.707 times V_{PEAK} . Therefore, for sine wave voltages, the required scale factor is 1.11 (0.707 divided by 0.636).

In contrast to measuring the average value, true rms measurement is a universal language among waveforms, allowing the magnitudes of all types of voltage (or current) waveforms to be compared to one another and to dc. RMS is a direct measure of the power or heating value of an ac voltage compared to that of a dc voltage; an ac signal of 1 V rms produces the same amount of heat in a resistor as a 1 V dc signal.

Mathematically, the rms value of a voltage is defined (using a simplified equation) as

$$V_{rms} = \sqrt{\text{Avg}(V^2)}$$

This involves squaring the signal, taking the average, and then obtaining the square root. True rms converters are smart rectifiers; they provide an accurate rms reading regardless of the type of waveform being measured. However, average responding converters can exhibit very high errors when their input signals deviate from their precalibrated waveform; the magnitude of the error depends on the type of waveform being measured. For example, if an average responding converter is calibrated to measure the rms value of sine wave voltages and is then used to measure either symmetrical square waves or dc voltages, the converter will have a computational error 11% (of reading) higher than the true rms value (see Table 3).

Table 3. Error Introduced by an Average Responding Circuit when Measuring Common Waveforms

Waveform Type 1 V Peak Amplitude	Crest Factor (V_{PEAK}/V_{rms})	True rms Value (V)	Average Responding Circuit Calibrated to Read RMS Value of Sine Waves Will Read (V)	% of Reading Error Using Average Responding Circuit
Undistorted Sine Wave	1.414	0.707	0.707	0
Symmetrical Square Wave	1.00	1.00	1.11	11.0
Undistorted Triangle Wave	1.73	0.577	0.555	-3.8
Gaussian Noise (98% of Peaks <1 V)	3	0.333	0.295	-11.4
Rectangular	2	0.5	0.278	-44
Pulse Train	10	0.1	0.011	-89
SCR Waveforms				
50% Duty Cycle	2	0.495	0.354	-28
25% Duty Cycle	4.7	0.212	0.150	-30

THEORY OF OPERATION

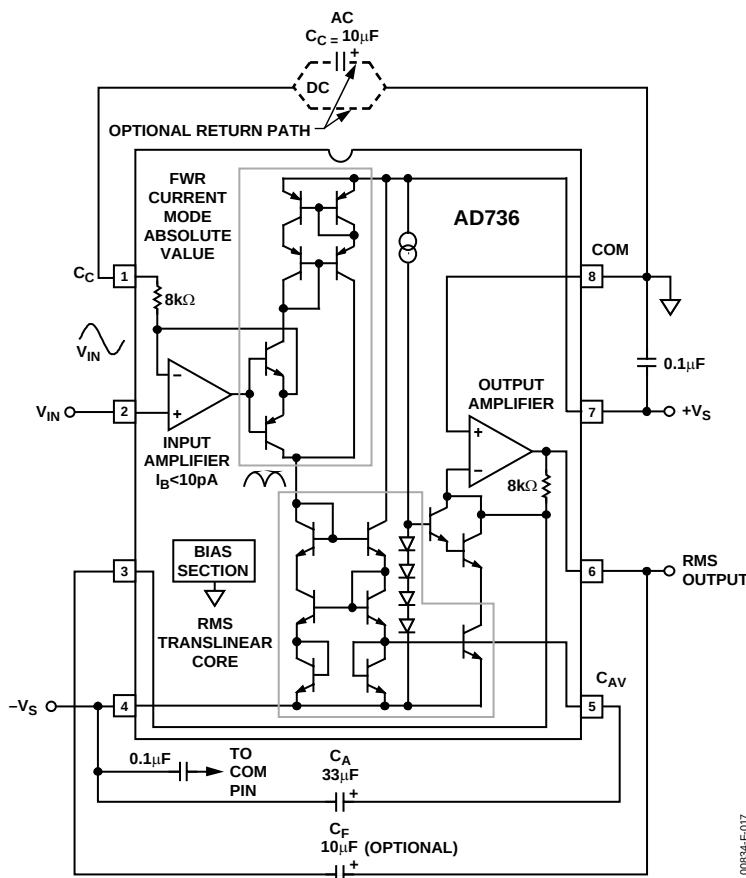


Figure 18. AD736 True RMS Circuit

As shown by Figure 18, the AD736 has five functional subsections: the input amplifier, full-wave rectifier (FWR), rms core, output amplifier, and bias section. The FET input amplifier allows both a high impedance, buffered input (Pin 2) and a low impedance, wide dynamic range input (Pin 1). The high impedance input, with its low input bias current, is well suited for use with high impedance input attenuators.

The output of the input amplifier drives a full-wave precision rectifier, which in turn drives the rms core. The essential rms operations of squaring, averaging, and square rooting are performed in the core, using an external averaging capacitor, C_{AV} . Without C_{AV} , the rectified input signal travels through the core unprocessed, as is done with the average responding connection (Figure 19).

A final subsection, an output amplifier, buffers the output from the core and allows optional low-pass filtering to be performed via the external capacitor, C_F , which is connected across the feedback path of the amplifier. In the average responding connection, this is where all of the averaging is carried out. In the rms circuit, this additional filtering stage helps reduce any output ripple that was not removed by the averaging capacitor, C_{AV} .

RMS MEASUREMENT—CHOOSING THE OPTIMUM VALUE FOR C_{AV}

Since the external averaging capacitor, C_{AV} , holds the rectified input signal during rms computation, its value directly affects the accuracy of the rms measurement, especially at low frequencies. Furthermore, because the averaging capacitor appears across a diode in the rms core, the averaging time constant increases exponentially as the input signal is reduced. This means that as the input level decreases, errors due to nonideal averaging decrease while the time required for the circuit to settle to the new rms level increases. Therefore, lower input levels allow the circuit to perform better (due to increased averaging) but increase the waiting time between measurements. Obviously, when selecting C_{AV} , a trade-off between computational accuracy and settling time is required.

Because the average responding connection shown in Figure 19 does not use the C_{AV} averaging capacitor, its settling time does not vary with input signal level. It is determined solely by the RC time constant of C_F and the internal 8 k Ω resistor in the output amplifier's feedback path.

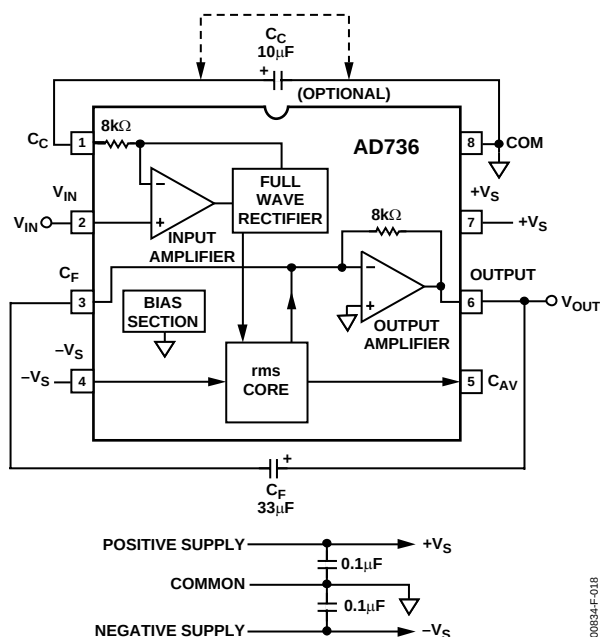


Figure 19. AD736 Average Responding Circuit

DC ERROR, OUTPUT RIPPLE, AND AVERAGING ERROR

Figure 20 shows the typical output waveform of the AD736 with a sine wave input applied. As with all real-world devices, the ideal output of $V_{OUT} = V_{IN}$ is never achieved exactly. Instead, the output contains both a dc and an ac error component.

As shown, the dc error is the difference between the average of the output signal (when all the ripple in the output has been removed by external filtering) and the ideal dc output. The dc error component is therefore set solely by the value of the averaging capacitor used—no amount of post filtering (i.e., using a very large C_F) will allow the output voltage to equal its ideal value. The ac error component, an output ripple, may be easily removed by using a large enough post-filtering capacitor, C_F .

In most cases, the combined magnitudes of both the dc and ac error components need to be considered when selecting appropriate values for capacitors C_{AV} and C_F . This combined error, representing the maximum uncertainty of the measurement, is termed the averaging error and is equal to the peak value of the output ripple plus the dc error.

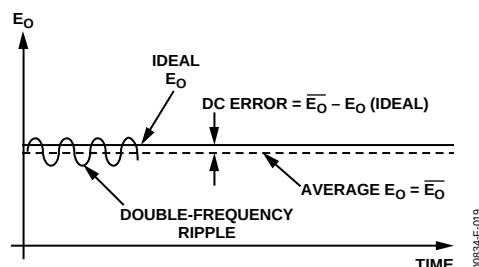


Figure 20. Output Waveform for Sine Wave Input Voltage

As the input frequency increases, both error components decrease rapidly; if the input frequency doubles, the dc error and ripple reduce to one quarter and one half of their original values, respectively, and rapidly become insignificant.

AC MEASUREMENT ACCURACY AND CREST FACTOR

The crest factor of the input waveform is often overlooked when determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the peak signal amplitude to the rms amplitude (crest factor = $V_{\text{PEAK}}/V_{\text{rms}}$). Many common waveforms, such as sine and triangle waves, have relatively low crest factors (≤ 2). Other waveforms, such as low duty cycle pulse trains and SCR waveforms, have high crest factors. These types of waveforms require a long averaging time constant (to average out the long time periods between pulses). Figure 8 shows the additional error versus the crest factor of the AD736 for various values of C_{AV} .

SELECTING PRACTICAL VALUES FOR INPUT COUPLING (C_C), AVERAGING (C_{AV}), AND FILTERING (C_F) CAPACITORS

Table 4 provides practical values of C_{AV} and C_F for several common applications.

The input coupling capacitor, C_C , in conjunction with the 8 k Ω internal input scaling resistor, determines the -3 dB low frequency roll-off. This frequency, F_L , is equal to

$$F_L = \frac{1}{2\pi(8,000)(\text{The Value of } C_C \text{ in Farads})}$$

Note that at F_L , the amplitude error is approximately -30% (-3 dB) of reading. To reduce this error to 0.5% of reading, choose a value of C_C that sets F_L at one-tenth of the lowest frequency to be measured.

In addition, if the input voltage has more than 100 mV of dc offset, then the ac-coupling network shown in Figure 23 should be used in addition to capacitor C_C .

AD736

Table 4. Capacitor Selection Chart

Application	RMS Input Level	Low Frequency Cutoff (–3 dB)	Max Crest Factor	C _{AV} (μF)	C _F (μF)	Settling Time ⁶ to 1%
General-Purpose rms Computation	0 V to 1 V	20 Hz	5	150	10	360 ms
		200 Hz	5	15	1	36 ms
	0 mV to 200 mV	20 Hz	5	33	10	360 ms
		200 Hz	5	3.3	1	36 ms
General-Purpose Average Responding	0 V to 1 V	20 Hz		None	33	1.2 sec
		200 Hz		None	3.3	120 ms
	0 mV to 200 mV	20 Hz		None	33	1.2 sec
		200 Hz		None	3.3	120 ms
SCR Waveform Measurement	0 mV to 200 mV	50 Hz	5	100	33	1.2 sec
		60 Hz	5	82	27	1.0 sec
	0 mV to 100 mV	50 Hz	5	50	33	1.2 sec
		60 Hz	5	47 μF	27 μF	1.0 sec
Audio Applications						
Speech	0 mV to 200 mV	300 Hz	3	1.5 μF	0.5 μF	18 ms
Music	0 mV to 100 mV	20 Hz	10	100 μF	68 μF	2.4 sec

⁶ Settling time is specified over the stated rms input level with the input signal increasing from zero. Settling times are greater for decreasing amplitude input signals.

APPLICATION CIRCUITS

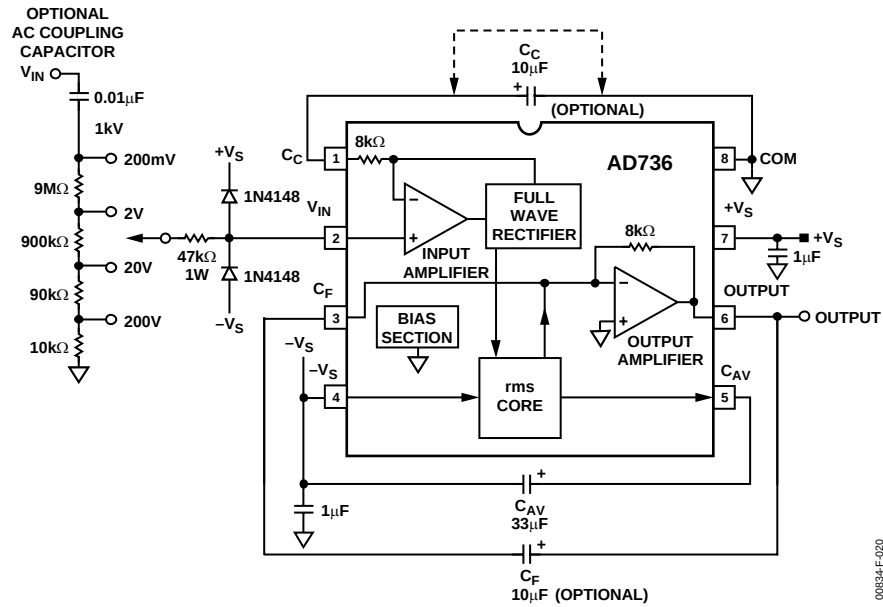


Figure 21. AD736 with a High Impedance Input Attenuator

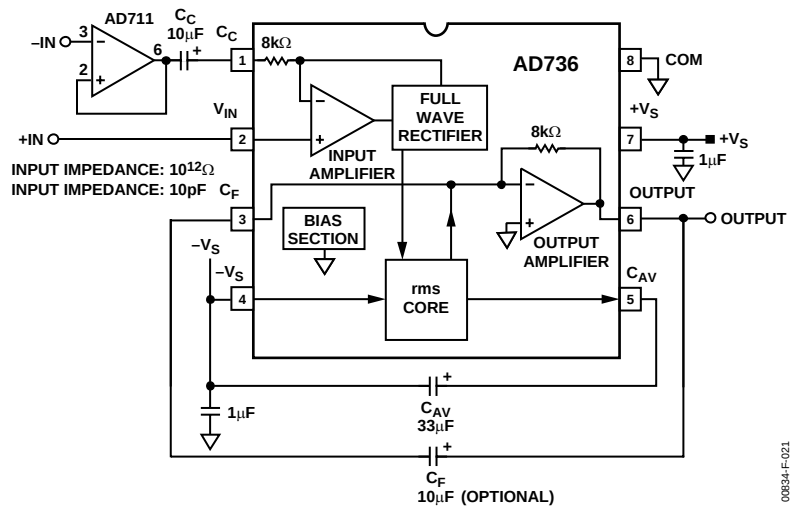


Figure 22. Differential Input Connection

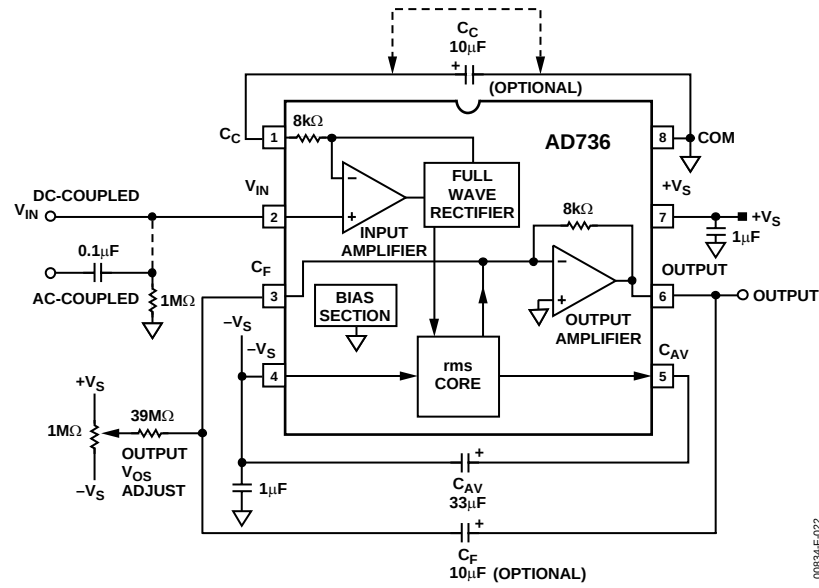


Figure 23. External Output V_{OS} Adjustment

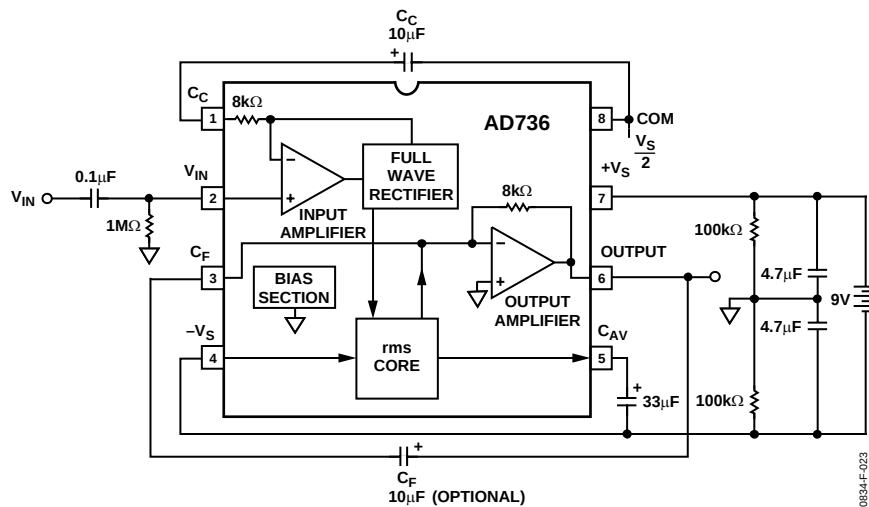


Figure 24. Battery-Powered Option

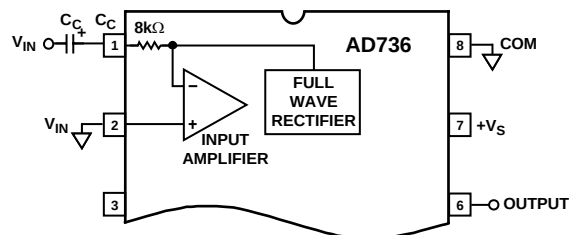
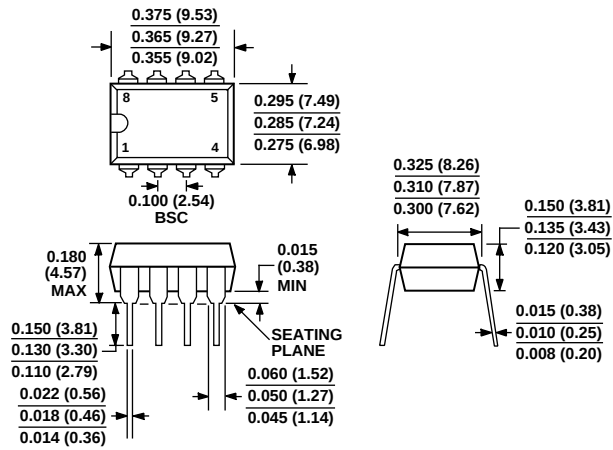


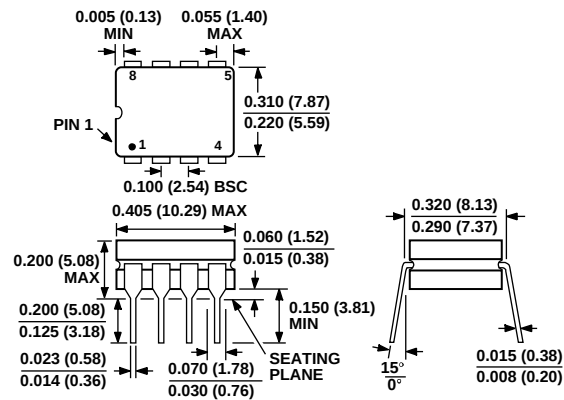
Figure 25. Low Z, AC-Coupled Input Connection

OUTLINE DIMENSIONS



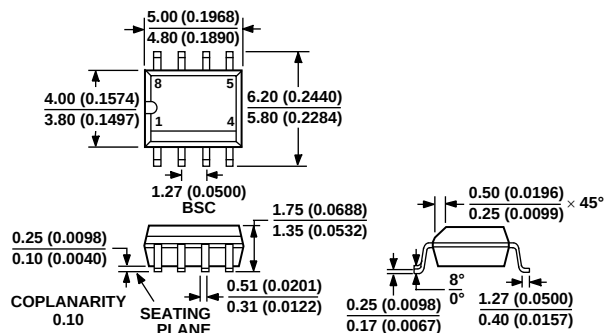
COMPLIANT TO JEDEC STANDARDS MO-095AA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 26. 8-Lead Plastic Dual In-Line Package [PDIP]
(N-8)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 27. 8-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 28. 8-Lead Standard Small Outline Package [SOIC] Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD736JN	0°C to +70°C	PDIP	N-8
AD736KN	0°C to +70°C	PDIP	N-8
AD736AQ	-40°C to +85°C	CERDIP	Q-8
AD736BQ	-40°C to +85°C	CERDIP	Q-8
AD736AR	-40°C to +85°C	SOIC	R-8
AD736AR-Reel	-40°C to +85°C	SOIC	R-8
AD736AR-Reel-7	-40°C to +85°C	SOIC	R-8
AD736BR	-40°C to +85°C	SOIC	R-8
AD736BR-Reel	-40°C to +85°C	SOIC	R-8
AD736BR-Reel-7	-40°C to +85°C	SOIC	R-8
AD736JR	0°C to +70°C	SOIC	R-8
AD736JR-Reel	0°C to +70°C	SOIC	R-8
AD736JR-Reel-7	0°C to +70°C	SOIC	R-8
AD736JRZ ¹	0°C to +70°C	SOIC	R-8
AD736JRZ-RL ¹	0°C to +70°C	SOIC	R-8
AD736JRZ-R7 ¹	0°C to +70°C	SOIC	R-8
AD736KR	0°C to +70°C	SOIC	R-8
AD736KR-Reel	0°C to +70°C	SOIC	R-8
AD736KR-Reel-7	0°C to +70°C	SOIC	R-8
AD736KRZ ¹	0°C to +70°C	SOIC	R-8
AD736KRZ-RL ¹	0°C to +70°C	SOIC	R-8
AD736KRZ-R7 ¹	0°C to +70°C	SOIC	R-8

¹ Z = Pb-Free Part.