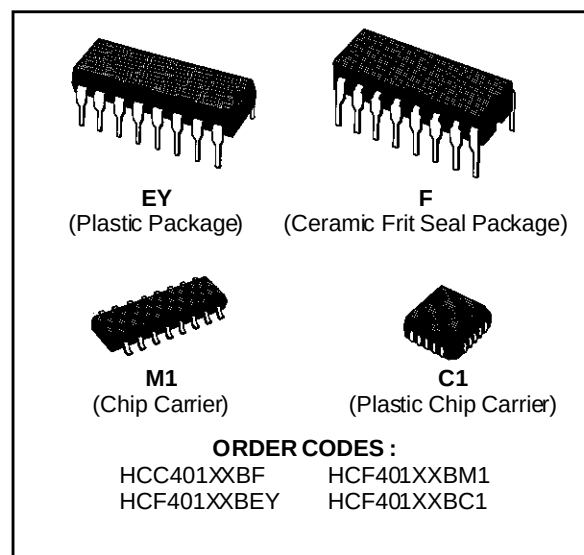


PRESETTABLE UP/DOWN COUNTERS (DUAL CLOCK WITH RESET) 40192B – BCD TYPE 40193B – BINARY TYPE

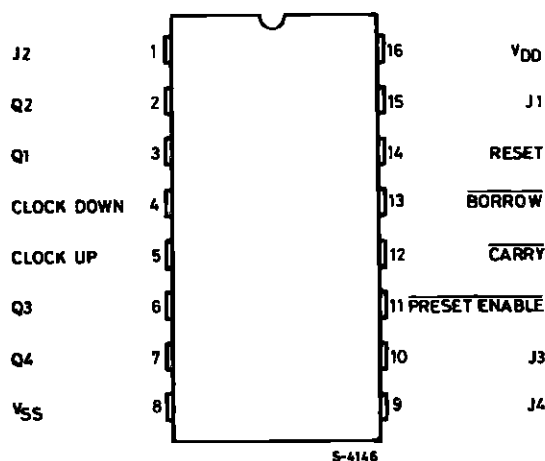
- INDIVIDUAL CLOCK LINES FOR COUNTING UP OR COUNTING DOWN
- SYNCHRONOUS HIGH-SPEED CARRY AND BORROW PROPAGATION DELAYS FOR CAS-CADING
- ASYNCHRONOUS RESET AND PRESET CAPABILITY
- MEDIUM-SPEED OPERATION - $f_{CL} = 8\text{MHz}$ (typ.) @ 10V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



DESCRIPTION

The **HCC40192B**, **HCC40193B**, (extended temperature range) and the **HCF40192B**, **HCF40193B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF40192B** Presettable BCD Up/Down Counter and the **HCC/HCF40193B** Presettable Binary Up/Down Counter each consist of 4 synchronously clocked, gated "D" type flip-flops connected as a counter. The inputs consist of 4 individual jam lines, a PRESET ENABLE control, individual CLOCK UP and CLOCK DOWN signals and a master RESET. Four buffered Q signal outputs as well as CARRY and BORROW outputs for multiple-stage counting schemes are provided. The counter is cleared so that all outputs are in a low state by a high on the RESET line. A RESET is accomplished asynchronously with the clock. Each output is individually programmable asynchronously with the clock to the level on the corresponding jam input when the PRESET ENABLE control is low. The counter counts up one count on the positive clock edge of the CLOCK UP signal provided the CLOCK DOWN line is high. The counter counts down one count on the positive clock edge of the CLOCK DOWN signal provided the CLOCK UP line

PIN CONNECTIONS

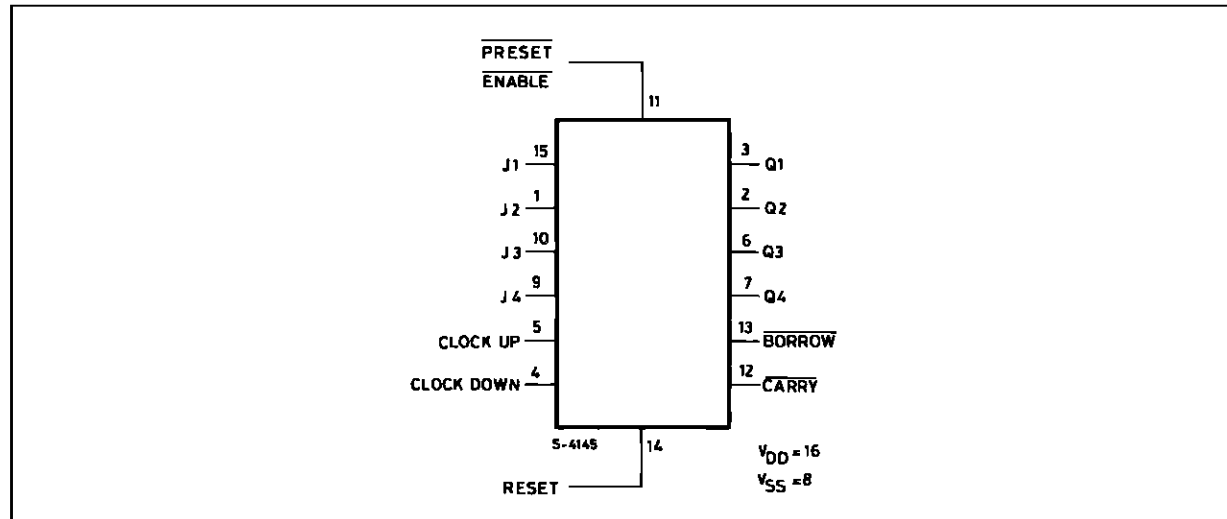


HCC/HCF40192B/193B

is high. The $\overline{\text{CARRY}}$ and $\overline{\text{BORROW}}$ signals are high when the counter is counting up or down. The CARRY signal goes low one-half clock cycle after the counter reaches its maximum count in the count-up mode. The BORROW signal goes low one-half clock cycle after the counter reaches its minimum

count in the count-down mode. Cascading of multiple packages is easily accomplished without the need for additional external circuitry by tying the BORROW and CARRY outputs to the CLOCK DOWN and CLOCK UP inputs, respectively, of the succeeding package.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}^*	Supply Voltage : HCC Types HCF Types	– 0.5 to + 20 – 0.5 to + 18	V V
V_i	Input Voltage	– 0.5 to $V_{DD} + 0.5$	V
I_i	DC Input Current (any one input)	± 10	mA
P_{tot}	Total Power Dissipation (per package)	200	mW
	Dissipation per Output Transistor for $T_{op} = \text{Full Package-temperature Range}$	100	mW
T_{op}	Operating Temperature : HCC Types HCF Types	– 55 to + 125 – 40 to + 85	°C °C
T_{stg}	Storage Temperature	– 65 to + 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltages are with respect to V_{SS} (GND).

RECOMMENDED OPERATING CONDITIONS

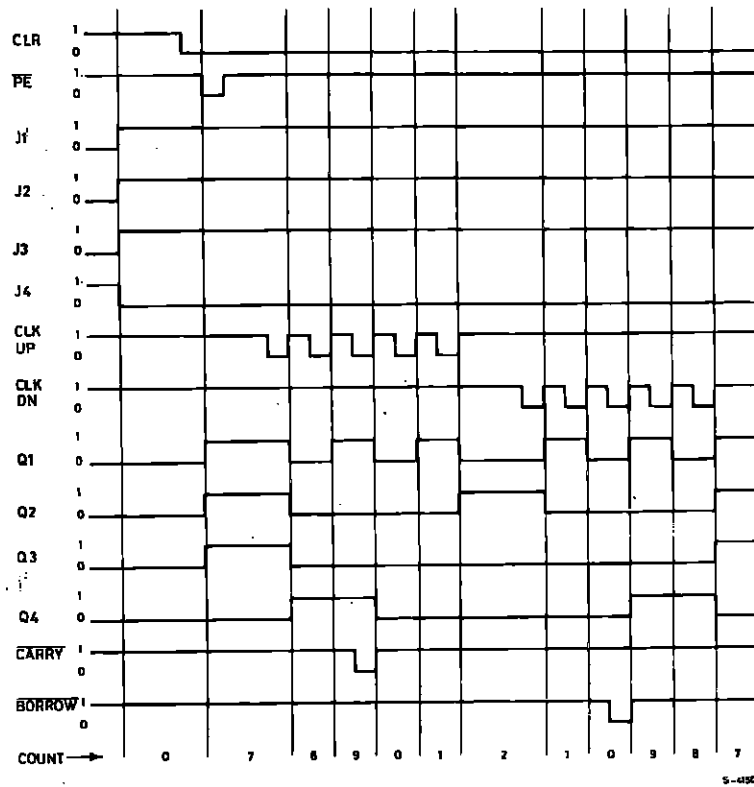
Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage : HCC Types HCF Types	3 to 18 3 to 15	V V
V_i	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature : HCC Types HCF Types	– 55 to + 125 – 40 to + 85	°C °C

Figure 1 is a schematic diagram of the control logic for the 4-bit ripple-carry adder. It shows the control logic (S1, S2, S3, S4) and the main adder logic (S1, S2, S3, S4) with inputs A, B, and C, and outputs S0, S1, S2, S3, S4. The control logic is labeled "CONTROL LOGIC 1" and "SAME AS CONTROL LOGIC 1".

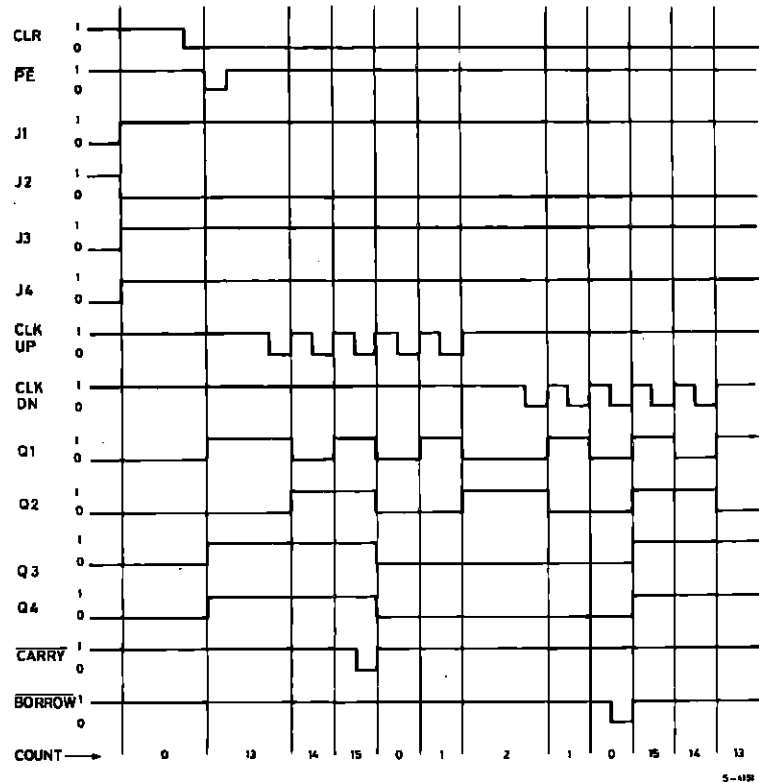
Figure 1 is a schematic diagram of the control logic for the 4-bit counter. It features four D-type flip-flops labeled S1, S2, S3, and S4, each with Set (S), Reset (R), Clock (C), and Data (D) inputs. The flip-flops are interconnected with a network of logic gates (AND, OR, NOT) to generate control signals. The outputs of the flip-flops are labeled S1, S2, S3, and S4. The counter is clocked by a 100 kHz signal, which is split into CLOCK UP and CLOCK DOWN signals. A RESET input is also shown. The counter's output is labeled CARRY. The diagram is labeled "CONTROL LOGIC 1".

TIMING DIAGRAMS

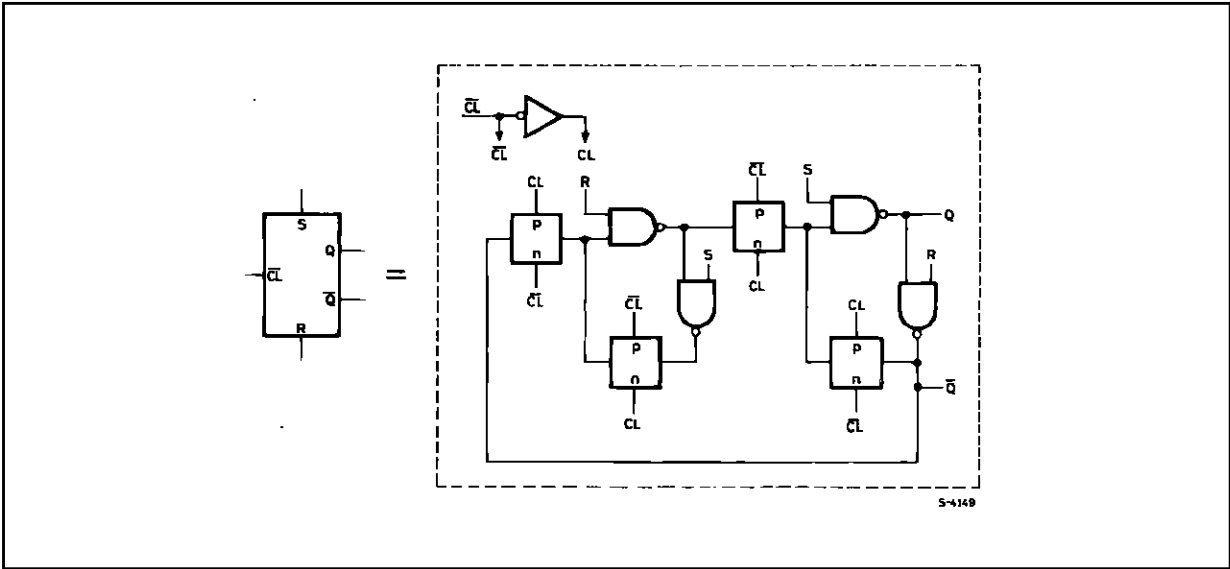
40192B (BCD).



40193B (Binary).



Internal Logic of Flip-flop.



TRUTH TABLE

Clock Up	Clock Down	<u>Preset</u> <u>Enable</u>	Reset	Action
	1	1	0	Count Up
	1	1	0	No Count
1		1	0	Count Down
1		1	0	No Count
X	X	0	0	Preset
X	X	X	1	Reset

1 = High Level 0 = Low Level X = Don't Care.

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

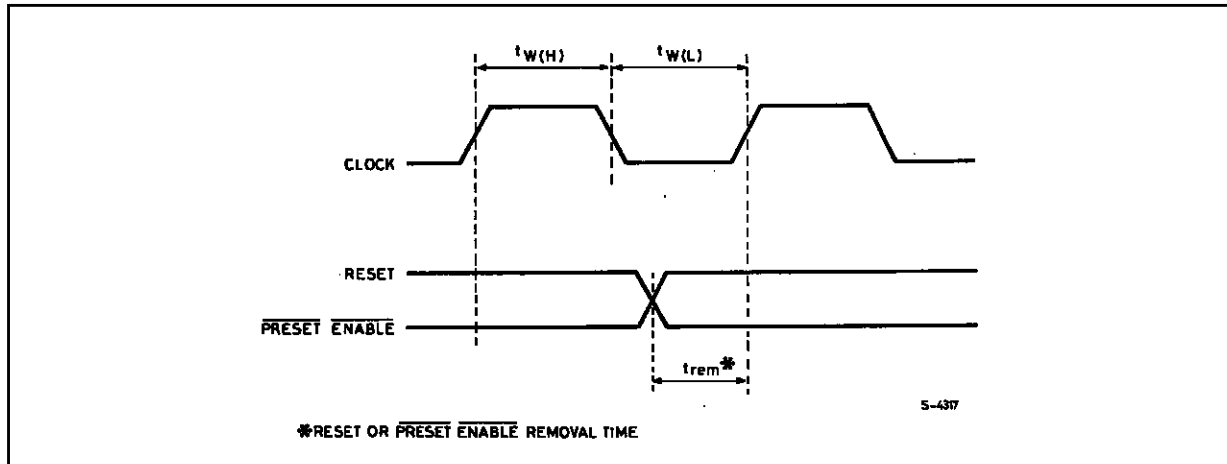
Symbol	Parameter		Test Conditions				Value						Unit	
			V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)	T _{Low} *		25°C			T _{High} *		
							Min.	Max.	Min.	Typ.	Max.	Min.		Max.
I _L	Quiescent Current	HCC Types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF Types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V _{OH}	Output High Voltage	0/ 5		< 1	5	4.95		4.95			4.95		V	
		0/10		< 1	10	9.95		9.95			9.95			
		0/15		< 1	15	14.95		14.95			14.95			
V _{OL}	Output Low Voltage	5/0		< 1	5		0.05			0.05		0.05	V	
		10/0		< 1	10		0.05			0.05		0.05		
		15/0		< 1	15		0.05			0.05		0.05		
V _{IH}	Input High Voltage		0.5/4.5	< 1	5	3.5		3.5			3.5		V	
			1/9	< 1	10	7		7			7			
			1.5/13.5	< 1	15	11		11			11			
V _{IL}	Input Low Voltage		4.5/0.5	< 1	5		1.5			1.5		1.5	V	
			9/1	< 1	10		3			3		3		
			13.5/1.5	< 1	15		4			4		4		
I _{OH}	Output Drive Current	HCC Types	0/ 5	2.5		5	– 2		– 1.6	– 3.2		– 1.15		mA
			0/ 5	4.6		5	– 0.64		– 0.51	– 1		– 0.36		
			0/10	9.5		10	– 1.6		– 1.3	– 2.6		– 0.9		
			0/15	13.5		15	– 4.2		– 3.4	– 6.8		– 2.4		
		HCF Types	0/ 5	2.5		5	– 1.53		– 1.36	– 3.2		– 1.1		
			0/ 5	4.6		5	– 0.52		– 0.44	– 1		– 0.36		
			0/10	9.5		10	– 1.3		– 1.1	– 2.6		– 0.9		
			0/15	13.5		15	– 3.6		– 3.0	– 6.8		– 2.4		
I _{OL}	Output Sink Current	HCC Types	0/ 5	0.4		5	0.64		0.51	1		0.36	mA	
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF Types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I _{IH} , I _{IL}	Input Leakage Current	HCC Types	0/18	Any Input	18		± 0.1		±10 ^{–5}	± 0.1		± 1	μA	
		HCF Types	0/15		15		± 0.3		±10 ^{–5}	± 0.3		± 1		
C _I	Input Capacitance			Any Input					5	7.5			pF	

* T_{Low} = - 55°C for **HCC** device : - 40°C for **HCF** device.* T_{High} = + 125°C for **HCC** device : + 85°C for **HCF** device.The Noise Margin for both "1" and "0" level is : 1V min. with V_{DD} = 5V, 2V min. with V_{DD} = 10V, 2.5V min. with V_{DD} =

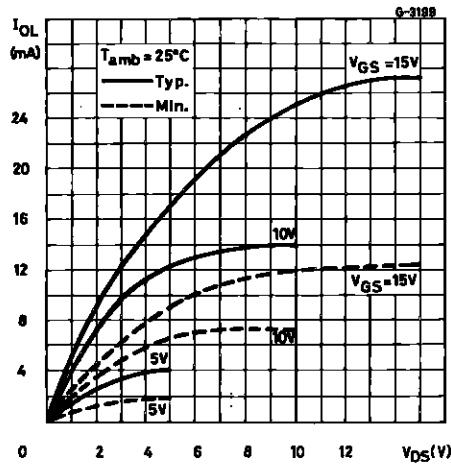
DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $C_L = 50\text{pF}$, $R_L = 200\text{k}\Omega$, typical temperature coefficient for all V_{DD} values is $0.3\%/^{\circ}\text{C}$, all input rise and fall time = 20ns)

Symbol	Parameter	Test Conditions		Value			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL} , t_{PLH}	Propagation Delay Time Clock Up or Clock Down to Q Reset to Q		5		250	500	ns
			10		120	240	
			15		90	180	
	$\overline{PE}$ to Q		5		200	400	ns
			10		100	200	
			15		70	140	
	Clock Up to $\overline{Carry}$ Clock Down to $\overline{Borrow}$		5		160	320	ns
			10		80	160	
			15		60	120	
	$\overline{Reset}$ or $\overline{PR}$ to $\overline{Borrow}$ or $\overline{Carry}$		5		300	600	ns
			10		150	300	
			15		110	220	
t_{THL} , t_{TLH}	Transition Time		5		100	200	ns
			10		50	100	
			15		40	80	
t_{rem}^*	Removal Time Reset or $\overline{PE}$		5	80	40		ns
			10	40	20		
			15	30	15		
t_w	Clock Input Pulse Width Reset		5	480	240		ns
			10	300	150		
			15	260	130		
	$\overline{PE}$		5		120	240	ns
			10		85	170	
			15		70	140	
	Clock		5		90	180	ns
			10		45	90	
			15		30	60	
t_r , t_f	Clock Input Rise or Fall Time		5			15	μs
			10			15	
			15			5	
f_{CL}	Maximum Clock Input Frequency		5	2	4		MHz
			10	5	8		
			15	5.5	11		

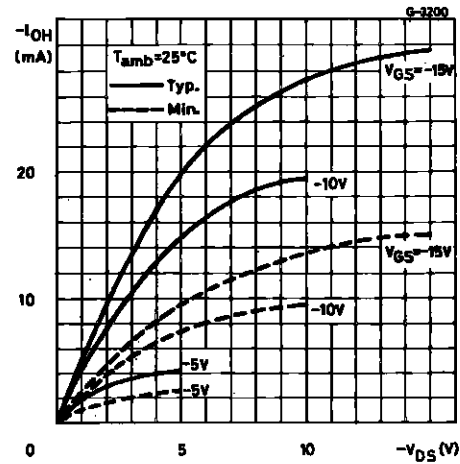
* The time required for Reset or Preset Enable control to be removed before clocking (see timing diagram).

Timing Diagram Defining t_{rem} .


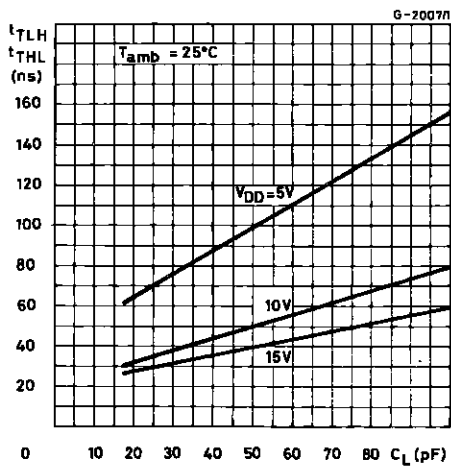
Output Low (sink) Current Characteristics.



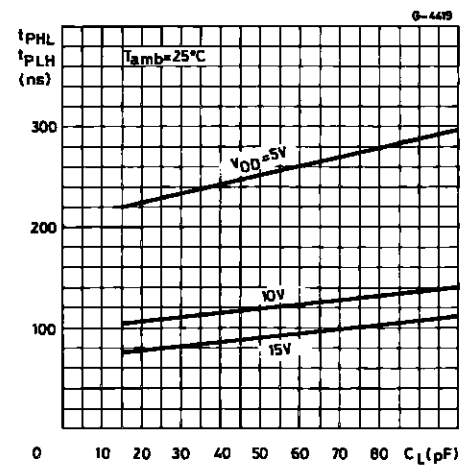
Output high (source) Current Characteristics.



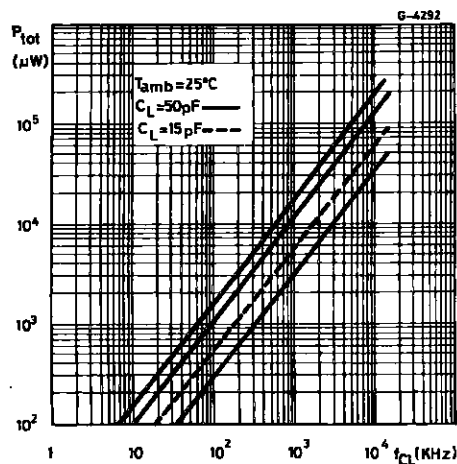
Typical Transition Time vs. Load Capacitance.



Typical Propagation Delay Time vs. Load Capacitance.

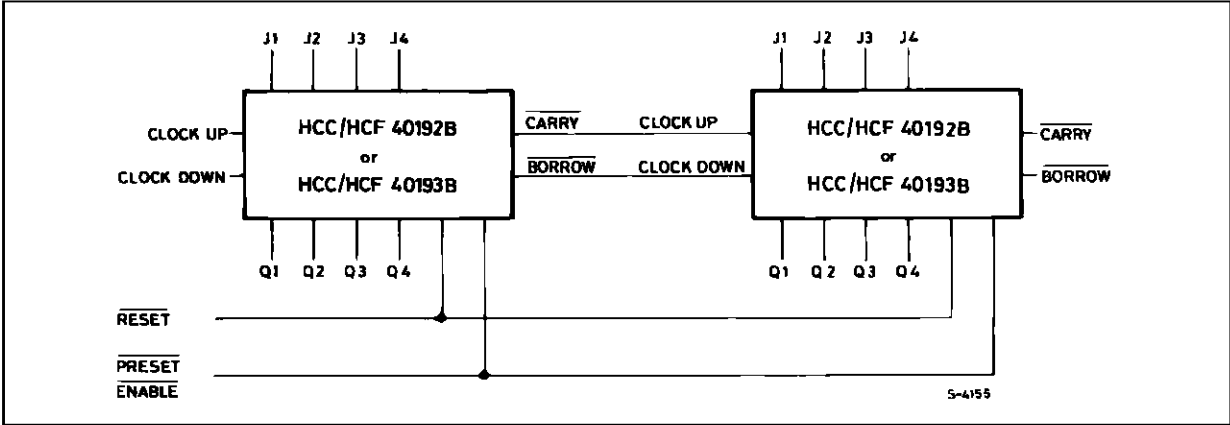


Typical Dynamic Power Dissipation.



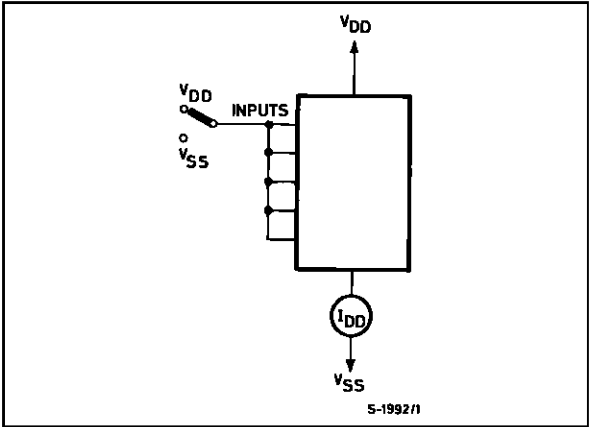
TYPICAL APPLICATION

CASCADED COUNTER PACKAGES

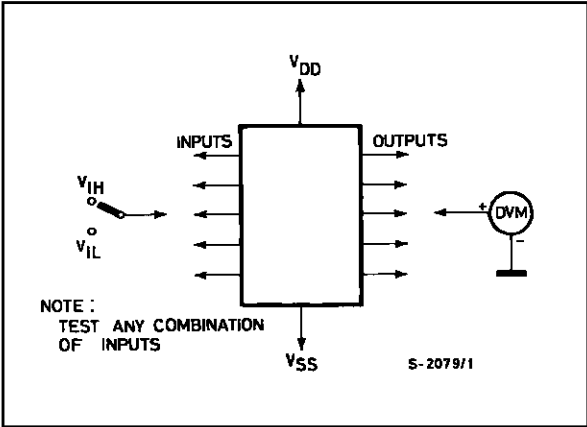


TEST CIRCUITS

Quiescent Device Current

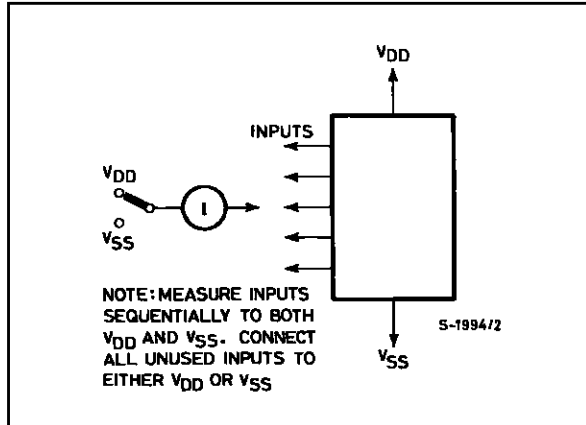


Input Voltage.

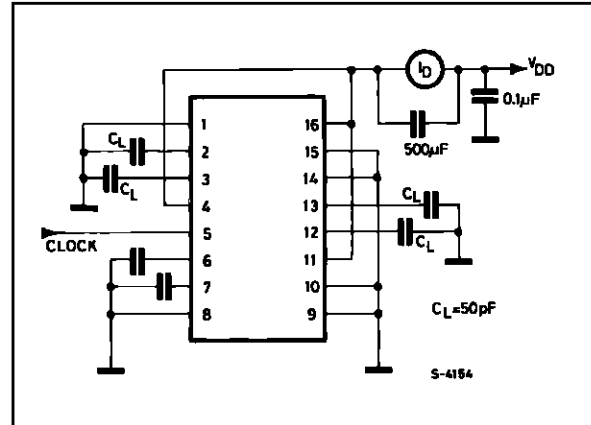


TEST CIRCUITS (continued)

Input Leakage Current.

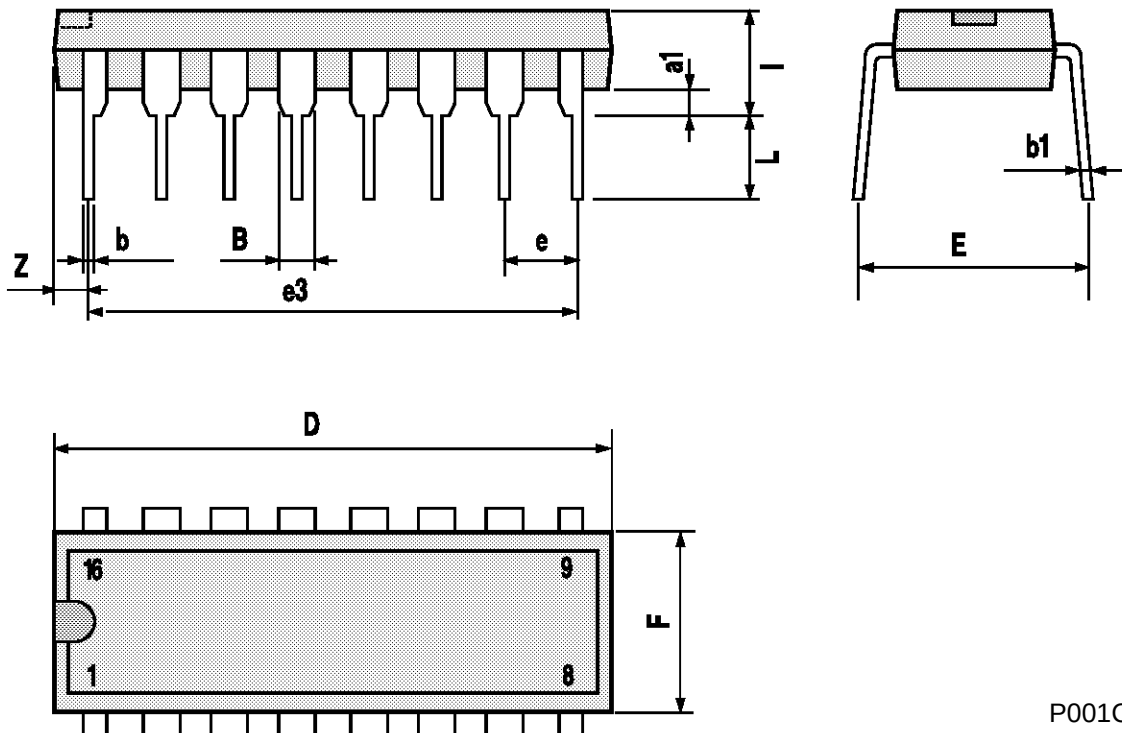


Dynamic Power Dissipation.



Plastic DIP16 (0.25) MECHANICAL DATA

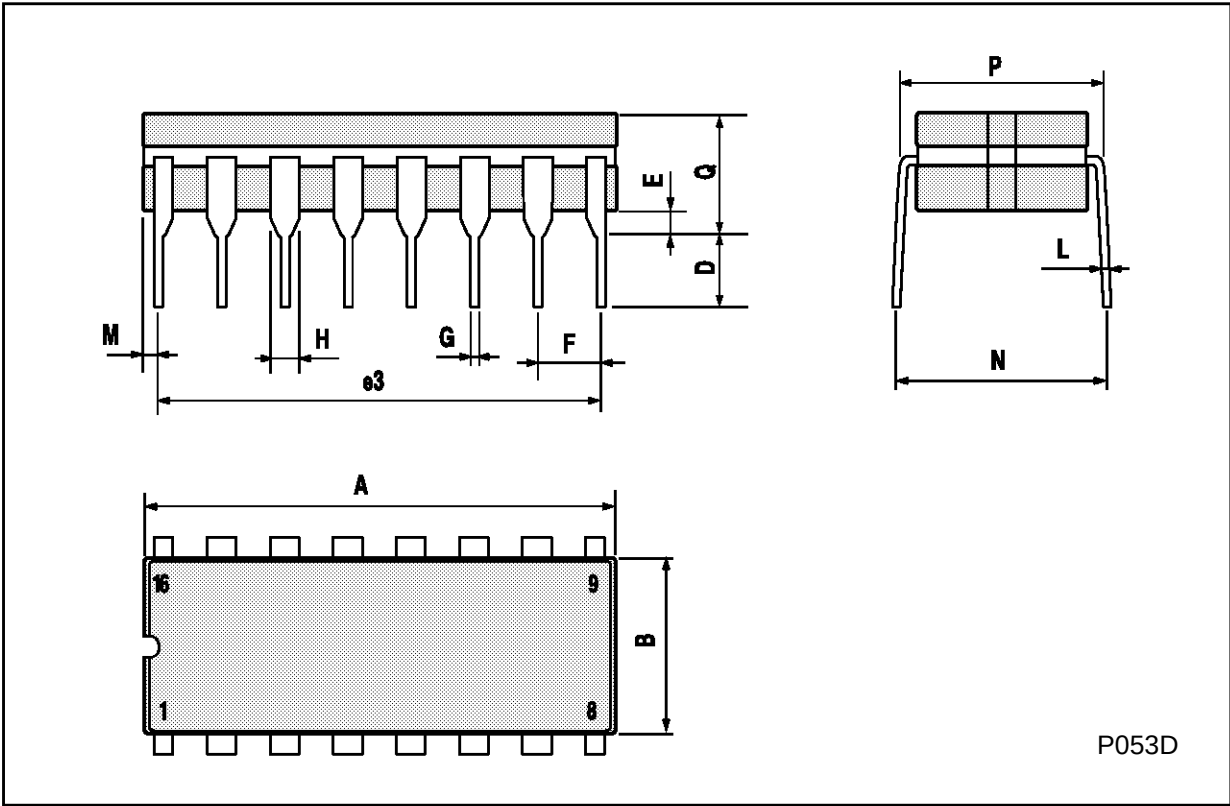
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

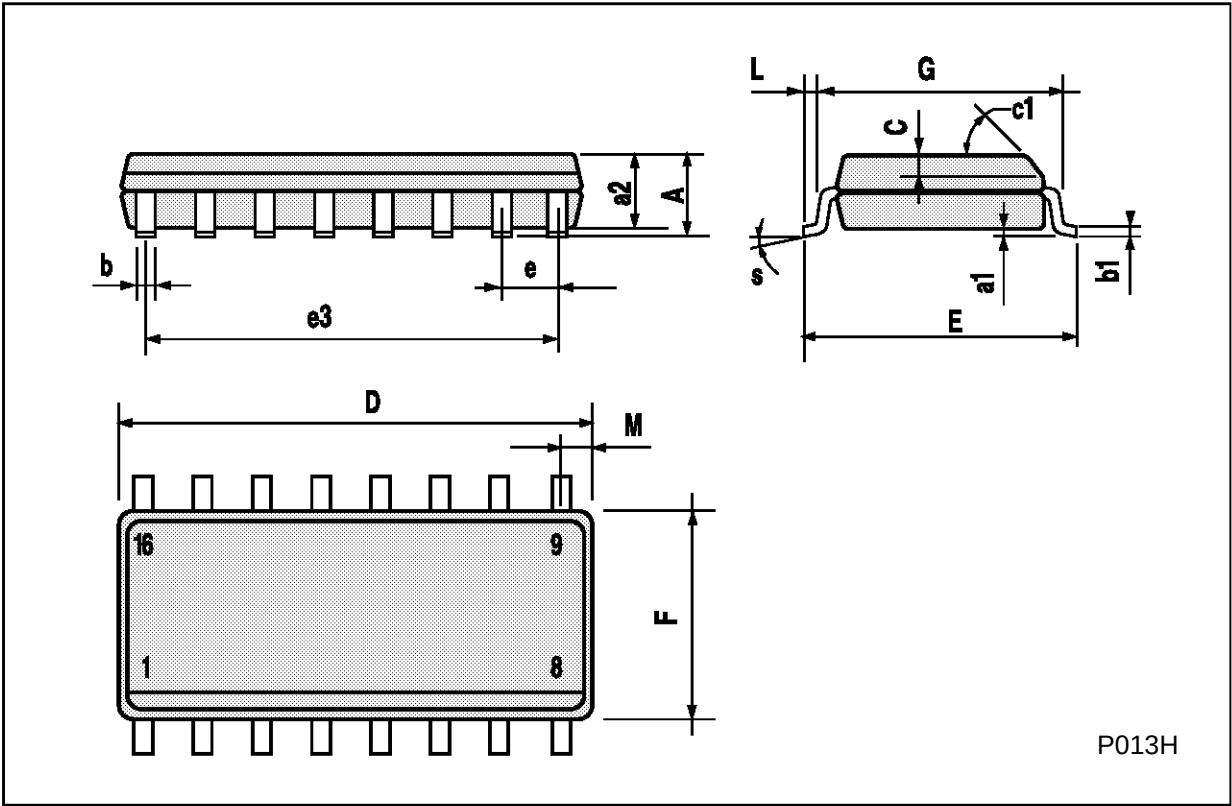
Ceramic DIP16/1 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



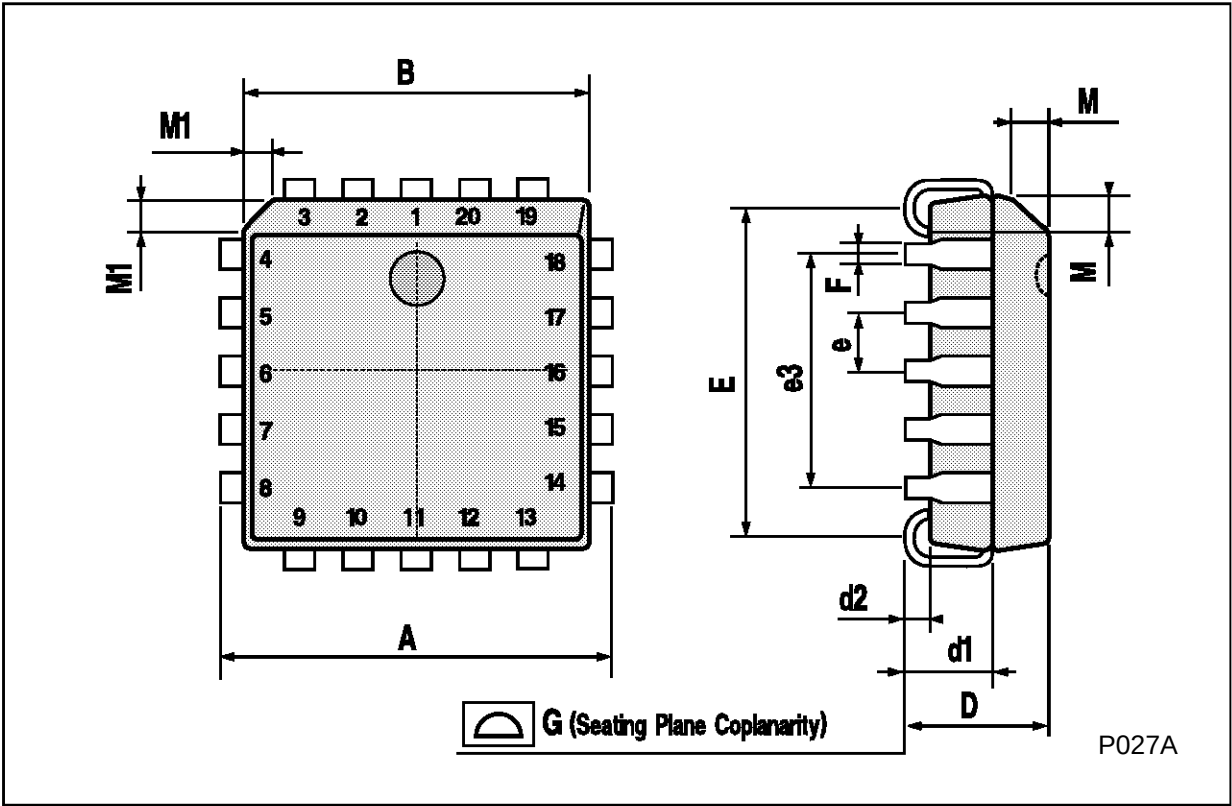
SO16 (Narrow) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



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