# PCF8533

## Universal LCD driver for low multiplex rates

Rev. 6 — 1 October 2012 Product data sheet

## 1. General description

The PCF8533 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)[1] with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 80 segments and can easily be cascaded for larger LCD applications. The PCF8533 is compatible with most microcontrollers and communicates via the two-line bidirectional $I^2C$-bus. Communication overheads are minimized by a display RAM with auto-incremental addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

## 2. Features and benefits

- Single-chip LCD controller and driver
- Selectable backplane drive configuration: static, 2, 3, or 4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$, or $\frac{1}{3}$
- Internal LCD bias generation with voltage follower buffers
- 80 segment outputs allowing to drive:
  - 40 7-segment alphanumeric characters
  - 20 14-segment alphanumeric characters
  - Any graphics of up to 320 elements
- 80 × 4 bit RAM for display data storage
- Auto-incremental display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- Independent supplies possible for LCD and logic voltages
- Wide power supply range: from 1.8 V to 5.5 V
- Wide LCD supply range: from 2.5 V for low threshold LCDs up to 6.5 V for high threshold twisted nematic LCDs
- Low power consumption
- 400 kHz $I^2C$-bus interface
- May be cascaded for large LCD applications (up to 5120 elements possible)
- No external components required
- Compatible with Chip-On-Glass (COG) technology
- Manufactured using silicon gate CMOS process

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 17.

# 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PCF8533U/2/F2 | bare die | 99 bumps; 5.28 x 1.4 x 0.38 mm | PCF8533-2 |

## 3.1 Ordering options

**Table 2. Ordering options**

| Type number | IC revision | Sales item (12NC) | Delivery form |
|---|---|---|---|
| PCF8533U/2/F2[2] | 2 | 935262345026 | chip with hard bumps in tray |

[1] Bump hardness see Table 26.

[2] Not to be used for new designs. Replacement part PCF85133U/2DA/1 for industrial parts and PCA85133U/2DA/Q1 for automotive parts.

# 4. Marking

**Table 3. Marking codes**

| Type number | Marking code |
|---|---|
| PCF8533U/2/F2 | PC8533-2 |


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

## 5. Block diagram

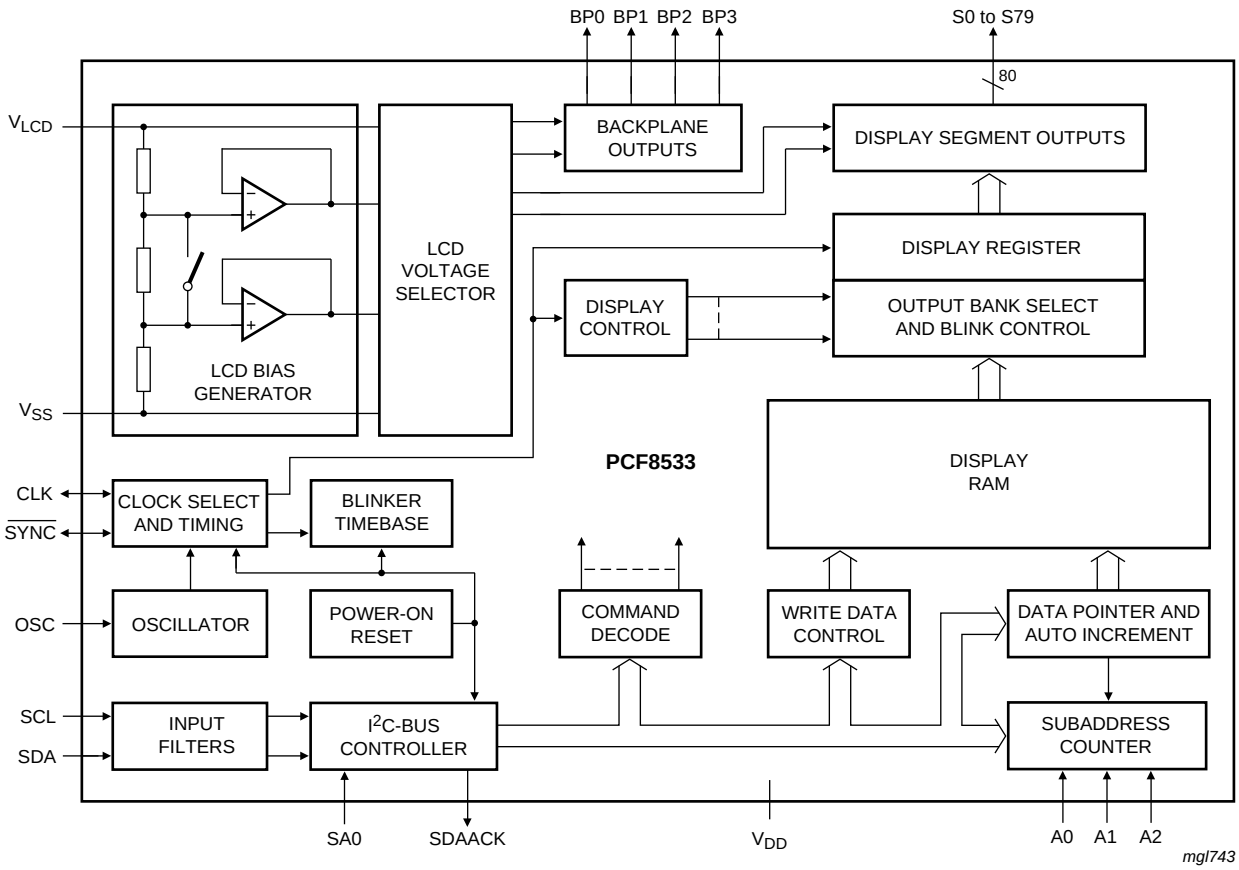


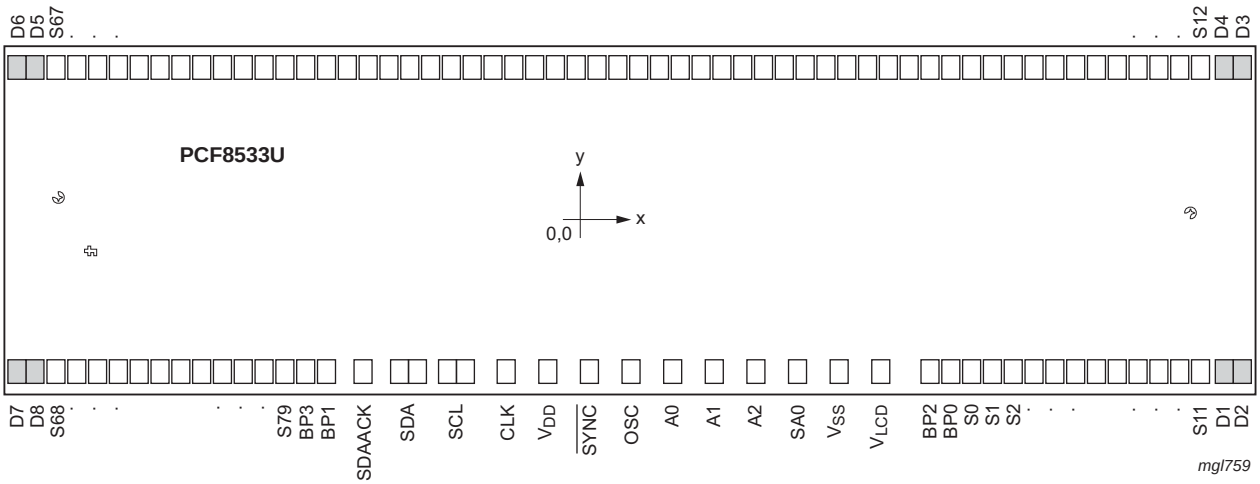

**Fig 1. Block diagram of PCF8533**


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

# 6. Pinning information

## 6.1 Pinning




Viewed from active side. For mechanical details, see Figure 28.

**Fig 2. Pin configuration for PCF8533U**

## 6.2 Pin description

**Table 4. Pin description overview**

| Symbol | Pin | Type | Description |
|---|---|---|---|
| SDAACK | 1 | output | $I^2C$-bus acknowledge |
| SDA | 2 and 3 | input/output | $I^2C$-bus serial data |
| SCL | 4 and 5 | input | $I^2C$-bus serial clock |
| CLK | 6 | input/output | clock input/output |
| $V_{DD}$ | 7 | supply | supply voltage |
| $\overline{SYNC}$ | 8 | input/output | cascade synchronization |
| OSC | 9 | input | oscillator select |
| A0, A1 and A2 | 10 to 12 | input | subaddress |
| SA0 | 13 | input | $I^2C$-bus slave address |
| $V_{SS}$[1] | 14 | supply | ground supply voltage |
| $V_{LCD}$ | 15 | supply | LCD supply voltage |
| BP0, BP1, BP2 and BP3 | 17, 99, 16 and 98 | output | LCD backplane output |
| S0 to S79 | 18 to 97 | output | LCD segment output |
| D1, D2, D3, D4, D5, D6, D7, D8 | | - | dummy pins |

[1] The substrate (rear side of the die) is at $V_{SS}$ potential and should be electrically isolated.


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

# 7. Functional description

The PCF8533 is a versatile peripheral device designed to interface between any microcontroller to a wide variety of LCD segment or dot-matrix displays. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 80 segments.

## 7.1 Commands of PCF8533

The five commands available to the PCF8533 are defined in Table 5.

**Table 5. Definition of commands**

| Command | Operation code | | | | | | | | Reference |
|---|---|---|---|---|---|---|---|---|---|
| **Bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| mode-set | 1 | 1 | 0 | 0 | E | B | M[1:0] | | Table 6 |
| load-data-pointer | 0 | P[6:0] | | | | | | | Table 7 |
| device-select | 1 | 1 | 1 | 0 | 0 | A[2:0] | | | Table 8 |
| bank-select | 1 | 1 | 1 | 1 | 1 | 0 | I | O | Table 9 |
| blink-select | 1 | 1 | 1 | 1 | 0 | AB | BF[1:0] | | Table 10 |

### 7.1.1 Command: mode-set

The mode-set command allows configuring the multiplex mode, the bias levels and enabling or disabling the display.

**Table 6. Mode-set command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 to 4 | - | 1100 | fixed value |
| 3 | E | | **display status**[1] |
| | | 0[2] | disabled (blank)[3] |
| | | 1 | enabled |
| 2 | B | | **LCD bias configuration**[4] |
| | | 0[2] | $\frac{1}{3}$ bias |
| | | 1 | $\frac{1}{2}$ bias |
| 1 to 0 | M[1:0] | | **LCD drive mode selection** |
| | | 01 | static; 1 backplane |
| | | 10 | 1:2 multiplex; 2 backplanes |
| | | 11 | 1:3 multiplex; 3 backplanes |
| | | 00[2] | 1:4 multiplex; 4 backplanes |

[1] The possibility to disable the display allows implementation of blinking under external control.

[2] Default value.

[3] The display is disabled by setting all backplane and segment outputs to $V_{LCD}$.

[4] Not applicable for static drive mode.


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

### 7.1.2 Command: load-data-pointer

The load-data-pointer command defines the display RAM address where the following display data will be sent to.

**Table 7. Load-data-pointer command bit description**

*See Section 7.6.1.*

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | - | 0 | fixed value |
| 6 to 0 | P[6:0] | 0000000[1] to 1001111 | **data pointer**<br>7-bit binary value of 0 to 79, transferred to the data pointer to define one of 80 display RAM addresses |

[1] Default value.

### 7.1.3 Command: device-select

The device-select command allows defining the subaddress counter value.

**Table 8. Device-select command bit description**

*See Section 7.6.2.*

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 to 3 | - | 11100 | fixed value |
| 2 to 0 | A[2:0] | 000[1] to 111 | **device selection**<br>3-bit binary value of 0 to 7, transferred to the subaddress counter to define one of 8 hardware subaddresses |

[1] Default value.

### 7.1.4 Command: bank-select

The bank-select command controls where data is written to RAM and where it is displayed from.

**Table 9. Bank-select command bit description**

*See Section 7.6.5.1 and Section 7.6.5.2.*

| Bit | Symbol | Value | Description[1] | |
|---|---|---|---|---|
| | | | **Static** | **1:2 multiplex** |
| 7 to 2 | - | 111110 | fixed value | |
| 1 | I | | **Input bank selection**: storage of arriving display data | |
| | | 0[2] | RAM row 0 | RAM rows 0 and 1 |
| | | 1 | RAM row 2 | RAM rows 2 and 3 |
| 0 | O | | **Output bank selection**: retrieval of LCD display data | |
| | | 0[2] | RAM row 0 | RAM rows 0 and 1 |
| | | 1 | RAM row 2 | RAM rows 2 and 3 |

[1] The bank-select command has no effect in 1:3 or 1:4 multiplex drive modes.

[2] Default value.


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

### 7.1.5 Command: blink-select

The blink-select command allows configuring the blink mode and the blink frequency.

**Table 10. Blink-select command bit description**

*See Section 7.1.5.1.*

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 to 3 | - | 11110 | fixed value |
| 2 | AB | | **blink mode selection**[1] |
| | | 0[2] | normal blinking |
| | | 1 | blinking by alternating display RAM banks |
| 1 to 0 | BF[1:0] | | **blink mode selection**[3] |
| | | 00[2] | off |
| | | 01 | 1 |
| | | 10 | 2 |
| | | 11 | 3 |

[1] Only normal blinking can be selected in multiplexer 1:3 or 1:4 drive modes.

[2] Default value.

[3] For the blink frequency, see Table 11.

#### 7.1.5.1 Blinking

The display blink capabilities of the PCF8533 are very versatile. The whole display can blink at frequencies selected by the blink-select command (see Table 10). The blink frequencies are fractions of the clock frequency. The ratios between the clock and blink frequencies depend on the blink mode selected (see Table 11).

**Table 11. Blink frequencies**

| Blink mode | Normal operating mode ratio | Nominal blink frequency of $f_{clk}$ (typical $f_{clk}$ = 1.536 kHz) | Unit |
|---|---|---|---|
| Off | - | blinking off | Hz |
| 1 | $\frac{f_{clk}}{768}$ | 2 | Hz |
| 2 | $\frac{f_{clk}}{1536}$ | 1 | Hz |
| 3 | $\frac{f_{clk}}{3072}$ | 0.5 | Hz |

An additional feature is for an arbitrary selection of LCD segments to blink. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads. With the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blink frequency. This mode can also be specified by the blink-select command.

In the 1:3 and 1:4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can blink by selectively changing the display RAM data at fixed time intervals.


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

The entire display can blink at a frequency other than the typical blink frequency. This can be effectively performed by resetting and setting the display enable bit E at the required rate using the mode-set command (see Table 6).

## 7.2 Power-On Reset (POR)

At power-on, the PCF8533 resets to the following starting conditions:

1. All backplane outputs are set to $V_{LCD}$.
2. All segment outputs are set to $V_{LCD}$.
3. The selected drive mode is: 1:4 multiplex with $\frac{1}{3}$ bias.
4. Blinking is switched off.
5. Input and output bank selectors are reset.
6. The $I^2C$-bus interface is initialized.
7. The data pointer and the subaddress counter are cleared (set to logic 0).
8. The display is disabled (bit E = 0, see Table 6).

**Remark:** Do not transfer data on the $I^2C$-bus for at least 1 ms after a power-on to allow the reset action to complete.

## 7.3 Possible display configurations

The display configurations possible with the PCF8533 depend on the required number of active backplane outputs. A selection of display configurations is given in Table 12.

All of the display configurations given in Table 12 can be implemented in a typical system as shown in Figure 4.

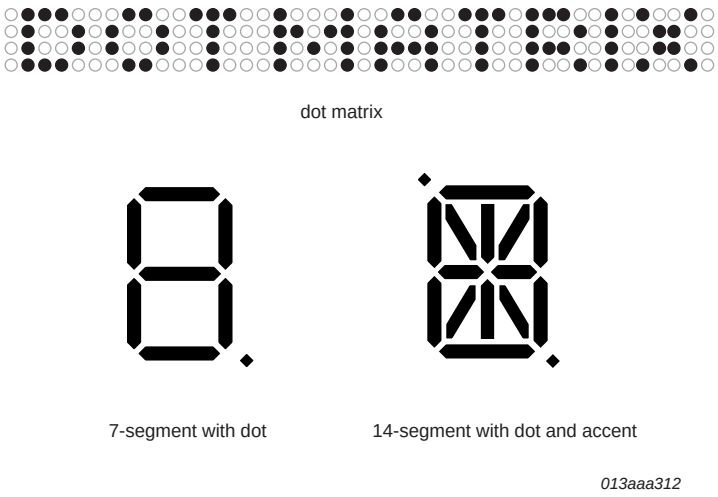



**Fig 3. Example of displays suitable for PCF8533**


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

**Table 12. Selection of possible display configurations**

| Number of | | | | |
|---|---|---|---|---|
| **Backplanes** | **Icons** | **Digits/Characters** | | **Dot matrix/ Elements** |
| | | **7-segment[1]** | **14-segment[2]** | |
| 4 | 320 | 40 | 20 | 320 (4 × 80) |
| 3 | 240 | 30 | 15 | 240 (3 × 80) |
| 2 | 160 | 20 | 10 | 160 (2 × 80) |
| 1 | 80 | 10 | 5 | 80 (1 × 80) |

[1] 7 segment display has 8 elements including the decimal point.

[2] 14 segment display has 16 elements including decimal point and accent dot.

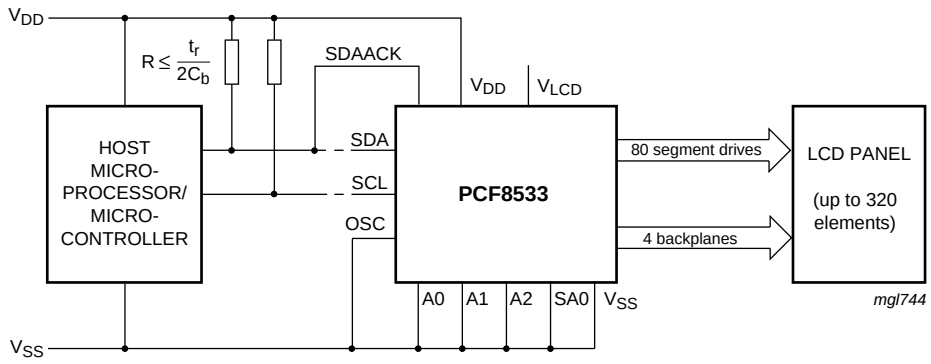



**Fig 4. Typical system configuration**

The host microcontroller maintains the 2-line I$^2$C-bus communication channel with the PCF8533. The internal oscillator is enabled by connecting pin OSC to pin $V_{SS}$. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are the power supplies ($V_{DD}$, $V_{SS}$, and $V_{LCD}$) and the LCD panel chosen for the application.

### 7.3.1 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider of three impedances connected between pins $V_{LCD}$ and $V_{SS}$. The center impedance is bypassed by switch if the ½ bias voltage level for the 1:2 multiplex drive mode configuration is selected.

### 7.3.2 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{LCD}$ and the resulting discrimination ratios (D) are given in Table 13.

Discrimination is a term which is defined as the ratio of the on and off RMS voltage across a segment. It can be thought of as a measurement of contrast.


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

**Table 13. Biasing characteristics**

| LCD drive mode | Number of: | | LCD bias configuration | $\frac{V_{off(RMS)}}{V_{LCD}}$ | $\frac{V_{on(RMS)}}{V_{LCD}}$ | $D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$ |
|---|---|---|---|---|---|---|
| | Backplanes | Levels | | | | |
| static | 1 | 2 | static | 0 | 1 | ∞ |
| 1:2 multiplex | 2 | 3 | ½ | 0.354 | 0.791 | 2.236 |
| 1:2 multiplex | 2 | 4 | ⅓ | 0.333 | 0.745 | 2.236 |
| 1:3 multiplex | 3 | 4 | ⅓ | 0.333 | 0.638 | 1.915 |
| 1:4 multiplex | 4 | 4 | ⅓ | 0.333 | 0.577 | 1.732 |

A practical value for $V_{LCD}$ is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th(off)}$), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode, a suitable choice is $V_{LCD} > 3V_{th(off)}$.

Multiplex drive modes of 1:3 and 1:4 with ½ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for ½ bias

a = 2 for ⅓ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 1:

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1+a)^2}} \quad (1)$$

where the values for n are

n = 1 for static drive mode

n = 2 for 1:2 multiplex drive mode

n = 3 for 1:3 multiplex drive mode

n = 4 for 1:4 multiplex drive mode

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 2:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1+a)^2}} \quad (2)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 3:

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{a^2 + 2a + n}{a^2 - 2a + n}} \quad (3)$$

Using Equation 3, the discrimination for an LCD drive mode of 1:3 multiplex with ½ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with ½ bias is $\frac{\sqrt{21}}{3} = 1.528$.


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage $V_{LCD}$ as follows:

- 1:3 multiplex (½ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449 V_{off(RMS)}$
- 1:4 multiplex (½ bias): $V_{LCD} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309 V_{off(RMS)}$

These compare with $V_{LCD} = 3V_{off(RMS)}$ when ⅓ bias is used.

$V_{LCD}$ is sometimes referred as the LCD operating voltage.

#### 7.3.2.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel will be switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 5. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \quad (4)$$

$$V_{off(RMS)} \leq V_{th(off)} \quad (5)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a, n (see Equation 1 to Equation 3) and the $V_{LCD}$ voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes named $V_{th}$. $V_{th(on)}$ is sometimes named saturation voltage $V_{sat}$.

It is important to match the module properties to those of the driver in order to achieve optimum performance.

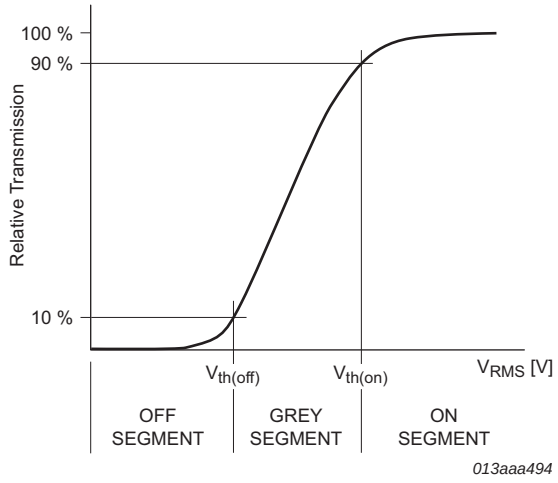



**Fig 5. Electro-optical characteristic: relative transmission curve of the liquid**

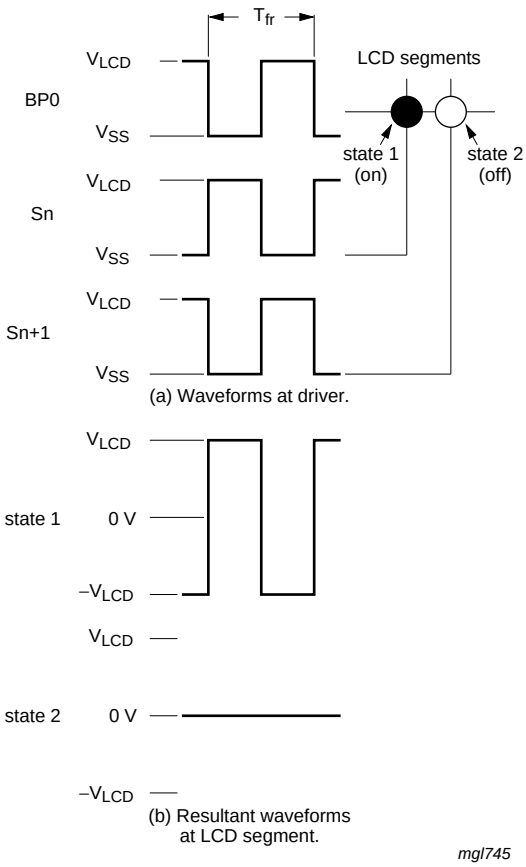

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

### 7.3.3 LCD drive mode waveforms

#### 7.3.3.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. The backplane (BPn) and segment drive (Sn) waveforms for this mode are shown in Figure 6.




$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = V_{LCD}$.

$V_{state2}(t) = V_{(Sn+1)}(t) - V_{BP0}(t)$.

$V_{off(RMS)} = 0$ V.

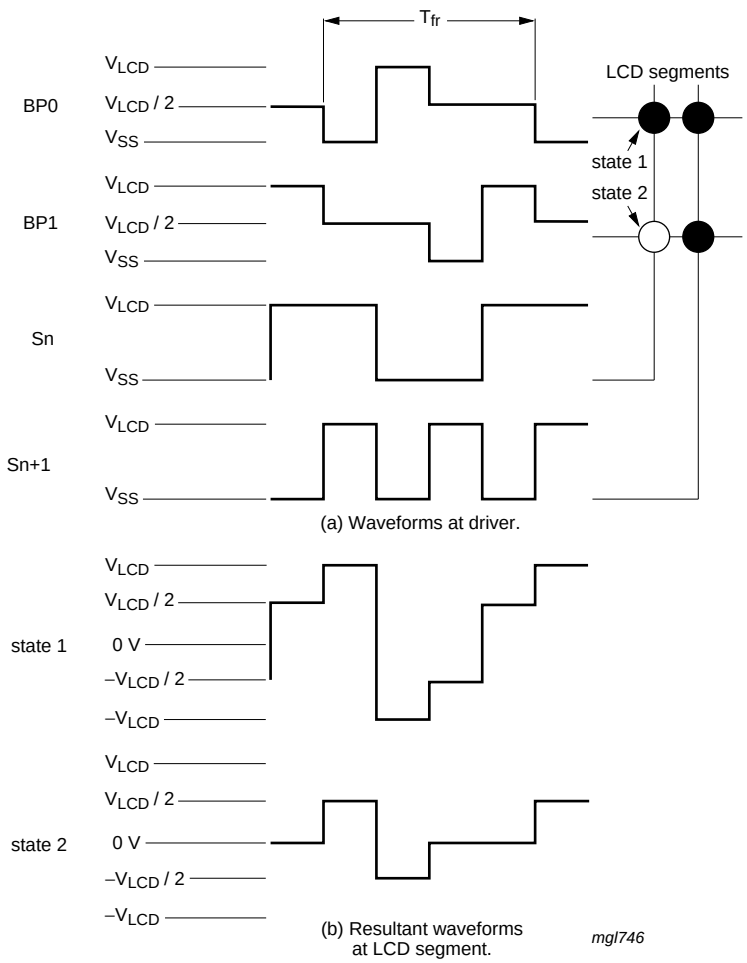
**Fig 6. Static drive mode waveforms**


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

### 7.3.3.2 1:2 multiplex drive mode

The 1:2 multiplex drive mode is used when two backplanes are provided in the LCD. This mode allows fractional LCD bias voltages of ½ bias or ⅓ bias as shown in Figure 7 and Figure 8.




$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.791V_{LCD}$.

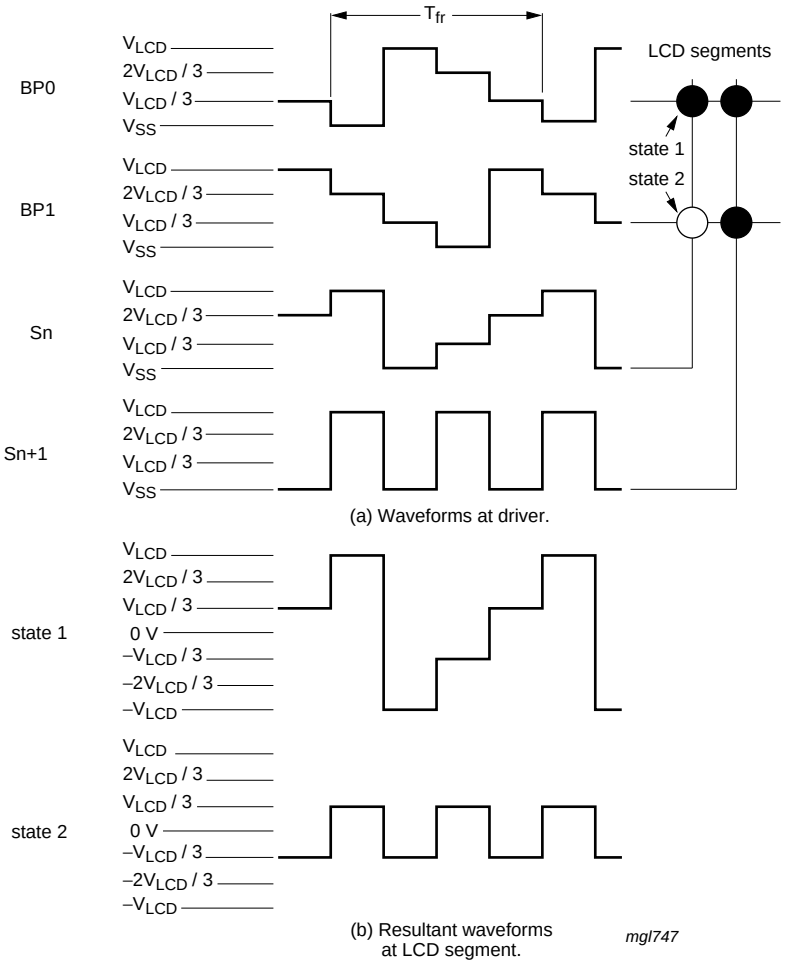
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.354V_{LCD}$.

**Fig 7. Waveforms for the 1:2 multiplex drive mode with ½ bias**


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.




$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.745V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

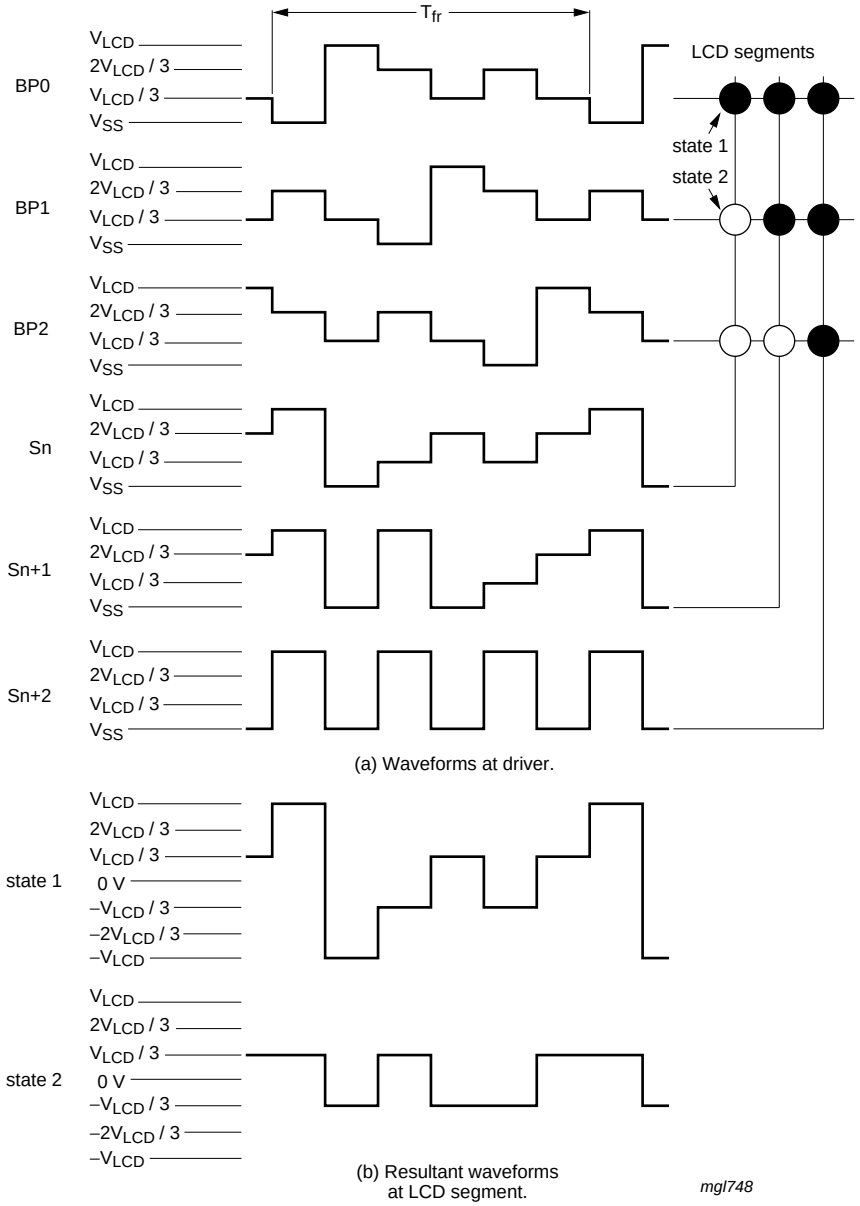
**Fig 8. Waveforms for the 1:2 multiplex drive mode with ⅓ bias**


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

#### 7.3.3.3 1:3 multiplex drive mode

The 1:3 multiplex drive mode is used when three backplanes are provided in the LCD as shown in Figure 9.




$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.638V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

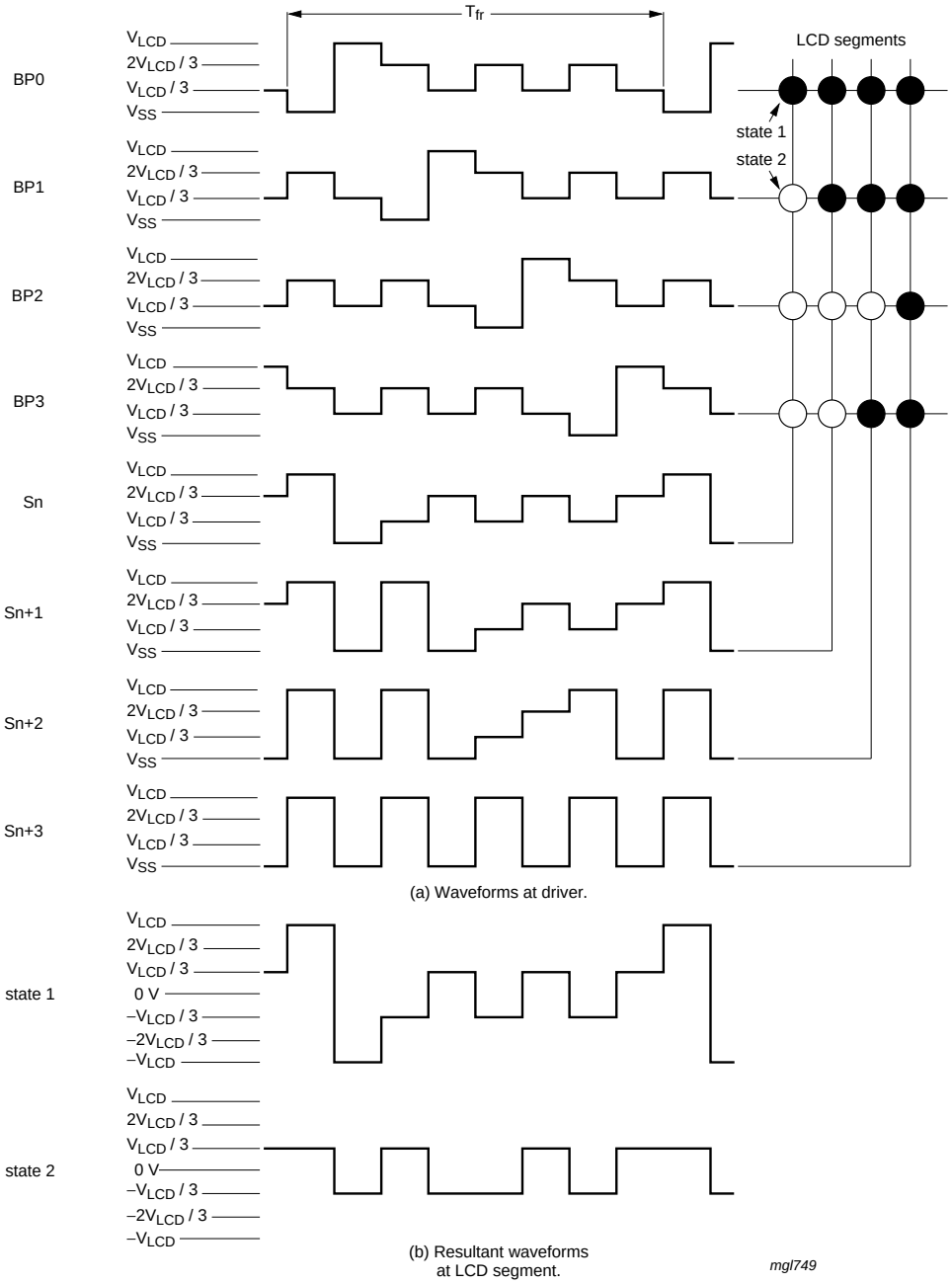
**Fig 9. Waveforms for the 1:3 multiplex drive mode with ⅓ bias**


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

### 7.3.3.4 1:4 multiplex drive mode

The 1:4 multiplex drive mode is used when four backplanes are provided in the LCD as shown in Figure 10.




$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.577V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

**Fig 10. Waveforms for the 1:4 multiplex drive mode with ⅓ bias**


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

## 7.4 Oscillator

The internal logic and the LCD drive signals of the PCF8533 are timed by a frequency $f_{clk}$, which either is derived from the built-in oscillator frequency $f_{osc}$ or equals an external clock frequency $f_{clk(ext)}$.

$$f_{clk} = \frac{f_{osc}}{64}$$

The clock frequency $f_{clk}$ determines the LCD frame frequency $f_{fr}$ (see Table 14) and is calculated as follows:

$$f_{fr} = \frac{f_{clk}}{24}$$

**Table 14. LCD frame frequency**

| Nominal clock frequency (Hz) | LCD frame frequency (Hz) |
|---|---|
| 1536 | 64 |

### 7.4.1 Internal clock

The internal oscillator is enabled by connecting pin OSC to $V_{SS}$. In this case, the output from pin CLK provides the clock signal for cascaded PCF8533 in the system.

### 7.4.2 External clock

Pin CLK is enabled as an external clock input by connecting pin OSC to $V_{DD}$.

**Remark:** A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal.

### 7.4.3 Timing

The PCF8533 timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal ($\overline{SYNC}$) maintains the correct timing relationship between all PCF8533 in the system. The timing also generates the LCD frame signal ($f_{fr}$) whose frequency is derived as an integer division of the clock frequency $f_{clk}$ (see Table 14), applied to pin CLK from either the internal or an external clock.

## 7.5 Backplane and segment outputs


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

### 7.5.1 Backplane outputs

The LCD drive section includes four backplane outputs: BP0 to BP3. The backplane output signals are generated based on the selected LCD drive mode.

- In 1:4 multiplex drive mode: BP0 to BP3 must be connected directly to the LCD.

If less than four backplane outputs are required, the unused outputs can be left open-circuit.

- In 1:3 multiplex drive mode: BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.
- In 1:2 multiplex drive mode: BP0 and BP2, respectively, BP1 and BP3 carry the same signals and can also be paired to increase the drive capabilities.
- In static drive mode: The same signal is carried by all four backplane outputs; and they can be connected in parallel for very high drive requirements.

### 7.5.2 Segment outputs

The LCD drive section includes 80 segment outputs (S0 to S79) which must be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display register. When less than 80 segment outputs are required, the unused segment outputs must be left open-circuit.

## 7.6 Display RAM

The display RAM is a static 80 $\times$ 4 bit RAM which stores LCD data.

There is a one-to-one correspondence between

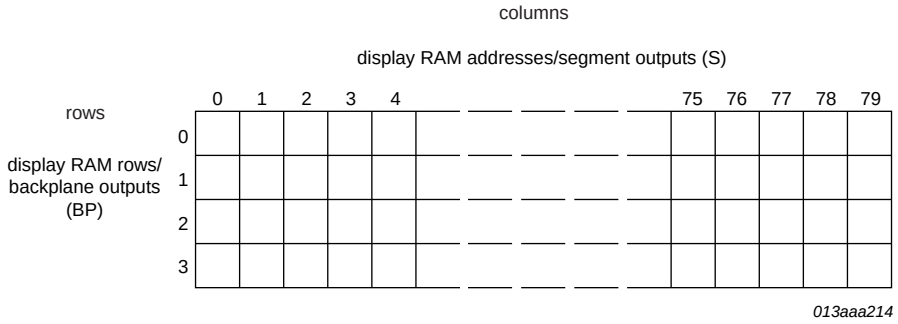
- the bits in the RAM bitmap and the LCD elements
- the RAM columns and the segment outputs
- the RAM rows and the backplane outputs.

A logic 1 in the RAM bitmap indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the off-state.

The display RAM bit map, Figure 11, shows rows 0 to 3 which correspond with the backplane outputs BP0 to BP3, and columns 0 to 79 which correspond with the segment outputs S0 to S79. In multiplexed LCD applications the segment data of the first, second, third and fourth row of the display RAM are time-multiplexed with BP0, BP1, BP2, and BP3 respectively.


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.




The display RAM bitmap shows the direct relationship between the display RAM addresses and the segment outputs and between the bits in a RAM word and the backplane outputs.

**Fig 11. Display RAM bitmap**

When display data is transmitted to the PCF8533, the received display bytes are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and depending on the current multiplex drive mode the bits are stored singularly, in pairs, triples or quadruples. To illustrate the filling order, an example of a 7-segment display showing all drive modes is given in Figure 12; the RAM filling organization depicted applies equally to other LCD types.

- In static drive mode the eight transmitted data bits are placed into row 0 as one byte.
- In 1:2 multiplex drive mode the eight transmitted data bits are placed in pairs into row 0 and 1 as two successive 4-bit RAM words.
- In 1:3 multiplex drive mode the eight bits are placed in triples into row 0, 1, and 2 as three successive 3-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address, but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted (see Section 7.6.3).
- In 1:4 multiplex drive mode, the eight transmitted data bits are placed in quadruples into row 0, 1, 2, and 3 as two successive 4-bit RAM words.


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

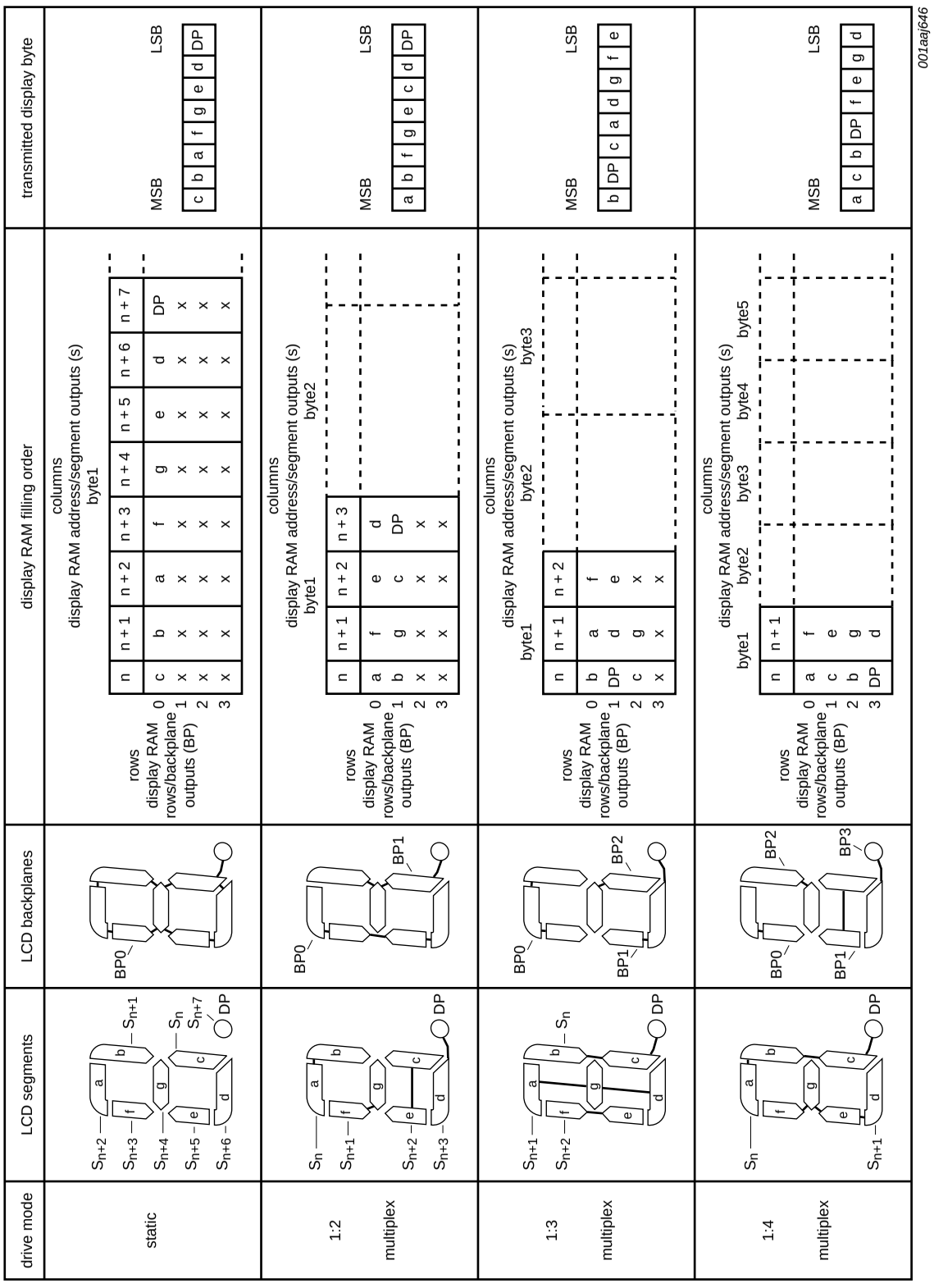



**Fig 12. Relationships between LCD layout, drive mode, display RAM filling order, and display data transmitted over the I²C-bus**


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

### 7.6.1 Data pointer

The addressing mechanism for the display RAM is realized using a data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command (see Table 7). Following this command, an arriving data byte is stored at the display RAM address indicated by the data pointer. The filling order is shown in Figure 12. After each byte is stored, the content of the data pointer is automatically incremented by a value dependent on the selected LCD drive mode:

- In static drive mode by eight
- In 1:2 multiplex drive mode by four
- In 1:3 multiplex drive mode by three
- In 1:4 multiplex drive mode by two

If an $I^2C$-bus data access is terminated early, then the state of the data pointer is unknown. So, the data pointer must be rewritten before further RAM accesses.

### 7.6.2 Subaddress counter

The storage of display data is determined by the content of the subaddress counter. Storage is allowed only when the content of the subaddress counter match with the hardware subaddress applied to A0, A1, and A2. The subaddress counter value is defined by the device-select command (see Table 8). If the content of the subaddress counter and the hardware subaddress do not match, then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCF8533 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

The hardware subaddress must not be changed while the device is being accessed on the $I^2C$-bus interface.

### 7.6.3 RAM writing in 1:3 multiplex drive mode

In 1:3 multiplex drive mode, the RAM is written as shown in Table 15 (see Figure 12 as well).

**Table 15. Standard RAM filling in 1:3 multiplex drive mode**

*Assumption: BP2/S2, BP2/S5, BP2/S8 and so on,* ***are not connected*** *to any elements on the display.*

| Display RAM bits (rows)/ backplane outputs (BPn) | Display RAM addresses (columns)/segment outputs (Sn) | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **:** |
| **0** | a7 | a4 | a1 | b7 | b4 | b1 | c7 | c4 | c1 | d7 | : |
| **1** | a6 | a3 | a0 | b6 | b3 | b0 | c6 | c3 | c0 | d6 | : |
| **2** | a5 | a2 | - | b5 | b2 | - | c5 | c2 | - | d5 | : |
| **3** | - | - | - | - | - | - | - | - | - | - | : |


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

If the bit at position BP2/S2 would be written by a second byte transmitted, then the mapping of the segment bits would change as illustrated in Table 16.

**Table 16. Entire RAM filling by rewriting in 1:3 multiplex drive mode**

*Assumption: BP2/S2, BP2/S5, BP2/S8 and so on, **are connected** to elements on the display.*

| Display RAM bits (rows)/ backplane outputs (BPn) | Display RAM addresses (columns)/segment outputs (Sn) | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **:** |
| **0** | a7 | a4 | a1/b7 | b4 | b1/c7 | c4 | c1/d7 | d4 | d1/e7 | e4 | : |
| **1** | a6 | a3 | a0/b6 | b3 | b0/c6 | c3 | c0/d6 | d3 | d0/e6 | e3 | : |
| **2** | a5 | a2 | b5 | b2 | c5 | c2 | d5 | d2 | e5 | e2 | : |
| **3** | - | - | - | - | - | - | - | - | - | - | : |

In the case described in Table 16 the RAM has to be written entirely and BP2/S2, BP2/S5, BP2/S8 and so on, have to be connected to elements on the display. This can be achieved by a combination of writing and rewriting the RAM like follows:

- In the first write to the RAM, bits a7 to a0 are written
- The data-pointer (see Section 7.6.1 on page 21) has to be set to the address of bit a1
- In the second write, bits b7 to b0 are written, overwriting bits a1 and a0 with bits b7 and b6
- The data-pointer has to be set to the address of bit b1
- In the third write, bits c7 to c0 are written, overwriting bits b1 and b0 with bits c7 and c6

Depending on the method of writing to the RAM (standard or entire filling by rewriting), some elements remain unused or can be used, but it has to be considered in the module layout process as well as in the driver software design.

### 7.6.4 Writing over the RAM address boundary

In all multiplex drive modes, depending on the setting of the data pointer, it is possible to fill the RAM over the RAM address boundary. If the PCF8533 is part of a cascade, the additional bits fall into the next device that also generates the acknowledge signal. If the PCF8533 is a single device or the last device in a cascade, the additional bits will be discarded and no acknowledge signal will be generated.

### 7.6.5 Bank selection

#### 7.6.5.1 Output bank selector

The output bank selector (see Table 9) selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the selected LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode, all RAM addresses of row 0 are selected, these are followed by the contents of row 1, 2, and then 3
- In 1:3 multiplex mode, rows 0, 1, and 2 are selected sequentially
- In 1:2 multiplex mode, rows 0 and 1 are selected
- In static mode, row 0 is selected


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

The PCF8533 includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In the 1:2 multiplex mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

#### 7.6.5.2 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in row 2 in static drive mode or in rows 2 and 3 in 1:2 multiplex drive mode by using the bank-select command (see Table 9). The input bank selector functions independently to the output bank selector.

#### 7.6.5.3 RAM bank switching

The PCF8533 includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. A bank can be thought of as one RAM row or a collection of RAM rows (see Figure 13). The RAM bank switching gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is complete.

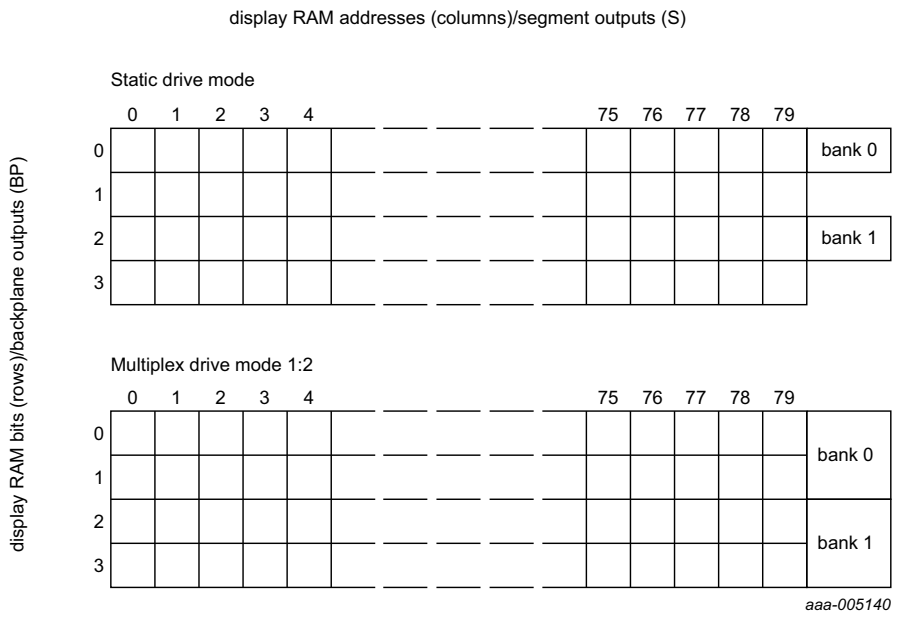



**Fig 13. RAM banks in static and multiplex driving mode 1:2**

There are two banks; bank 0 and bank 1. Figure 13 shows the location of these banks relative to the RAM map. Input and output banks can be set independently from one another with the Bank-select command (see Table 9 on page 6). Figure 14 shows the concept.


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

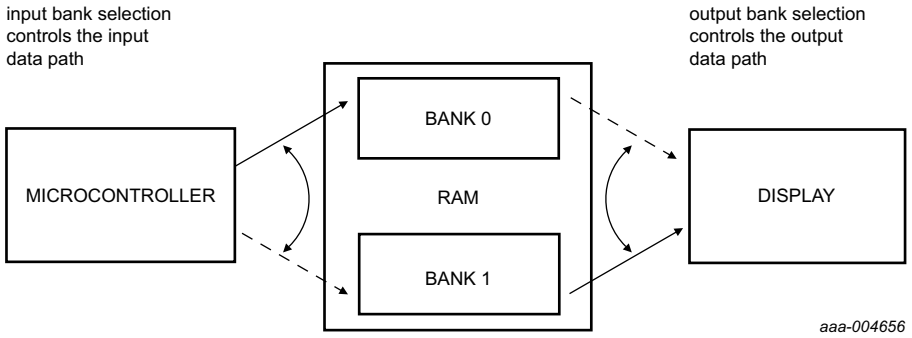



**Fig 14. Bank selection**

In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In the 1:2 multiplex mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

In Figure 15 an example is shown for 1:2 multiplex drive mode where the displayed data is read from the first two rows of the memory (bank 0), while the transmitted data is stored in the second two rows of the memory (bank 1).

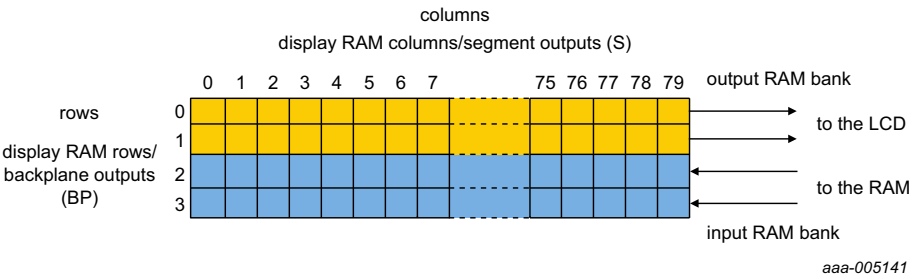



**Fig 15. Example of the Bank-select command with multiplex drive mode 1:2**


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

# 8. I²C-bus interface

## 8.1 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

By connecting pin SDAACK to pin SDA on the PCF8533, the SDA line becomes fully I²C-bus compatible. In COG applications where the track resistance from the SDAACK pin to the system SDA line can be significant, possibly a voltage divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. As a consequence, it may be possible that the acknowledge generated by the PCF8533 cannot be interpreted as logic 0 by the master. In COG applications where the acknowledge cycle is required, it is therefore necessary to minimize the track resistance from the SDAACK pin to the system SDA line to guarantee a valid LOW level.

By separating the acknowledge output from the serial data line (having the SDAACK open circuit) design efforts to generate a valid acknowledge level can be avoided. However, in that case the I²C-bus master has to be set up in such a way that it ignores the acknowledge cycle.[2]

The following definition assumes that SDA and SDAACK are connected and refers to the pair as SDA.

### 8.1.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal; see Figure 16.

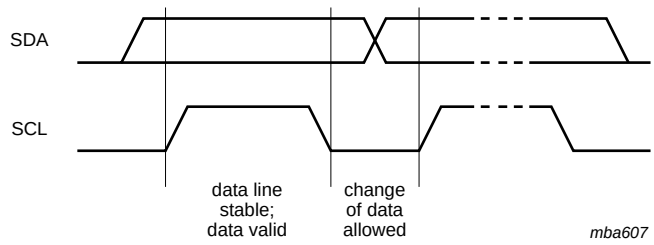



**Fig 16. Bit transfer**

### 8.1.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW change of the data line, while the clock is HIGH is defined as the START condition (S).

2. For further information, please consider the NXP application note: Ref. 1 “AN10170”.


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

A LOW-to-HIGH change of the data line while the clock is HIGH is defined as the STOP condition (P).

The START and STOP conditions are shown in Figure 17.

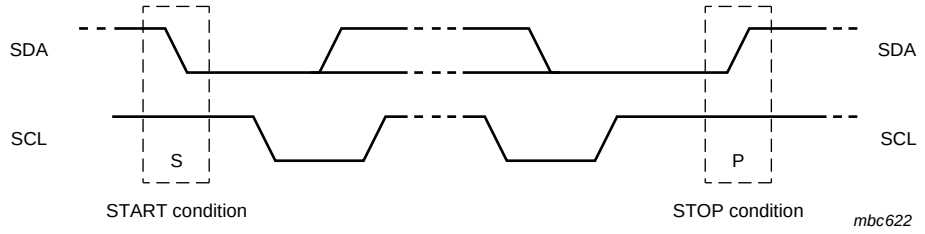



**Fig 17. Definition of START and STOP conditions**

### 8.1.3 System configuration

A device generating a message is a transmitter; a device receiving a message is a receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves; see Figure 18.

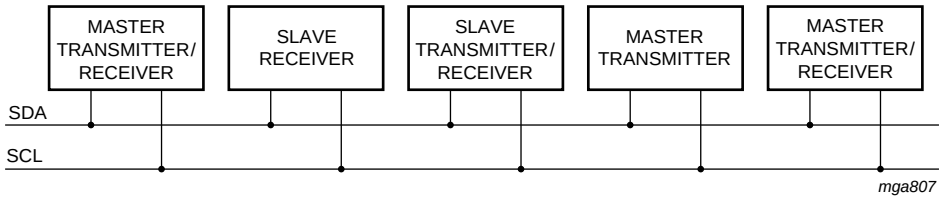



**Fig 18. System configuration**

### 8.1.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- A master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the $I^2C$-bus is illustrated in Figure 19.


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

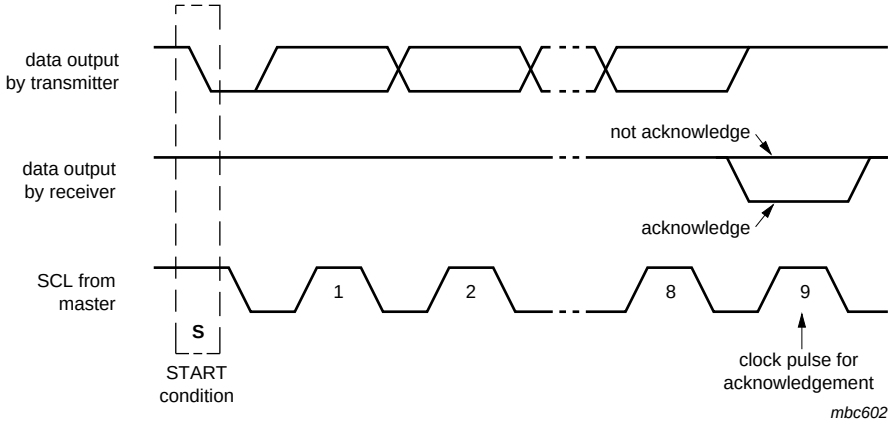



**Fig 19. Acknowledgement on the I²C-bus**

### 8.1.5 I²C-bus controller

The PCF8533 acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCF8533 is the acknowledge signal of the selected device. Device selection depends on the I²C-bus slave address, the transferred command data and the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1, and A2 are normally tied to $V_{SS}$ which defines the hardware subaddress 0. In multiple device applications A0, A1, and A2 are tied to $V_{SS}$ or $V_{DD}$ using a binary coding scheme, so that no two devices with a common I²C-bus slave address have the same hardware subaddress.

### 8.1.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

### 8.1.7 I²C-bus protocol

Two I²C-bus slave addresses (0111 000 and 0111 001) are reserved for the PCF8533.

The PCF8533 slave address is illustrated in Table 17.

**Table 17. I²C slave address byte**

| Bit | Slave address | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7<br>MSB | 6 | 5 | 4 | 3 | 2 | 1 | 0<br>LSB |
| | 0 | 1 | 1 | 1 | 0 | 0 | SA0 | R/$\overline{W}$ |

The least significant bit of the slave address that a PCF8533 will respond to is defined by the level tied to its SA0 input. The PCF8533 is a write-only device and will not respond to a read access. Having two reserved slave addresses allows the following on the same I²C-bus:

- Up to 16 PCF8533 for very large LCD applications
- The use of two types of LCD multiplex drive modes.


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

The I²C-bus protocol is shown in Figure 20. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of two possible PCF8533 slave addresses available. All PCF8533 whose SA0 inputs correspond to bit 0 of the slave address respond by asserting an acknowledge in parallel. This I²C-bus transfer is ignored by all PCF8533 whose SA0 inputs are set to the alternative level.

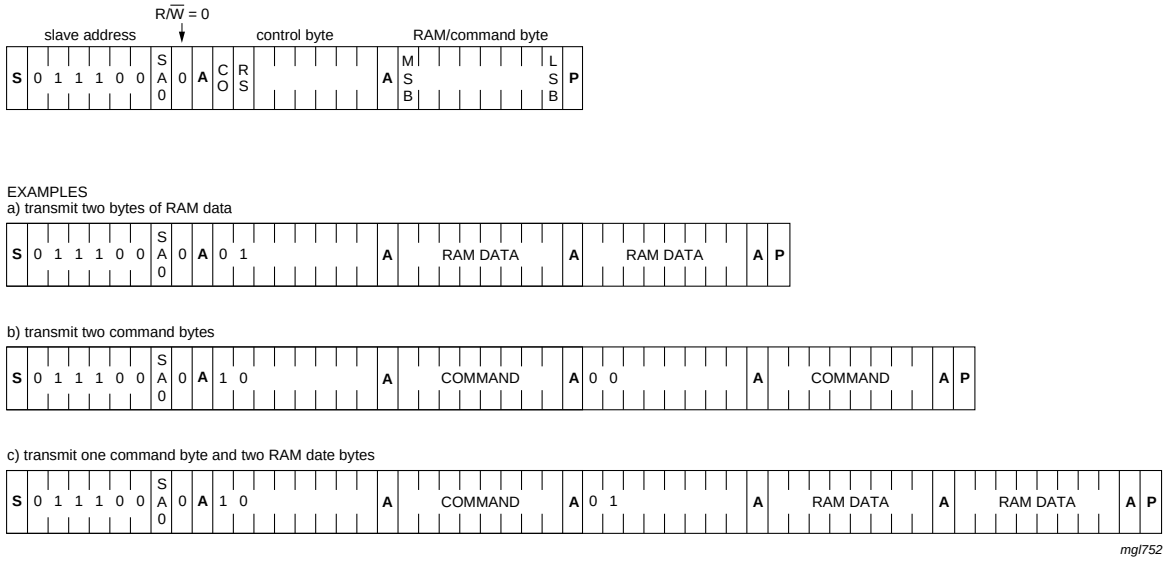



**Fig 20. I²C-bus protocol**

After acknowledgement, the control byte is sent defining if the next byte is a RAM or command information. The control byte also defines if the next byte is a control byte or further RAM or command data (see Figure 21 and Table 18). In this way, it is possible to configure the device and then fill the display RAM with little overhead.

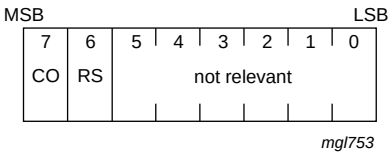



**Fig 21. Control byte format**

**Table 18. Control byte description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | CO | | **continue bit** |
| | | 0 | last control byte |
| | | 1 | control bytes continue |
| 6 | RS | | register selection |
| | | 0 | command register |
| | | 1 | data register |
| 5 to 0 | - | | not relevant |


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

The command bytes and control bytes are also acknowledged by all addressed PCF8533 connected to the bus.

The display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter; see Section 7.6.1 and Section 7.6.2.

The acknowledgement after each byte is made only by the (A0, A1, and A2) addressed PCF8533. After the last (display) byte, the $I^2C$-bus master asserts a STOP condition (P). Alternatively a START may be asserted to RESTART an $I^2C$-bus access.


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

# 9. Internal circuitry

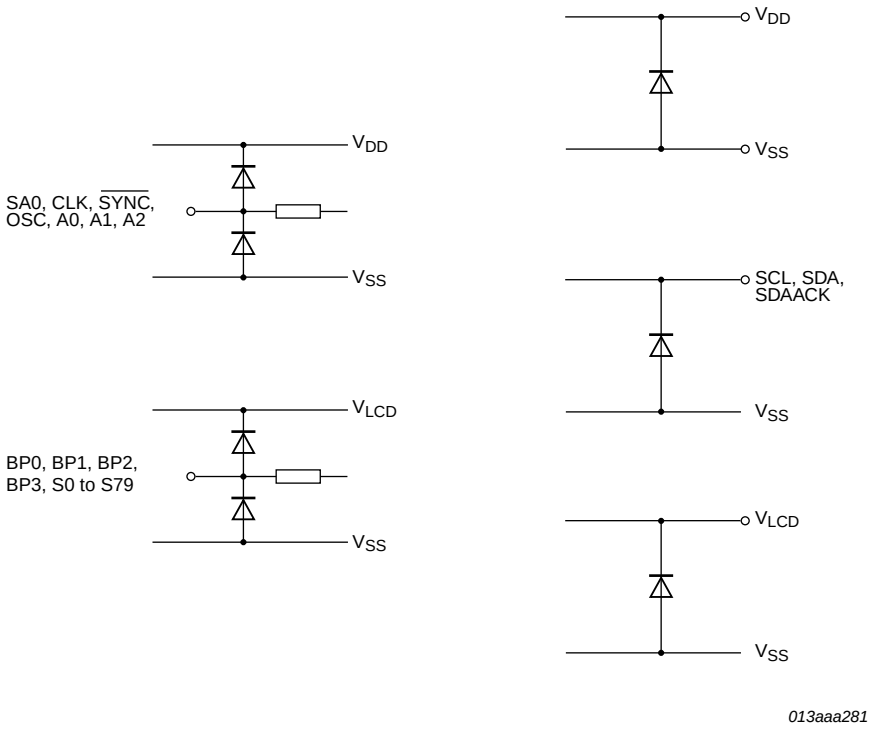



**Fig 22. Device protection diagram**


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

# 10. Limiting values

**CAUTION**

Static voltages across the liquid crystal display can build up when the LCD supply voltage ($V_{LCD}$) is on while the IC supply voltage ($V_{DD}$) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, $V_{LCD}$ and $V_{DD}$ must be applied or removed together.

**Table 19. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | | −0.5 | +6.5 | V |
| $V_{LCD}$ | LCD supply voltage | | | −0.5 | +7.5 | V |
| $V_{i(n)}$ | voltage on any input | $V_{DD}$-related inputs | | −0.5 | +6.5 | V |
| $V_{o(n)}$ | voltage on any output | $V_{LCD}$-related outputs | | −0.5 | +7.5 | V |
| $I_I$ | input current | | | −10 | +10 | mA |
| $I_O$ | output current | | | −10 | +10 | mA |
| $I_{DD}$ | supply current | | | −50 | +50 | mA |
| $I_{SS}$ | ground supply current | | | −50 | +50 | mA |
| $I_{DD(LCD)}$ | LCD supply current | | | −50 | +50 | mA |
| $P_{tot}$ | total power dissipation | | | - | 400 | mW |
| P/out | power dissipation per output | | | - | 100 | mW |
| $V_{ESD}$ | electrostatic discharge voltage | HBM | [1] | - | ±4500 | V |
| | | MM | [2] | - | ±200 | V |
| $I_{lu}$ | latch-up current | | [3] | - | 200 | mA |
| $T_{stg}$ | storage temperature | | [4] | −65 | +150 | °C |
| $T_{amb}$ | ambient temperature | operating device | | −40 | +85 | °C |

[1] Pass level; Human Body Model (HBM), according to Ref. 6 “JESD22-A114”.

[2] Pass level; Machine Model (MM), according to Ref. 7 “JESD22-A115”.

[3] Pass level; latch-up testing according to Ref. 8 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[4] According to the store and transport requirements (see Ref. 11 “UM10569”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

# 11. Static characteristics

**Table 20. Static characteristics**

*$V_{DD}$ = 1.8 V to 5.5 V; $V_{SS}$ = 0 V; $V_{LCD}$ = 2.5 V to 6.5 V; $T_{amb}$ = −40 °C to +85 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Supplies** | | | | | | | |
| $V_{DD}$ | supply voltage | | | 1.8 | - | 5.5 | V |
| $V_{LCD}$ | LCD supply voltage | | | 2.5 | - | 6.5 | V |
| $V_{POR}$ | power-on reset voltage | | | 1.0 | 1.3 | 1.6 | V |
| $I_{DD}$ | supply current | $f_{clk(ext)}$ = 1536 Hz | [1][2] | - | 3 | 5 | µA |
| $I_{DD(LCD)}$ | LCD supply current | $f_{clk(ext)}$ = 1536 Hz | [1] | - | 25 | 30 | µA |
| **Logic** | | | | | | | |
| $V_I$ | input voltage | | | $V_{SS}$ − 0.5 | - | $V_{DD}$ + 0.5 | V |
| $V_{IL}$ | LOW-level input voltage | on pins CLK, $\overline{SYNC}$, OSC, A0 to A2, SA0 | | $V_{SS}$ | - | $0.3V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | on pins CLK, $\overline{SYNC}$, OSC, A0 to A2, SA0 | | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $V_O$ | output voltage | | | −0.5 | - | $V_{DD}$ + 0.5 | V |
| $V_{OH}$ | HIGH-level output voltage | | | $0.8V_{DD}$ | - | - | V |
| $V_{OL}$ | LOW-level output voltage | | | - | - | $0.2V_{DD}$ | V |
| $I_L$ | leakage current | on pins OSC, CLK, SCL, SDA, A0 to A2, SA0; $V_I = V_{DD}$ or $V_{SS}$ | | −1 | - | +1 | µA |
| $I_{OL}$ | LOW-level output current | output sink current; on pins CLK, $\overline{SYNC}$; $V_{OL}$ = 0.4 V; $V_{DD}$ = 5 V | | 1 | - | - | mA |
| $I_{OH}$ | HIGH-level output current | output source current; on pin CLK; $V_{OH}$ = 4.6 V; $V_{DD}$ = 5 V | | 1 | - | - | mA |
| $C_I$ | input capacitance | | [3] | - | - | 7 | pF |
| **$I^2C$-bus**[4] | | | | | | | |
| $I_{OL(SDA)}$ | LOW-level output current on pin SDA | $V_{OL}$ = 0.4 V; $V_{DD}$ = 5 V | | 3 | - | - | mA |
| Input on pins SDA and SCL | | | | | | | |
| $V_I$ | input voltage | | | $V_{SS}$ − 0.5 | - | 5.5 | V |
| $V_{IL}$ | LOW-level input voltage | | | $V_{SS}$ | - | $0.3V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | $0.7V_{DD}$ | - | 5.5 | V |
| $I_{LI}$ | input leakage current | $V_I = V_{DD}$ or $V_{SS}$ | | −1 | - | +1 | µA |
| $C_I$ | input capacitance | | [3] | - | - | 7 | pF |


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

**Table 20. Static characteristics** *...continued*

*$V_{DD}$ = 1.8 V to 5.5 V; $V_{SS}$ = 0 V; $V_{LCD}$ = 2.5 V to 6.5 V; $T_{amb}$ = −40 °C to +85 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **LCD outputs** | | | | | | | |
| Output pins BP0 to BP3 and S0 to S79 | | | | | | | |
| $\Delta V_O$ | output voltage variation | on pins BP0 to BP3; $C_{bpl}$ = 35 nF | [5] | −100 | - | +100 | mV |
| | | on pins S0 to S79; $C_{sgm}$ = 5 nF | [6] | −100 | - | +100 | mV |
| $R_O$ | output resistance | $V_{LCD}$ = 5 V | | | | | |
| | | on pins BP0 to BP3 | [7] | - | 1.5 | 10 | kΩ |
| | | on pins S0 to S79 | [7] | - | 6.0 | 13.5 | kΩ |

[1] LCD outputs are open-circuit; inputs at $V_{SS}$ or $V_{DD}$; external clock with 50 % duty factor; $I^2C$-bus inactive.

[2] For typical values, see Figure 23.

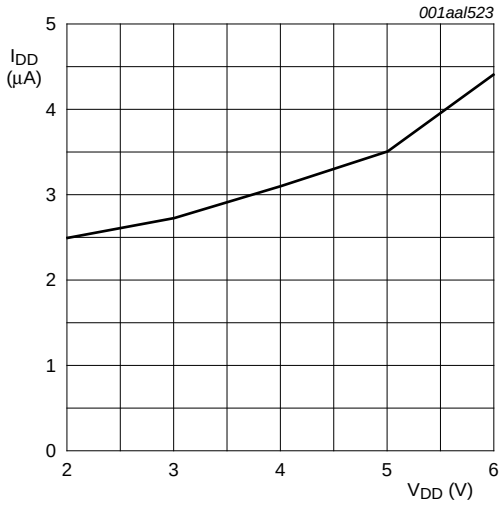
[3] Not tested, design specification only.

[4] The $I^2C$-bus interface of PCF8533 is 5 V tolerant.

[5] $C_{bpl}$ = backplane capacitance.

[6] $C_{sgm}$ = segment capacitance.

[7] Outputs measured individually and sequentially.




$T_{amb}$ = 30 °C; 1:4 multiplex drive mode; $V_{LCD}$ = 6.5 V; $f_{clk(ext)}$ = 1.536 kHz; all RAM written with logic 1; no display connected; $I^2C$-bus inactive.

**Fig 23. Typical $I_{DD}$ with respect to $V_{DD}$**


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

# 12. Dynamic characteristics

**Table 21. Dynamic characteristics**

*$V_{DD}$ = 1.8 V to 5.5 V; $V_{SS}$ = 0 V; $V_{LCD}$ = 2.5 V to 6.5 V; $T_{amb}$ = −40 °C to +85 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Clock** | | | | | | | |
| $f_{clk(int)}$ | internal clock frequency | | [1][2] | 960 | 1536 | 3046 | Hz |
| $f_{clk(ext)}$ | external clock frequency | | [1][2] | 797 | 1536 | 3046 | Hz |
| $t_{clk(H)}$ | HIGH-level clock time | | | 130 | - | - | µs |
| $t_{clk(L)}$ | LOW-level clock time | | | 130 | - | - | µs |
| **Synchronization: input pin $\overline{SYNC}$** | | | | | | | |
| $t_{PD(SYNC_N)}$ | $\overline{SYNC}$ propagation delay | | | - | 30 | - | ns |
| $t_{SYNC_NL}$ | $\overline{SYNC}$ LOW time | | | 1 | - | - | µs |
| **Outputs: pins BP0 to BP3 and S0 to S79** | | | | | | | |
| $t_{PD(drv)}$ | driver propagation delay | $V_{LCD}$ = 5 V | | - | - | 30 | µs |
| **$I^2C$-bus: timing[3]; see Figure 25** | | | | | | | |
| Pin SCL | | | | | | | |
| $f_{SCL}$ | SCL clock frequency | | | - | - | 400 | kHz |
| $t_{LOW}$ | LOW period of the SCL clock | | | 1.3 | - | - | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | | | 0.6 | - | - | µs |
| Pin SDA | | | | | | | |
| $t_{SU;DAT}$ | data set-up time | | | 100 | - | - | ns |
| $t_{HD;DAT}$ | data hold time | | | 0 | - | - | ns |
| Pins SCL and SDA | | | | | | | |
| $t_{BUF}$ | bus free time between a STOP and START condition | | | 1.3 | - | - | µs |
| $t_{SU;STO}$ | set-up time for STOP condition | | | 0.6 | - | - | µs |
| $t_{HD;STA}$ | hold time (repeated) START condition | | | 0.6 | - | - | µs |
| $t_{SU;STA}$ | set-up time for a repeated START condition | | | 0.6 | - | - | µs |
| $t_r$ | rise time of both SDA and SCL signals | $f_{SCL}$ = 400 kHz | | - | - | 0.3 | µs |
| | | $f_{SCL}$ < 125 kHz | | - | - | 1.0 | µs |
| $t_f$ | fall time of both SDA and SCL signals | | | - | - | 0.3 | µs |
| $C_b$ | capacitive load for each bus line | | | - | - | 400 | pF |
| $t_{w(spike)}$ | spike pulse width | on bus | | - | - | 50 | ns |

[1] Typical output duty cycle of 50 %.

[2] The corresponding frame frequency is $f_{fr} = f_{clk}/24$.

[3] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to $V_{IL}$ and $V_{IH}$ with an input voltage swing of $V_{SS}$ to $V_{DD}$.


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

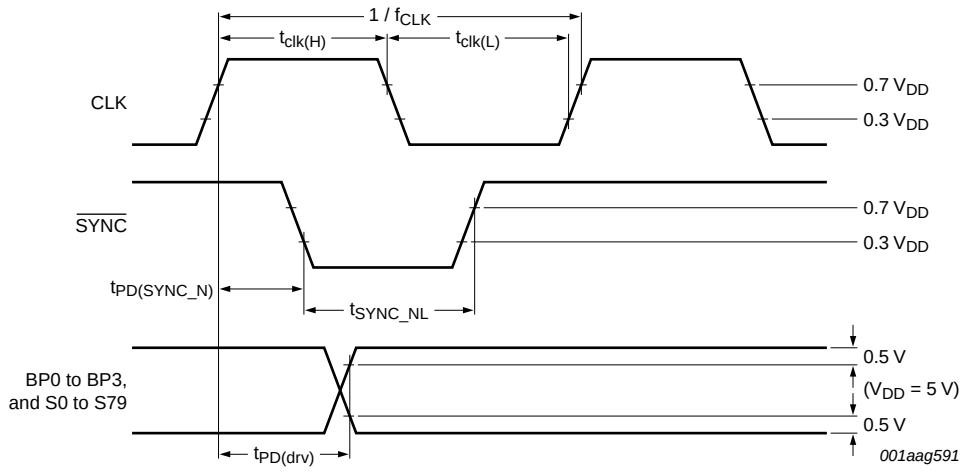



**Fig 24. Driver timing waveforms**

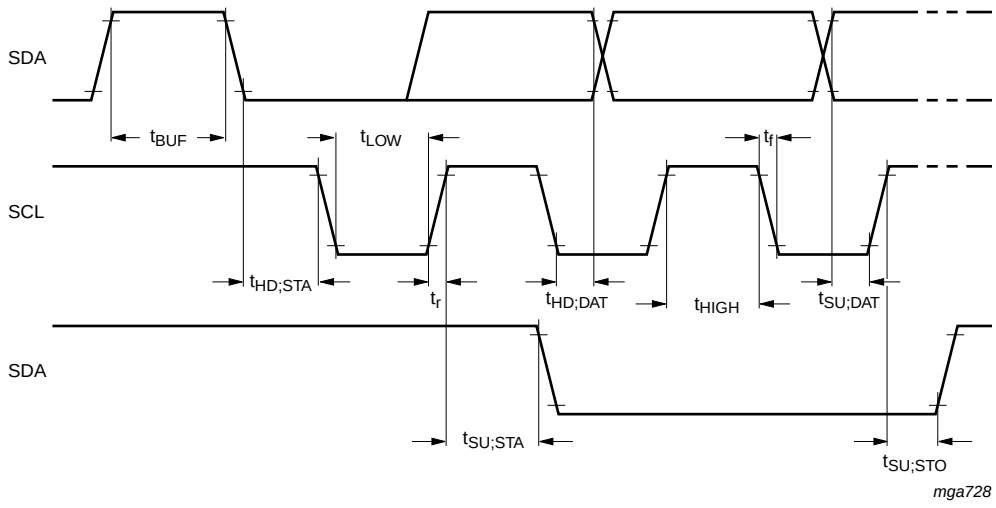



**Fig 25. I²C-bus timing waveforms**


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

# 13. Application information

## 13.1 Cascaded operation

Large display configurations of up to sixteen PCF8533 can be recognized on the same $I^2C$-bus by using the 3-bit hardware subaddress (A0, A1 and A2) and the programmable $I^2C$-bus slave address (SA0).

**Table 22. Addressing cascaded PCF8533**

| Cluster | Bit SA0 | Pin | | | Device |
|---|---|---|---|---|---|
| | | A2 | A1 | A0 | |
| 1 | 0 | 0 | 0 | 0 | 0 |
| | | 0 | 0 | 1 | 1 |
| | | 0 | 1 | 0 | 2 |
| | | 0 | 1 | 1 | 3 |
| | | 1 | 0 | 0 | 4 |
| | | 1 | 0 | 1 | 5 |
| | | 1 | 1 | 0 | 6 |
| | | 1 | 1 | 1 | 7 |
| 2 | 1 | 0 | 0 | 0 | 8 |
| | | 0 | 0 | 1 | 9 |
| | | 0 | 1 | 0 | 10 |
| | | 0 | 1 | 1 | 11 |
| | | 1 | 0 | 0 | 12 |
| | | 1 | 0 | 1 | 13 |
| | | 1 | 1 | 0 | 14 |
| | | 1 | 1 | 1 | 15 |

When cascaded PCF8533 are synchronized, they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8533 of the cascade contribute additional segment outputs, but their backplane outputs are left open-circuit (see Figure 26).


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

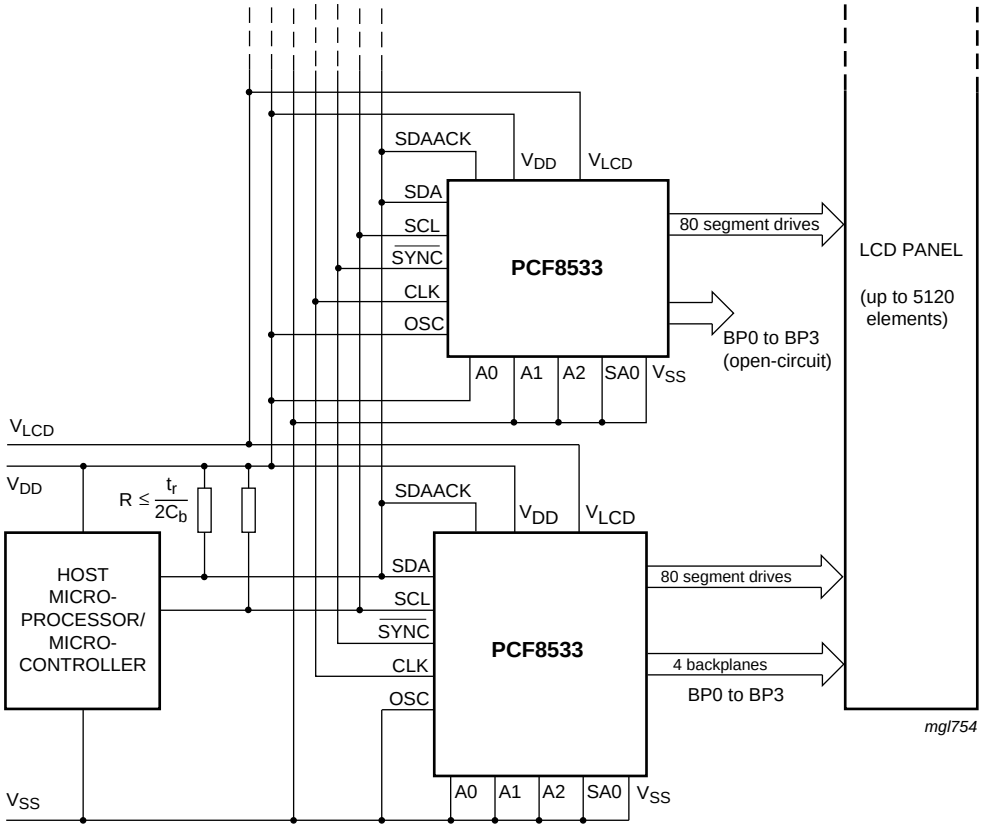



**Fig 26. Cascaded PCF8533 configuration**

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCF8533. This synchronization is guaranteed after the Power-On Reset (POR). The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidentally lost (for example, by noise in adverse electrical environments, or by the definition of a multiplex mode when PCF8533 with different SA0 levels are cascaded).

$\overline{\text{SYNC}}$ is organized as an input/output pin; the output selection being realized as an open-drain driver with an internal pull-up resistor. A PCF8533 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8533 to assert $\overline{\text{SYNC}}$. The timing relationships between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8533 are shown in Figure 27.


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

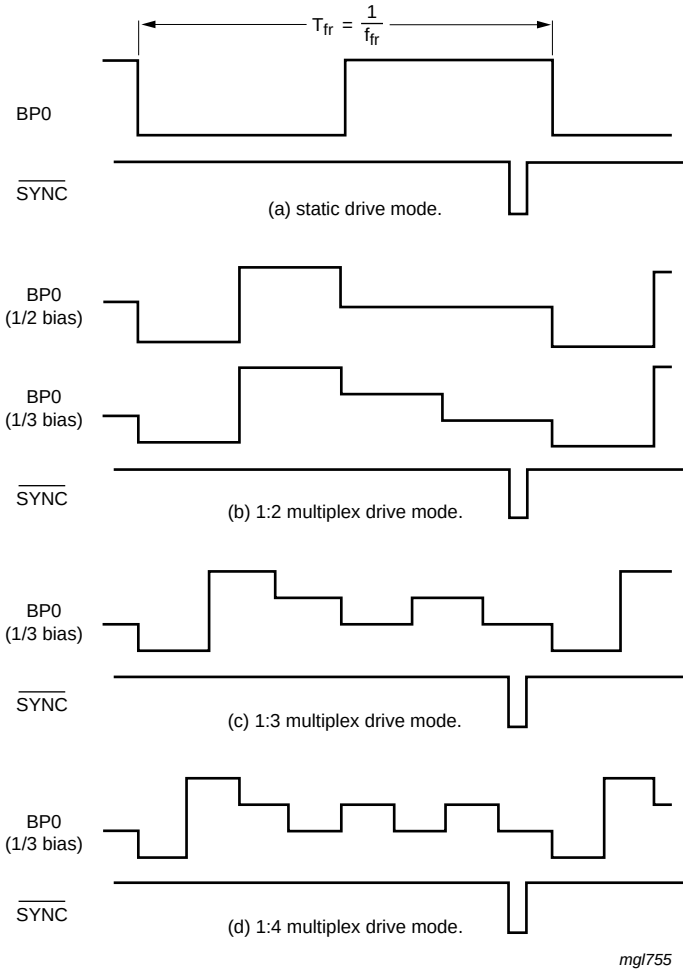



**Fig 27. Synchronization of the cascade for the various PCF8533 drive modes**

The contact resistance between the $\overline{\text{SYNC}}$ pins of cascaded devices must be controlled. If the resistance is too high, then the device will not be able to synchronize properly. This is particularly applicable to COG applications. Table 23 shows the limiting values for contact resistance.

**Table 23. $\overline{\text{SYNC}}$ contact resistance**

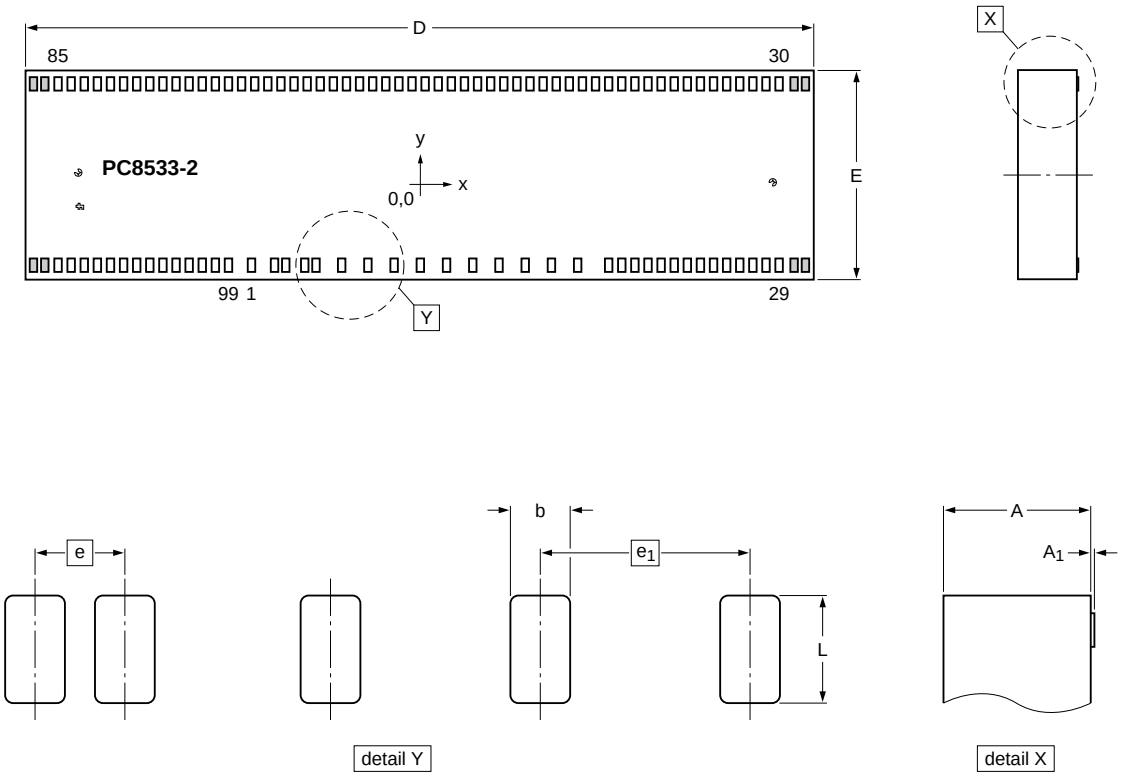
| Number of devices | Maximum contact resistance |
|---|---|
| 2 | 6000 Ω |
| 3 to 5 | 2200 Ω |
| 6 to 10 | 1200 Ω |
| 11 to 16 | 700 Ω |


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

## 14. Bare die outline

**Bare die; 99 bumps; 5.28 x 1.4 x 0.38 mm** **PCF8533-2**




Dimensions

| Unit | | A | $A_1$ | b | D | E | $e^{(1)}$ | $e_1{}^{(1)}$ | L |
|---|---|---|---|---|---|---|---|---|---|
| | max | | 0.020 | 0.053 | | | | 0.289 | 0.093 |
| mm | nom | 0.381 | 0.017 | 0.050 | 5.276 | 1.402 | | | 0.090 |
| | min | | 0.014 | 0.047 | | | 0.08 | | 0.087 |

Note

1. Dimension not drawn to scale

*pcf8533-2_do*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| PCF8533-2 | | | | | | ~~09-09-08~~ 10-01-28 |

**Fig 28. Bare die outline of PCF8533-2**


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

**Table 24. Bump locations**

*All x/y coordinates represent the position of the centre of each bump with respect to the center (x/y = 0) of the chip; see Figure 28.*

| Symbol | Bump | X (μm) | Y (μm) | | Description |
|---|---|---|---|---|---|
| SDAACK | 1 | −1079.20 | −594.40 | [1] | I²C-bus acknowledge output |
| SDA | 2 | −839.20 | −594.40 | [1] | I²C-bus serial data input |
| SDA | 3 | −759.20 | −594.40 | [1] | |
| SCL | 4 | −599.20 | −594.40 | | I²C-bus serial clock input |
| SCL | 5 | −519.20 | −594.40 | | |
| CLK | 6 | −414.80 | −594.40 | | clock input/output |
| $V_{DD}$ | 7 | −284.80 | −594.40 | | supply voltage |
| $\overline{SYNC}$ | 8 | 4.20 | −594.40 | | cascade synchronization input/output |
| OSC | 9 | 119.20 | −594.40 | | oscillator select |
| A0 | 10 | 249.20 | −594.40 | | subaddress input |
| A1 | 11 | 379.20 | −594.40 | | |
| A2 | 12 | 581.20 | −594.40 | | |
| SA0 | 13 | 711.20 | −594.40 | | I²C-bus slave address input; bit 0 |
| $V_{SS}$ | 14 | 841.20 | −594.40 | | ground supply voltage |
| $V_{LCD}$ | 15 | 1099.60 | −594.40 | | LCD supply voltage |
| BP2 | 16 | 1277.60 | −594.40 | | LCD backplane output |
| BP0 | 17 | 1357.60 | −594.40 | | |
| S0 | 18 | 1437.60 | −594.40 | | LCD segment output |
| S1 | 19 | 1517.60 | −594.40 | | |
| S2 | 20 | 1597.60 | −594.40 | | |
| S3 | 21 | 1677.60 | −594.40 | | |
| S4 | 22 | 1757.60 | −594.40 | | |
| S5 | 23 | 1837.60 | −594.40 | | |
| S6 | 24 | 1917.60 | −594.40 | | |
| S7 | 25 | 1997.60 | −594.40 | | |
| S8 | 26 | 2077.60 | −594.40 | | |
| S9 | 27 | 2157.60 | −594.40 | | |
| S10 | 28 | 2237.60 | −594.40 | | |
| S11 | 29 | 2317.60 | −594.40 | | |
| S12 | 30 | 2357.60 | 594.40 | | |
| S13 | 31 | 2277.60 | 594.40 | | |
| S14 | 32 | 2197.60 | 594.40 | | |
| S15 | 33 | 2117.60 | 594.40 | | |
| S16 | 34 | 2037.60 | 594.40 | | |
| S17 | 35 | 1957.60 | 594.40 | | |
| S18 | 36 | 1877.60 | 594.40 | | |
| S19 | 37 | 1797.60 | 594.40 | | |
| S20 | 38 | 1717.60 | 594.40 | | |
| S21 | 39 | 1637.60 | 594.40 | | |


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

**Table 24. Bump locations**

*All x/y coordinates represent the position of the centre of each bump with respect to the center (x/y = 0) of the chip; see Figure 28.*

| Symbol | Bump | X (μm) | Y (μm) | Description |
|---|---|---|---|---|
| S22 | 40 | 1557.60 | 594.40 | LCD segment output |
| S23 | 41 | 1477.60 | 594.40 | |
| S24 | 42 | 1317.60 | 594.40 | |
| S25 | 43 | 1237.60 | 594.40 | |
| S26 | 44 | 1157.60 | 594.40 | |
| S27 | 45 | 1077.60 | 594.40 | |
| S28 | 46 | 997.60 | 594.40 | |
| S29 | 47 | 917.60 | 594.40 | |
| S30 | 48 | 837.60 | 594.40 | |
| S31 | 49 | 757.60 | 594.40 | |
| S32 | 50 | 677.60 | 594.40 | |
| S33 | 51 | 597.60 | 594.40 | |
| S34 | 52 | 437.60 | 594.40 | |
| S35 | 53 | 357.60 | 594.40 | |
| S36 | 54 | 277.60 | 594.40 | |
| S37 | 55 | 197.60 | 594.40 | |
| S38 | 56 | 117.60 | 594.40 | |
| S39 | 57 | 37.60 | 594.40 | |
| S40 | 58 | −42.40 | 594.40 | |
| S41 | 59 | −122.40 | 594.40 | |
| S42 | 60 | −202.40 | 594.40 | |
| S43 | 61 | −282.40 | 594.40 | |
| S44 | 62 | −362.40 | 594.40 | |
| S45 | 63 | −442.40 | 594.40 | |
| S46 | 64 | −602.40 | 594.40 | |
| S47 | 65 | −682.40 | 594.40 | |
| S48 | 66 | −762.40 | 594.40 | |
| S49 | 67 | −842.40 | 594.40 | |
| S50 | 68 | −922.40 | 594.40 | |
| S51 | 69 | −1002.40 | 594.40 | |
| S52 | 70 | −1082.40 | 594.40 | |
| S53 | 71 | −1162.40 | 594.40 | |
| S54 | 72 | −1242.40 | 594.40 | |
| S55 | 73 | −1322.40 | 594.40 | |
| S56 | 74 | −1402.40 | 594.40 | |
| S57 | 75 | −1562.40 | 594.40 | |
| S58 | 76 | −1642.40 | 594.40 | |
| S59 | 77 | −1722.40 | 594.40 | |
| S60 | 78 | −1802.40 | 594.40 | |


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

**Table 24. Bump locations**

*All x/y coordinates represent the position of the centre of each bump with respect to the center (x/y = 0) of the chip; see Figure 28.*

| Symbol | Bump | X (μm) | Y (μm) | | Description |
|---|---|---|---|---|---|
| S61 | 79 | −1882.40 | 594.40 | | LCD segment output |
| S62 | 80 | −1962.40 | 594.40 | | |
| S63 | 81 | −2042.40 | 594.40 | | |
| S64 | 82 | −2122.40 | 594.40 | | |
| S65 | 83 | −2202.40 | 594.40 | | |
| S66 | 84 | −2282.40 | 594.40 | | |
| S67 | 85 | −2362.40 | 594.40 | | |
| S68 | 86 | −2322.40 | −594.40 | | |
| S69 | 87 | −2242.40 | −594.40 | | |
| S70 | 88 | −2162.40 | −594.40 | | |
| S71 | 89 | −2082.40 | −594.40 | | |
| S72 | 90 | −2002.40 | −594.40 | | |
| S73 | 91 | −1922.40 | −594.40 | | |
| S74 | 92 | −1842.40 | −594.40 | | |
| S75 | 93 | −1762.40 | −594.40 | | |
| S76 | 94 | −1682.40 | −594.40 | | |
| S77 | 95 | −1602.40 | −594.40 | | |
| S78 | 96 | −1522.40 | −594.40 | | |
| S79 | 97 | −1442.40 | −594.40 | | |
| BP3 | 98 | −1362.40 | −594.40 | | LCD backplane output |
| BP1 | 99 | −1282.40 | −594.40 | | |
| D1 | - | 2469.70 | −594.40 | [2] | dummy bump |
| D2 | - | 2549.70 | −594.40 | | |
| D3 | - | 2517.60 | 594.40 | | |
| D4 | - | 2437.60 | 594.40 | | |
| D5 | - | −2442.30 | 594.40 | | |
| D6 | - | −2522.30 | 594.40 | | |
| D7 | - | −2554.40 | −594.40 | | |
| D8 | - | −2474.40 | −594.40 | | |

[1] For most applications SDA and SDAACK are shorted together; see Section 8.1.

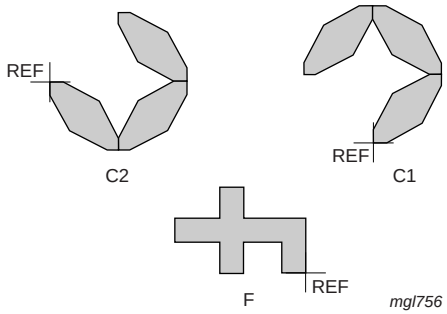
[2] The dummy bumps are connected to the adjacent segments but are not tested.

**Table 25. Alignment mark locations**

| Symbol | X (μm) | Y (μm) |
|---|---|---|
| C1 | 2300.5 | 55.0 |
| C2 | −2320.2 | 107.0 |
| F | −2208.3 | −165.4 |


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.




The positions of the alignment marks are shown in Figure 2 and Figure 28.

**Fig 29. Alignment marks of PCF8533**

**Table 26. Gold bump hardness**

| Type number | Min | Max | Unit[1] |
|---|---|---|---|
| PCF8533U/2/F2 | 60 | 120 | HV |

[1] Pressure of diamond head: 10 g to 50 g.

## 15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

# 16. Packing information

## 16.1 Tray information

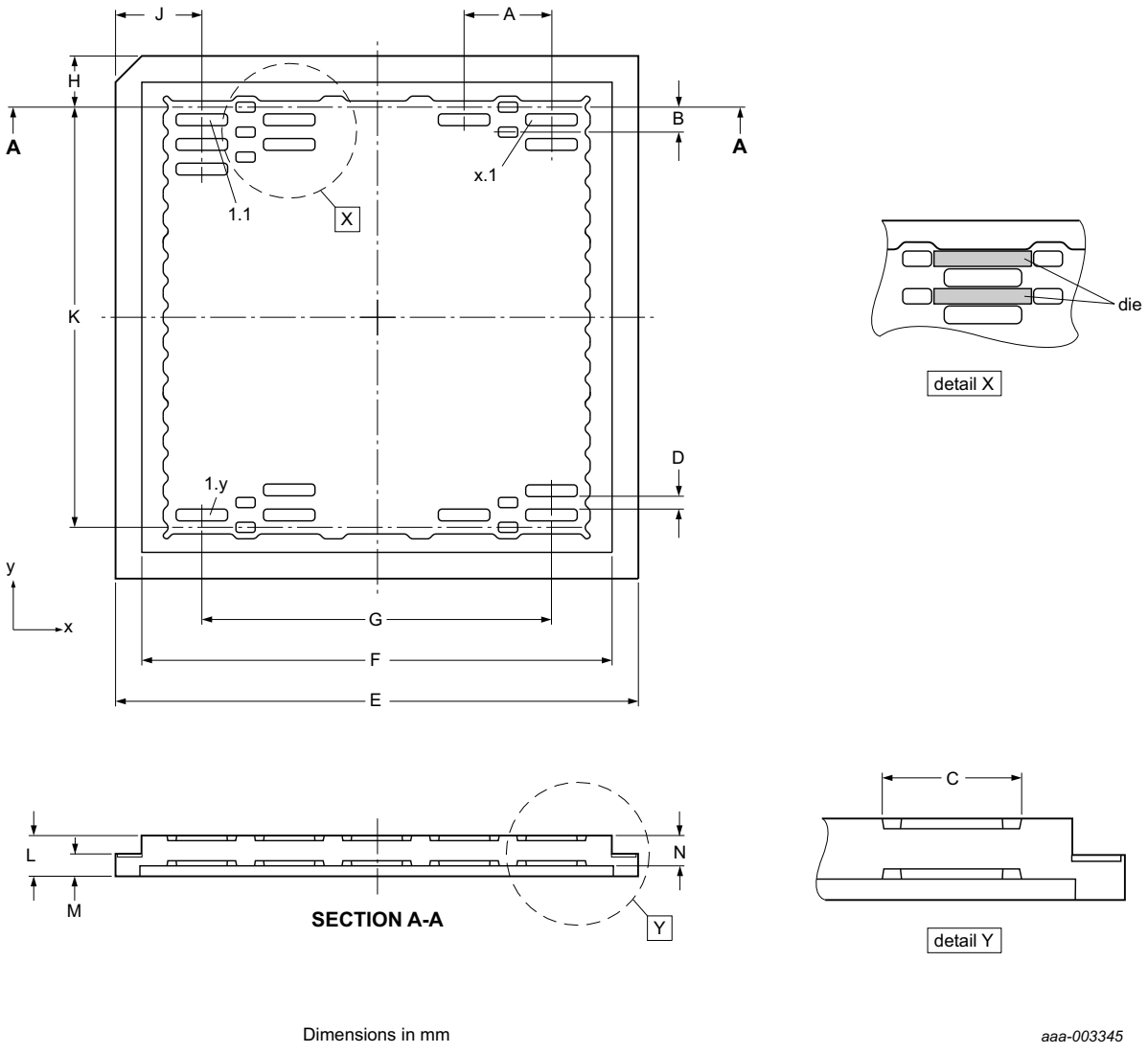



**Fig 30. Tray details**

**Table 27. Description of tray details**

*Tray details are shown in Figure 30.*

| Tray details | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Dimensions** | | | | | | | | | | | | | |
| A | B | C | D | E | F | G | H | J | K | L | M | N | Unit |
| 7.0 | 2.4 | 5.38 | 1.50 | 50.8 | 45.72 | 35.0 | 5.0 | 7.9 | 40.8 | 3.96 | 2.18 | 2.49 | mm |
| **Number of pockets** | | | | | | | | | | | | | |
| x direction | | | | | | | y direction | | | | | | |
| 6 | | | | | | | 18 | | | | | | |


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

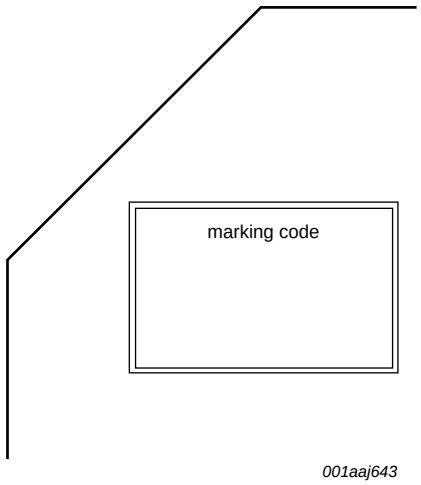



**Fig 31. Tray alignment**

The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to Figure 28 for the orientation and position of the type name on the die surface.


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

# 17. Abbreviations

**Table 28. Abbreviations**

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| COG | Chip-On-Glass |
| DC | Direct Current |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| $I^2C$ | Inter-Integrated Circuit bus |
| IC | Integrated Circuit |
| ITO | Indium Tin Oxide |
| LCD | Liquid Crystal Display |
| LSB | Least Significant Bit |
| MM | Machine Model |
| MOS | Metal-Oxide Semiconductor |
| MSB | Most Significant Bit |
| POR | Power-On Reset |
| RC | Resistance-Capacitance |
| RAM | Random Access Memory |
| RMS | Root Mean Square |
| SCL | Serial CLock line |
| SDA | Serial DAta line |


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

## 18. References

[1] **AN10170 —** Design guidelines for COG modules with NXP monochrome LCD drivers

[2] **AN10706 —** Handling bare die

[3] **AN10853 —** ESD and EMC sensitivity of IC

[4] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[5] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[6] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[7] **JESD22-A115 —** Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[8] **JESD78 —** IC Latch-Up Test

[9] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[10] **UM10204 —** $I^2C$-bus specification and user manual

[11] **UM10569 —** Store and transport requirements


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

# 19. Revision history

**Table 29. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PCF8533 v.6 | 20121001 | Product data sheet | - | PCF8533 v.5 |
| Modifications: | • Removed withdrawn product type<br>• Adjusted values for $I_{DD}$ and $I_{DD(LCD)}$ in Table 20<br>• Changed tray information (Section 16.1)<br>• Added ordering options (Section 3.1)<br>• Enhanced display RAM description (Section 7.6)<br>• Improved description of bit E (Table 6) | | | |
| PCF8533 v.5 | 20110629 | Product data sheet | - | PCF8533_4 |
| PCF8533_4 | 20100305 | Product data sheet | - | PCF8533_3 |
| PCF8533_3 | 20080424 | Product data sheet | - | PCF8533_2 |
| PCF8533_2 | 19990730 | Product specification | - | PCF8533_SDS_1 |
| PCF8533_SDS_1 | 19990312 | Product specification | - | - |


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

# 20. Legal information

## 20.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 20.2 Definitions

**Draft —** The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet —** A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification —** The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

## 20.3 Disclaimers

**Limited warranty and liability —** Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes —** NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use —** NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications —** Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values —** Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale —** NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license —** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

**Export control —** This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products —** Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations —** A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

**Bare die —** All die are tested on compliance with their related technical specifications as stated in this data sheet up to the point of wafer sawing and are handled in accordance with the NXP Semiconductors storage and transportation conditions. If there are data sheet limits not guaranteed, these will be separately indicated in the data sheet. There are no post-packing tests performed on individual die or wafers.

NXP Semiconductors has no control of third party procedures in the sawing, handling, packing or assembly of the die. Accordingly, NXP Semiconductors assumes no liability for device functionality or performance of the die or systems after third party sawing, handling, packing or assembly of the die. It is the responsibility of the customer to test and qualify their application in which the die is used.

All die sales are conditioned upon and subject to the customer entering into a written die sale agreement with NXP Semiconductors through its legal department.

### 20.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**$I^2C$-bus —** logo is a trademark of NXP B.V.

## 21. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

## 22. Tables

Table 1. Ordering information . . . . . .2
Table 2. Ordering options . . . . . .2
Table 3. Marking codes . . . . . .2
Table 4. Pin description overview . . . . . .4
Table 5. Definition of commands . . . . . .5
Table 6. Mode-set command bit description . . . . . .5
Table 7. Load-data-pointer command bit description . . .6
Table 8. Device-select command bit description . . . . . .6
Table 9. Bank-select command bit description . . . . . .6
Table 10. Blink-select command bit description . . . . . .7
Table 11. Blink frequencies . . . . . .7
Table 12. Selection of possible display configurations . . . .9
Table 13. Biasing characteristics . . . . . .10
Table 14. LCD frame frequency . . . . . .17
Table 15. Standard RAM filling in 1:3 multiplex drive mode . . . . . .21
Table 16. Entire RAM filling by rewriting in 1:3 multiplex drive mode . . . . . .22
Table 17. $I^2C$ slave address byte . . . . . .28
Table 18. Control byte description . . . . . .29
Table 19. Limiting values . . . . . .32
Table 20. Static characteristics . . . . . .33
Table 21. Dynamic characteristics . . . . . .35
Table 22. Addressing cascaded PCF8533 . . . . . .37
Table 23. $\overline{SYNC}$ contact resistance . . . . . .39
Table 24. Bump locations . . . . . .41
Table 25. Alignment mark locations . . . . . .43
Table 26. Gold bump hardness . . . . . .44
Table 27. Description of tray details . . . . . .45
Table 28. Abbreviations . . . . . .47
Table 29. Revision history . . . . . .49


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

## 23. Figures

Fig 1. Block diagram of PCF8533 . . . . . .3
Fig 2. Pin configuration for PCF8533U . . . . . .4
Fig 3. Example of displays suitable for PCF8533 . . . . . .8
Fig 4. Typical system configuration . . . . . .9
Fig 5. Electro-optical characteristic: relative transmission curve of the liquid . . . . . .11
Fig 6. Static drive mode waveforms . . . . . .12
Fig 7. Waveforms for the 1:2 multiplex drive mode with $\frac{1}{2}$ bias . . . . . .13
Fig 8. Waveforms for the 1:2 multiplex drive mode with $\frac{1}{3}$ bias . . . . . .14
Fig 9. Waveforms for the 1:3 multiplex drive mode with $\frac{1}{3}$ bias . . . . . .15
Fig 10. Waveforms for the 1:4 multiplex drive mode with $\frac{1}{3}$ bias . . . . . .16
Fig 11. Display RAM bitmap . . . . . .19
Fig 12. Relationships between LCD layout, drive mode, display RAM filling order, and display data transmitted over the $I^2C$-bus . . . . . .20
Fig 13. RAM banks in static and multiplex driving mode 1:2 . . . . . .24
Fig 14. Bank selection . . . . . .24
Fig 15. Example of the Bank-select command with multiplex drive mode 1:2 . . . . . .25
Fig 16. Bit transfer . . . . . .26
Fig 17. Definition of START and STOP conditions. . . . . .27
Fig 18. System configuration . . . . . .27
Fig 19. Acknowledgement on the $I^2C$-bus . . . . . .28
Fig 20. $I^2C$-bus protocol . . . . . .29
Fig 21. Control byte format . . . . . .29
Fig 22. Device protection diagram . . . . . .31
Fig 23. Typical $I_{DD}$ with respect to $V_{DD}$ . . . . . .34
Fig 24. Driver timing waveforms . . . . . .36
Fig 25. $I^2C$-bus timing waveforms . . . . . .36
Fig 26. Cascaded PCF8533 configuration. . . . . .38
Fig 27. Synchronization of the cascade for the various PCF8533 drive modes . . . . . .39
Fig 28. Bare die outline of PCF8533-2 . . . . . .40
Fig 29. Alignment marks of PCF8533 . . . . . .44
Fig 30. Tray details . . . . . .45
Fig 31. Tray alignment . . . . . .46


All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

## 24. Contents

**1 General description . . . . . 1**
**2 Features and benefits . . . . . 1**
**3 Ordering information . . . . . 2**
3.1 Ordering options . . . . . 2
**4 Marking . . . . . 2**
**5 Block diagram . . . . . 3**
**6 Pinning information . . . . . 4**
6.1 Pinning . . . . . 4
6.2 Pin description . . . . . 4
**7 Functional description . . . . . 5**
7.1 Commands of PCF8533 . . . . . 5
7.1.1 Command: mode-set . . . . . 5
7.1.2 Command: load-data-pointer . . . . . 6
7.1.3 Command: device-select . . . . . 6
7.1.4 Command: bank-select . . . . . 6
7.1.5 Command: blink-select . . . . . 7
7.1.5.1 Blinking . . . . . 7
7.2 Power-On Reset (POR) . . . . . 8
7.3 Possible display configurations . . . . . 8
7.3.1 LCD bias generator . . . . . 9
7.3.2 LCD voltage selector . . . . . 9
7.3.2.1 Electro-optical performance . . . . . 11
7.3.3 LCD drive mode waveforms . . . . . 12
7.3.3.1 Static drive mode . . . . . 12
7.3.3.2 1:2 multiplex drive mode . . . . . 13
7.3.3.3 1:3 multiplex drive mode . . . . . 15
7.3.3.4 1:4 multiplex drive mode . . . . . 16
7.4 Oscillator . . . . . 17
7.4.1 Internal clock . . . . . 17
7.4.2 External clock . . . . . 17
7.4.3 Timing . . . . . 17
7.5 Backplane and segment outputs . . . . . 17
7.5.1 Backplane outputs . . . . . 18
7.5.2 Segment outputs . . . . . 18
7.6 Display RAM . . . . . 18
7.6.1 Data pointer . . . . . 21
7.6.2 Subaddress counter . . . . . 21
7.6.3 RAM writing in 1:3 multiplex drive mode . . . . . 21
7.6.4 Writing over the RAM address boundary . . . . 22
7.6.5 Bank selection . . . . . 23
7.6.5.1 Output bank selector . . . . . 23
7.6.5.2 Input bank selector . . . . . 23
7.6.5.3 RAM bank switching . . . . . 23
**8 I²C-bus interface . . . . . 26**
8.1 Characteristics of the I²C-bus . . . . . 26
8.1.1 Bit transfer . . . . . 26
8.1.2 START and STOP conditions . . . . . 26
8.1.3 System configuration . . . . . 27
8.1.4 Acknowledge . . . . . 27
8.1.5 I²C-bus controller . . . . . 28
8.1.6 Input filters . . . . . 28
8.1.7 I²C-bus protocol . . . . . 28
**9 Internal circuitry . . . . . 31**
**10 Limiting values . . . . . 32**
**11 Static characteristics . . . . . 33**
**12 Dynamic characteristics . . . . . 35**
**13 Application information . . . . . 37**
13.1 Cascaded operation . . . . . 37
**14 Bare die outline . . . . . 40**
**15 Handling information . . . . . 44**
**16 Packing information . . . . . 45**
16.1 Tray information . . . . . 45
**17 Abbreviations . . . . . 47**
**18 References . . . . . 48**
**19 Revision history . . . . . 49**
**20 Legal information . . . . . 50**
20.1 Data sheet status . . . . . 50
20.2 Definitions . . . . . 50
20.3 Disclaimers . . . . . 50
20.4 Trademarks . . . . . 51
**21 Contact information . . . . . 51**
**22 Tables . . . . . 52**
**23 Figures . . . . . 53**
**24 Contents . . . . . 54**

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2012. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 1 October 2012
Document identifier: PCF8533