

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9210P, TC9211P

ELECTRONIC VOLUME CONTROL IC

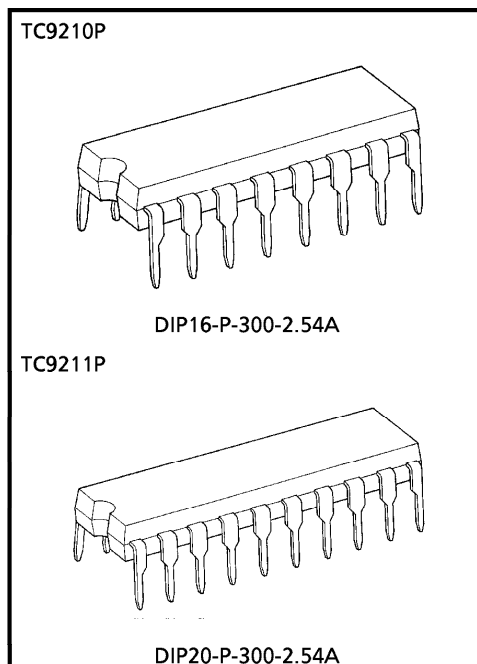
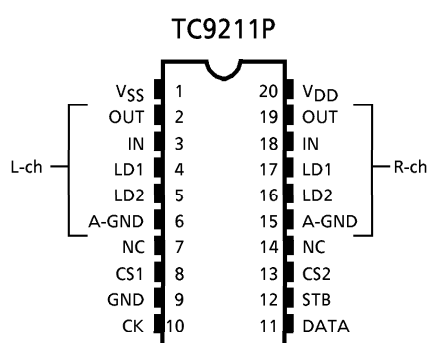
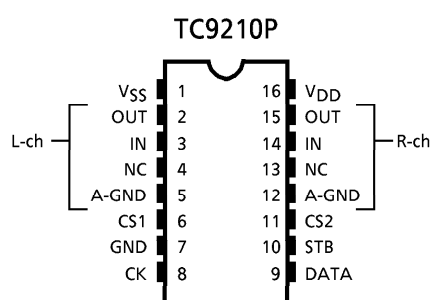
TC9210P and TC9211P are electronic volume control ICs developed for use in audio equipment such as home stereo sets.

The volume, balance and loudness circuits can be controlled by serial data which are input externally.

FEATURES

- Forty-level volume control in 2dB steps from 0dB to 78dB, ∞ dB.
- The volume circuit features 2 built-in channels which can be controlled independently, thus controlling balance.
- TC9211P features a built-in loudness circuit (20dB tap).
- Single and dual power supply operation.
- Chip select input allows control of up to four of these chips on the same bus.
- Polysilicon resistors enables low-distortion, high-performance volume systems.

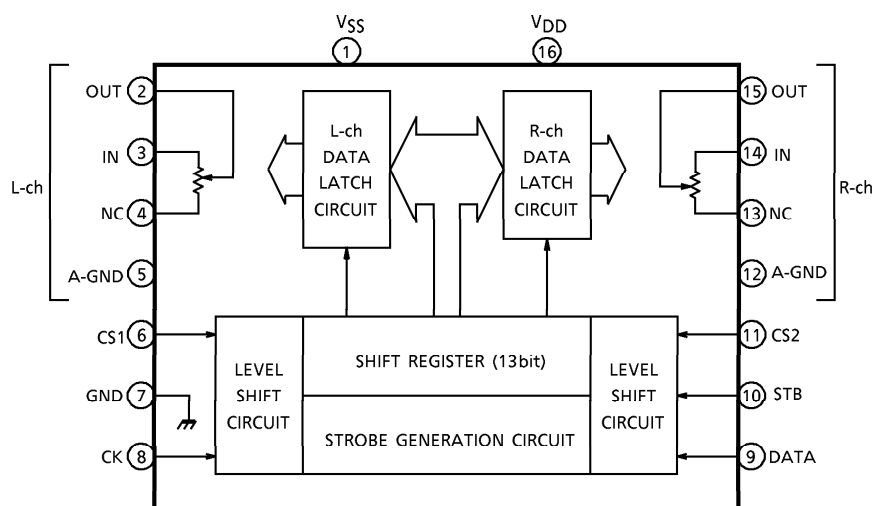
PIN CONNECTION



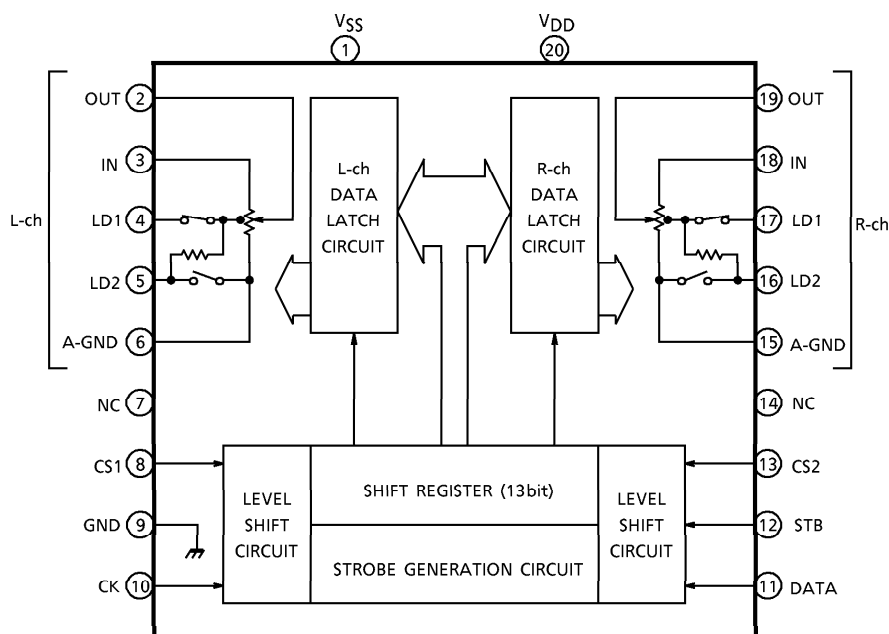
Weight

DIP16-P-300-2.54A : 1.0g (Typ.)
DIP20-P-300-2.54A : 1.4g (Typ.)

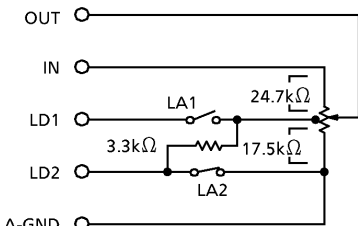
BLOCK DIAGRAM (TC9210P)



BLOCK DIAGRAM (TC9211P)



PIN FUNCTION NUMBERS IN PARENTHESES APPLY TO TC9210P

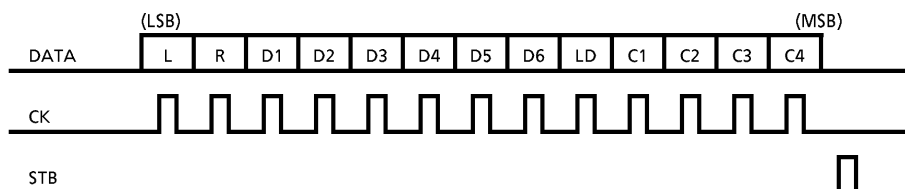
PIN NUMBER	SYMBOL	PIN NAME	FUNCTION AND OPERATION	NOTE									
1 (1)	V _{SS}	Negative power supply pin	Dual power supply V_{DD} = 6.0~17V GND = 0V V_{SS} = - 6.0~ - 17V	—									
9 (7)	GND	Digital ground pin											
20 (16)	V _{DD}	Positive power supply pin											
20 (16)	V _{DD}	Positive power supply pin	Single power supply V_{DD} = 6.0~18V GND = V_{SS} = 0V										
2 (2)	L-OUT	Volume output pins	● Volume circuit (TC9211P)  <table border="1" data-bbox="916 925 1219 1048"><thead><tr><th></th><th>LA1</th><th>LA2</th></tr></thead><tbody><tr><td>Loudness "ON"</td><td>ON</td><td>OFF</td></tr><tr><td>Loudness "OFF"</td><td>OFF</td><td>ON</td></tr></tbody></table>		LA1	LA2	Loudness "ON"	ON	OFF	Loudness "OFF"	OFF	ON	—
	LA1			LA2									
Loudness "ON"	ON			OFF									
Loudness "OFF"	OFF	ON											
19 (15)	R-OUT												
3 (3)	L-IN	Volume input pins											
18 (14)	R-IN												
4 (—)	L-LD1			Tap output pins for loudness									
17 (—)	R-LD1												
5 (—)	L-LD2												
16 (—)	R-LD2												
6 (5)	L-A-GND	Analog ground pins											
15 (12)	R-A-GND												
8 (6)	CS1	Chip select input pins	Switching chip select code allows control of up to 4 chips simultaneously on one bus.	—									
13 (11)	CS2												
10 (8)	CK	Clock input pin	Clock input for data transfer	Low threshold value input pins									
11 (9)	DATA	Data input pin	Serial data input for setting volume										
12 (10)	STB	Strobe input pin	Strobe input for writing data										
7, 14 (4, 13)	NC	Not connected		—									

OPERATIONAL DESCRIPTION

1. Setting volume values (attenuation)

The volume values are set using 13bit serial data.

- Data format



1) L is left-channel select data ; R is right-channel select data.

When L = 1, left-channel volume is set ; when R = 1, right-channel volume is set. (When R = L = 1, both channel volumes are set simultaneously).

2) LD is loudness setting data. When LD = 1, loudness is on. (Only for TC9211P. Set to 0 for TC9210P.)

3) D1-D6 are volume value setting data.

VOLUME VALUE	D1	D2	D3	D4	D5	D6
0dB	0	0	0	0	0	0
2	1	0	0	0	0	0
4	0	1	0	0	0	0
6	1	1	0	0	0	0
8	0	0	1	0	0	0
10	1	0	1	0	0	0
12	0	1	1	0	0	0
14	1	1	1	0	0	0
16	0	0	0	1	0	0
18	1	0	0	1	0	0
20	0	1	0	1	0	0
22	1	1	0	1	0	0
24	0	0	1	1	0	0
26	1	0	1	1	0	0
28	0	1	1	1	0	0
30	1	1	1	1	0	0
32	0	0	0	0	1	0
34	1	0	0	0	1	0
36	0	1	0	0	1	0
38	1	1	0	0	1	0

VOLUME VALUE	D1	D2	D3	D4	D5	D6
40dB	0	0	1	0	1	0
42	1	0	1	0	1	0
44	0	1	1	0	1	0
46	1	1	1	0	1	0
48	0	0	0	1	1	0
50	1	0	0	1	1	0
52	0	1	0	1	1	0
54	1	1	0	1	1	0
56	0	0	1	1	1	0
58	1	0	1	1	1	0
60	0	1	1	1	1	0
62	1	1	1	1	1	0
64	0	0	0	0	0	1
66	1	0	0	0	0	1
68	0	1	0	0	0	1
70	1	1	0	0	0	1
72	0	0	1	0	0	1
74	1	0	1	0	0	1
76	0	1	1	0	0	1
78	1	1	1	0	0	1
∞	0	0	0	1	0	1

(Note) Note that if data other than those listed above are input, volume values are undefined.

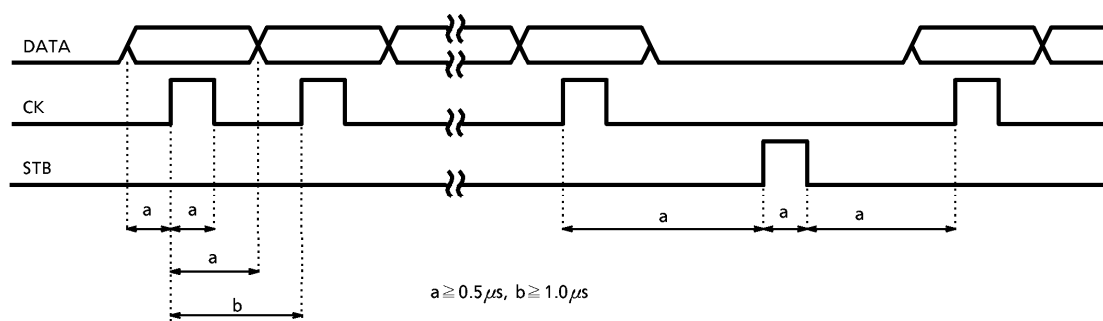
4) C1-C4 are chip select code data.

Code data are set according to CS1 and CS2 input.

CS1	CS2	C1	C2	C3	C4
L	L	0	0	1	1
H	L	1	0	1	1
L	H	0	1	1	1
H	H	1	1	1	1

2. Serial data timing

Input CK, DATA and STB according to the following timing.

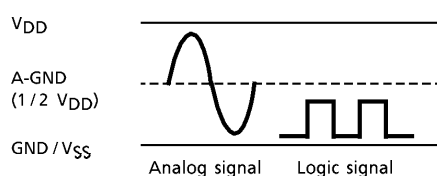


3. Single and dual power supply operation

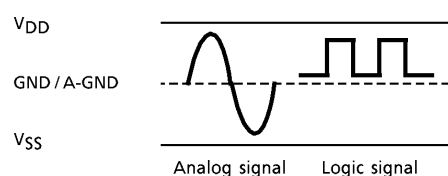
TC9210P and TC9211P can operate with single or dual power supplies.

With single or dual power supply, serial data logic level can be 0-5V.

• Single power supply operation



• Dual power supply operation



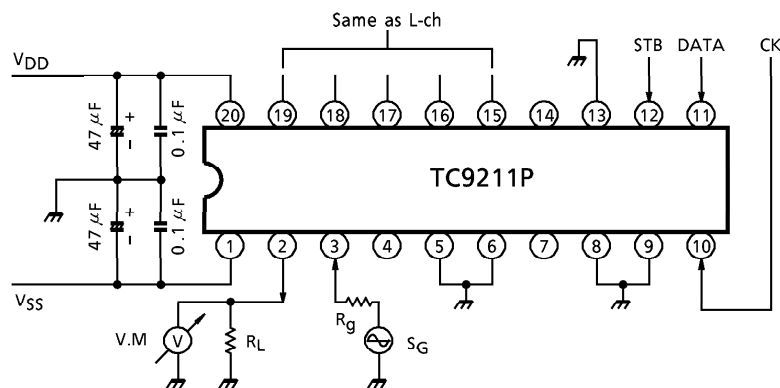
MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage (1)	V _{DD} -V _{SS}	- 0.3~36	V
Power Supply Voltage (2)	V _{DD} -GND	- 0.3~20	V
GND Input Voltage	V _{IN} (1)	- 0.3~V _{DD} + 0.3	V
V _{SS} Input Voltage	V _{IN} (2)	V _{SS} - 0.3~V _{DD} + 0.3	V
Power Dissipation	P _D	300	mW
Operating Temperature	T _{opr}	- 40~85	°C
Storage Temperature	T _{stg}	- 65~150	°C

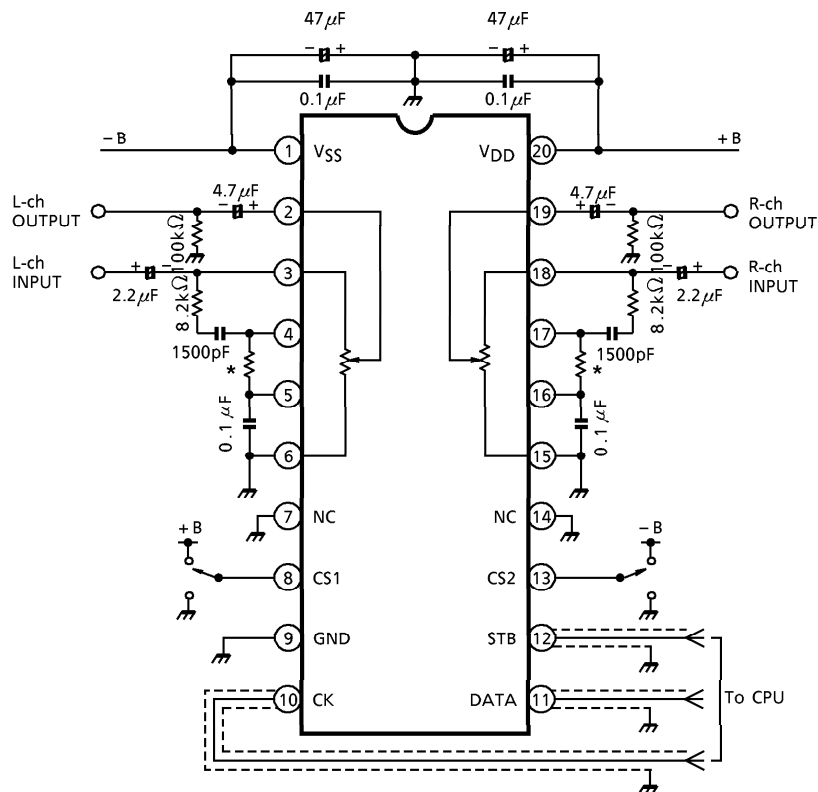
ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{DD} = 15V, V_{SS} = - 15V, GND = 0V, Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage (1)		V _{DD} -V _{SS}	—	Dual power supply operation		12	~	34	V
Operating Supply Voltage (2)		V _{DD} -GND	—	Single power supply operation		6.0	~	18	V
Operating Supply Current		I _{DD}	1	No load, No input		—	0.5	1.0	mA
Input Voltage	"H" Level	V _{IH} (1)	—	CK, DATA, STB terminal V _{DD} = 6.0~18V	4.0	~	V _{DD}	V	
	"L" Level	V _{IL} (1)			GND	~	1.0		
Input Voltage	"H" Level	V _{IH} (2)	—	CS1, CS2 terminal	V _{DD} × 0.7	~	V _{DD}	V	
	"L" Level	V _{IL} (2)			GND	~	V _{DD} × 0.3		
Input Current	"H" Level	I _{IH}	—	CK, DATA, STB, CS1, CS2 terminal	V _{IH} = 15V	− 1.0	~	1.0	μA
	"L" Level	I _{IL}			V _{IL} = 0V	− 1.0	~	1.0	
Operating Frequency Range		f _{op}	—	CK, DATA, STB terminal		0	~	1.0	MHz
Minimum Clock Frequency		T _{ck}				0.5	—	—	μs
Volume Resistance Value		R _{VR}	—	Loudness "OFF"		18.5	27.5	36.5	kΩ
Step Deviation		ΔVR	—	Volume step deviation		− 1.2	~	1.2	dB
Analog Switch ON Resistance		R _{ON}	—	Internal analog switch		—	350	600	Ω
Analog Switch OFF Leak Current		I _{OFF}				− 0.1	~	0.1	μA
Total Harmonic Distortion		THD	1	f _{IN} = 1kHz V _{IN} = 1V _{rms} R _g = 600Ω, R _L = 100kΩ BW = 20Hz~20kHz		—	0.005	—	%
Maximum Attenuation		ATT _{MAX}				—	100	—	dB
Output Noise Voltage		V _N				—	1.0	—	μV _{rms}
Cross Talk		C·T				—	100	—	dB

TEST CIRCUIT 1 ($I_{DD}/THD/ATT_{MAX}/V_N/C\cdot T$)



APPLICATION CIRCUIT (TC9211P)

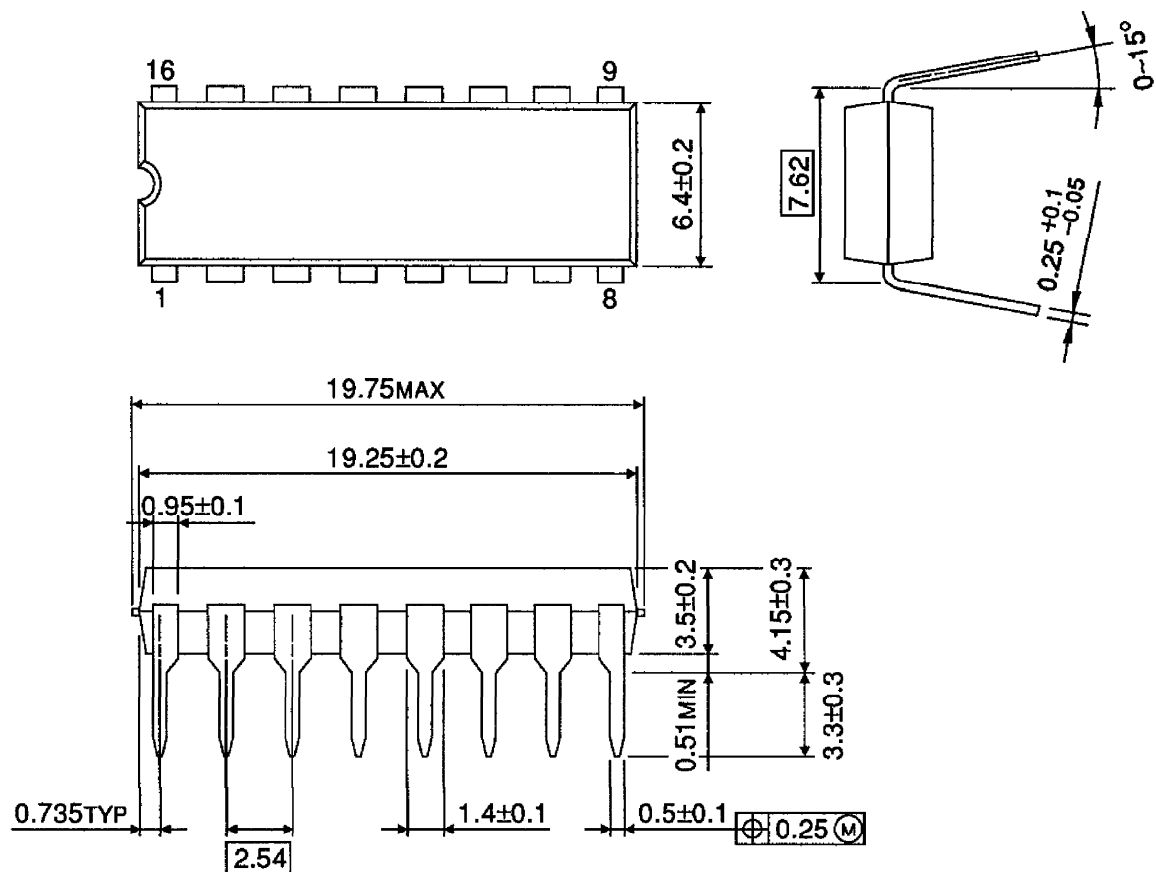


* For preventing noise when loudness is turned on or off. $R = 220k\Omega \sim 470k\Omega$

(Note) High-frequency digital signals are input to pins CK, DATA and STB. Since these signals may cause noise in analog circuits, either use shield wire for CK, DATA, and STB signal lines, or design the pattern so that these signal lines are protected by the ground line.

PACKAGE DIMENSIONS
DIP16-P-300-2.54A

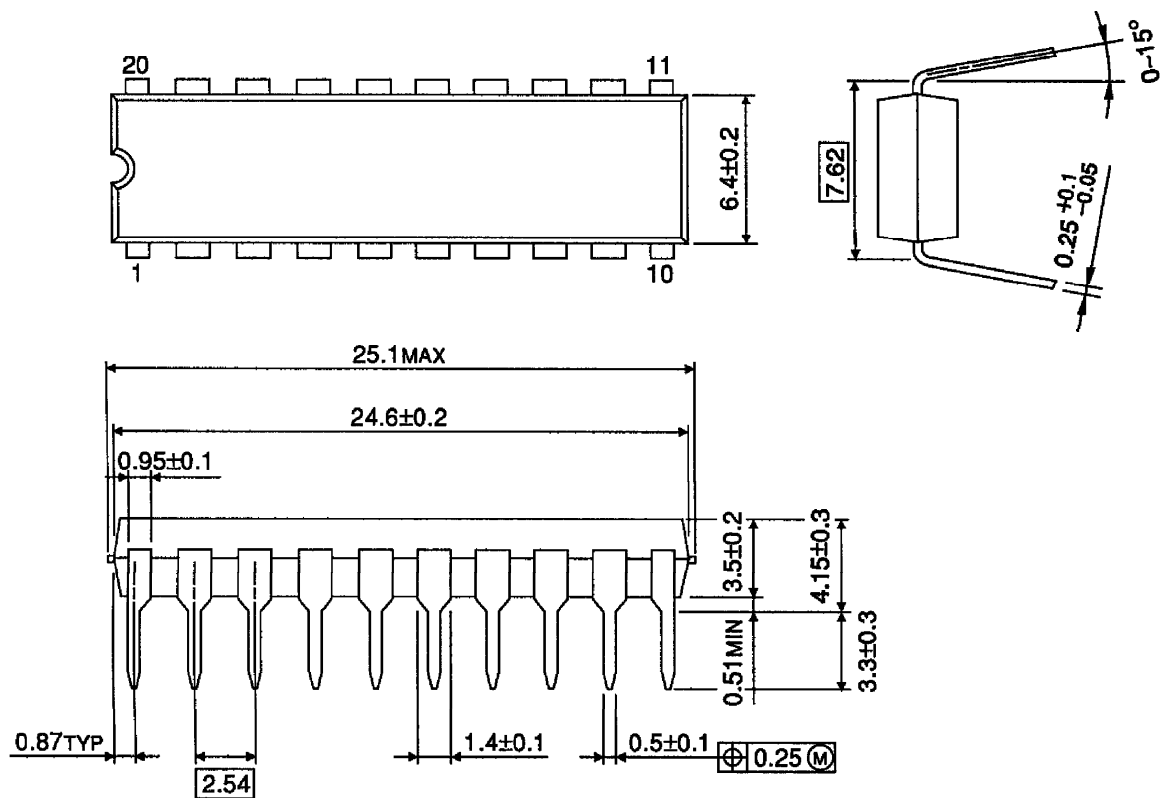
Unit : mm



Weight : 1.0g (Typ.)

PACKAGE DIMENSIONS
DIP20-P-300-2.54A

Unit : mm



Weight : 1.4g (Typ.)

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000707EBA

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