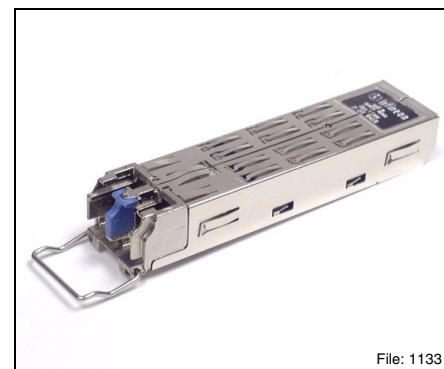


iSFP™ - Intelligent Small Form-factor Pluggable
SONET OC-12/OC-3 IR-1 / SDH STM S-4.1/S-1.1
Multirate Applications up to 622 Mbit/s
Single Mode 1310 nm Transceiver with LC™ Connector
V23848-H18-C56
V23848-H19-C56
Features

- Small Form-factor Pluggable (SFP) MSA compatible transceiver¹⁾
- Fully SFF-8472 compatible
- Incorporating Intelligent – Digital Diagnostic Monitoring Interface
- Internal calibration implementation
- Advanced release mechanism
- Easy access, even in belly to belly applications
- Wire handle release for simplicity
- Color coded blue tab (single mode)
- PCI height compatible
- Excellent EMI performance
- Separate and common chassis/signal ground module concepts available
- RJ-45 style LC™ connector system
- Single power supply (3.3 V)
- Low power consumption
- Small size for high channel density
- UL-94 V-0 certified
- ESD Class 1C per JESD22-A114-B (MIL-STD 883D Method 3015.7)
- According to FCC (Class B) and EN 55022
- For distances of up to 21 km (see **Supported Link Lengths**)
- Fabry Perot laser, PIN photo diode
- Laser safety according to Class 1 FDA and IEC
- AC/AC Coupling according to MSA
- Suitable for multirate applications up to 622 Mbit/s
- Fast Ethernet (FE) compatible
- Extended operating temperature range of –40°C to 85°C
- SFP evaluation kit V23848-S5-V4 available upon request
- A press fit cage and cage plugs are available as accessory products from Infineon (see **SFP Accessories**)



File: 1132



File: 1133

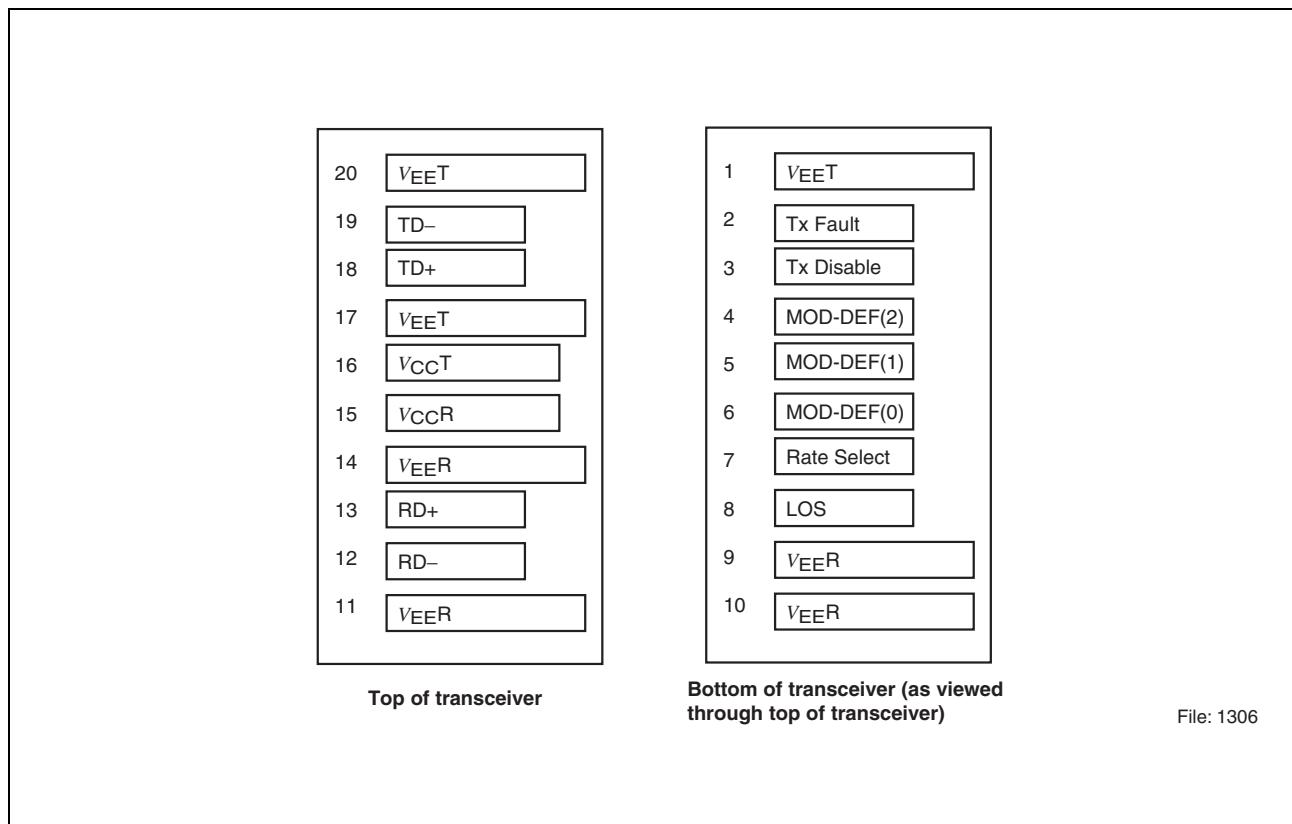
¹⁾ MSA documentation can be found at www.infineon.com/fiberoptics under Transceivers, SFP Transceivers.

For ordering information see next page.

iSFP™ is a trademark of Infineon Technologies. LC™ is a trademark of Lucent.

Ordering Information

Part Number	Chassis/Signal Grounding Concept
V23848-H18-C56	Common
V23848-H19-C56	Separated

Pin Configuration

Figure 1 iSFP™ Transceiver Electrical Pad Layout

Pin Description

Pin No.	Name	Logic Level	Function
1	$V_{EE}T$	N/A	Transmitter Ground ¹⁾
2	Tx Fault	LV TTL	Transmitter Fault Indication ^{2) 8)}
3	Tx Disable	LV TTL	Transmitter Disable ³⁾
4	MOD-DEF(2)	LV TTL	Module Definition 2 ^{4) 8)}
5	MOD-DEF(1)	LV TTL	Module Definition 1 ^{5) 8)}
6	MOD-DEF(0)	N/A	Module Definition 0 ^{6) 8)}
7	Rate Select	N/A	Not connected
8	LOS	LV TTL	Loss Of Signal ^{7) 8)}
9	$V_{EE}R$	N/A	Receiver Ground ¹⁾
10	$V_{EE}R$	N/A	Receiver Ground ¹⁾
11	$V_{EE}R$	N/A	Receiver Ground ¹⁾
12	RD-	LVPECL	Inv. Received Data Out ⁹⁾
13	RD+	LVPECL	Received Data Out ⁹⁾
14	$V_{EE}R$	N/A	Receiver Ground ¹⁾
15	$V_{CC}R$	N/A	Receiver Power
16	$V_{CC}T$	N/A	Transmitter Power
17	$V_{EE}T$	N/A	Transmitter Ground ¹⁾
18	TD+	LVPECL	Transmit Data In ¹⁰⁾
19	TD-	LVPECL	Inv. Transmit Data In ¹⁰⁾
20	$V_{EE}T$	N/A	Transmitter Ground ¹⁾

¹⁾ Common transmitter and receiver ground within the module.

²⁾ A high signal indicates a laser fault of some kind and that laser is switched off.

³⁾ A low signal switches the transmitter on. A high signal or when not connected switches the transmitter off.

⁴⁾ MOD-DEF(2) is the data line of two wire serial interface for serial ID.

⁵⁾ MOD-DEF(1) is the clock line of two wire serial interface for serial ID.

⁶⁾ MOD-DEF(0) is grounded by the module to indicate that the module is present.

⁷⁾ A low signal indicates normal operation, light is present at receiver input. A high signal indicates the received optical power is below the worst case receiver sensitivity.

⁸⁾ Should be pulled up on host board to V_{CC} by 4.7 - 10 k Ω .

⁹⁾ AC coupled inside the transceiver. Must be terminated with 100 Ω differential at the user SERDES.

¹⁰⁾ AC coupled and 100 Ω differential termination inside the transceiver.

Description

Description

The Infineon OC-12 transceiver – part of Infineon iSFP™ family – is compatible to the Physical Medium Depend (PMD) sublayer and baseband medium compatible to SONET OC-12/OC-3 IR-1 (Telcordia GR-253-CORE) and SDH STM-4 S-4.1/S-1.1 (ITU-T G.957).

The appropriate fiber optic cable is 9 μm single mode fiber with LC™ connector.

Supported Link Lengths

Category within Standard	Reach		Unit
	min.	max. ¹⁾	
SDH STM-4 S-4.1	0	15,000	meters
SONET OC-12 IR-1	0	21,000	

¹⁾ Maximum reach over fiber type SM-G.652 as defined by ITU-T G.957 and Telcordia GR-253-CORE standards. Longer reach possible depending upon link implementation.

The Infineon iSFP™ single mode transceiver is a single unit comprised of a transmitter, a receiver, and an LC™ receptacle.

This transceiver supports the LC™ connectorization concept. It is compatible with RJ-45 style backpanels for high end datacom and telecom applications while providing the advantages of fiber optic technology.

The Infineon single mode OC-12 transceiver is a single unit comprised of a transmitter, a receiver, and an LC receptacle. This design frees the customer from many alignment and PC board layout concerns. The module is designed for low cost LAN and applications with datarates from 125 to 622 Mbit/s. It can be used as the network end device interface in workstations, servers, and storage devices, and in a broad range of network devices such as bridges, routers, and intelligent hubs, as well as local and wide area ATM switches.

This transceiver operates at up to OC-12 datarates from a single power supply (+3.3 V). The 100 Ω differential data inputs and outputs are LVPECL and CML compatible.

Functional Description of iSFP™ Transceiver

This transceiver is designed to transmit serial data via single mode cable.

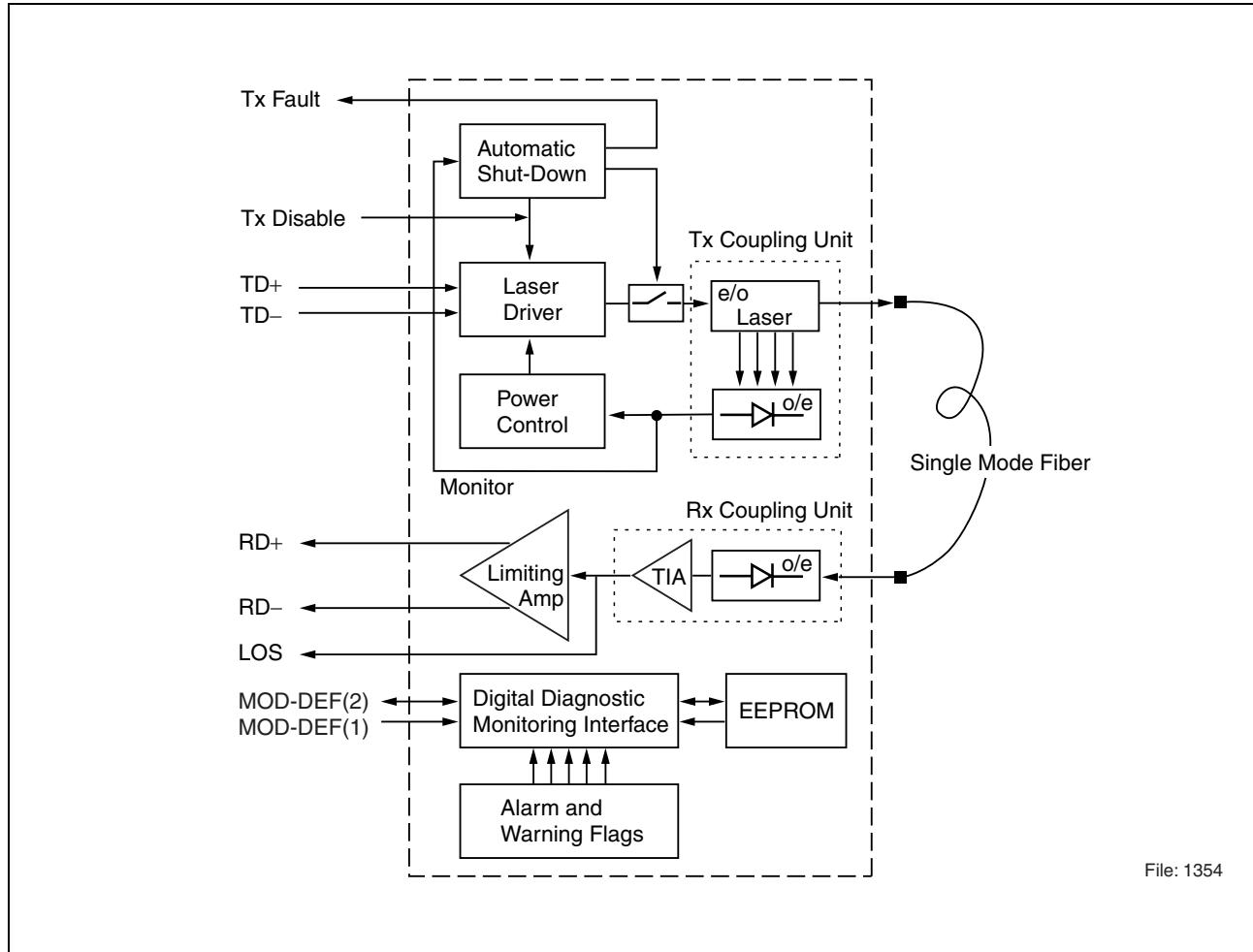


Figure 2 Functional Diagram

The receiver component converts the optical serial data into CML compatible electrical data (RD+ and RD-). The Loss Of Signal (LOS) shows whether an optical signal is present.

The transmitter converts CML compatible electrical serial data (TD+ and TD-) into optical serial data. Data lines are differentially $100\ \Omega$ terminated.

The transmitter contains a laser driver circuit that drives the modulation and bias current of the laser diode. The currents are controlled by a power control circuit to guarantee constant output power of the laser over temperature and aging. The power control uses the output of the monitor PIN diode (mechanically built into the laser coupling unit) as a controlling signal, to prevent the laser power from exceeding the operating limits.

Single fault condition is ensured by means of an integrated automatic shutdown circuit that disables the laser when it detects laser fault to guarantee the laser Eye Safety.

Description

The transceiver contains a supervisory circuit to control the power supply. This circuit makes an internal reset signal whenever the supply voltage drops below the reset threshold. It keeps the reset signal active for at least 140 milliseconds after the voltage has risen above the reset threshold. During this time the laser is inactive.

A low signal on TxDis enables transmitter. If TxDis is high or not connected the transmitter is disabled.

An enhanced Digital Diagnostic Monitoring Interface (Intelligent) has been incorporated into the Infineon Small Form-factor Pluggable (SFP) transceiver. This allows real time access to transceiver operating parameters, based on the SFF-8472.

This transceiver features Internal Calibration. Measurements are calibrated over operating temperature and voltage and must be interpreted as defined in SFF-8472.

The transceiver generates this diagnostic data by digitization of internal analog signals monitored by a new diagnostic Integrated Circuit (IC).

This diagnostic IC has inbuilt sensors to include alarm and warning thresholds. These threshold values are set during device manufacture and therefore allow the user to determine when a particular value is outside of its operating range.

Alarm and Warning Flags are given. Alarm Flags indicate conditions likely to be associated with an inoperational link and cause for immediate action. Warning Flags indicate conditions outside the normally guaranteed bounds but not necessarily causes of immediate link failures.

These enhanced features are in addition to the existing SFP features provided by the manufacturer i.e. serial number and other vendor specific data.

The serial ID interface defines a 256 byte memory map in EEPROM, accessible over a 2 wire, serial interface at the 8 bit address 1010000X (A0h).

The Digital Diagnostic Monitoring Interface makes use of the 8 bit address 1010001X (A2h), so the originally defined serial ID memory map remains unchanged and is therefore backward compatible.

Digital Diagnostic Monitoring Parameters

Parameter	Accuracy SFF-8472	Accuracy Actual
Tx Optical Power	±3 dB	±2 dB
Rx Optical Power	±3 dB	±3 dB
Bias Current	±10%	±10%
Power Supply Voltage	±3%	±3%
Transceiver Temperature	±3°C	±3°C

Regulatory Compliance (EMI)

Feature	Standard	Comments
ESD: Electrostatic Discharge to the Electrical Pins	EIA/JESD22-A114-B (MIL-STD 883D method 3015.7)	Class 1C
Immunity: Against Electrostatic Discharge (ESD) to the Duplex LC Receptacle	EN 61000-4-2 IEC 61000-4-2	Discharges ranging from ± 2 kV to ± 15 kV on the receptacle cause no damage to transceiver (under recommended conditions).
Immunity: Against Radio Frequency Electromagnetic Field	EN 61000-4-3 IEC 61000-4-3	With a field strength of 10 V/m, noise frequency ranges from 10 MHz to 2 GHz. No effect on transceiver performance between the specification limits.
Emission: Radiated Field Strength	FCC 47 CFR Part 15, Class B CISPR 22 EN 55022 Class B	Noise frequency range: 30 MHz to 18 GHz
 1) File: 1408		This device complies with part 15 of the FCC Rules ²⁾ . Operation is subject to the following two conditions: 1) This device may not cause harmful interference. 2) This device must accept any interference received, including interference that may cause undesired operation.

¹⁾ Only for V23848-H18-C56.

²⁾ Any kind of modification not expressly approved by Infineon Technologies may affect the regulatory compliance of the concerned product. As a consequence thereof this could void the user's authority to operate the equipment.

Technical Data
Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Data Input Voltage	$V_{ID\ max}$		$V_{CC}+0.5$	V
Differential Data Input Voltage Swing	$V_{ID\ pk-pk}$		5	V
Storage Ambient Temperature	T_S	-40	85	°C
Operating Case Temperature ¹⁾	T_C	-40	85	°C
Storage Relative Humidity	RH_s	5	95	%
Operating Relative Humidity	RH_o	5	85	%
Supply Voltage	$V_{CC\ max}$		4	V
Data Output Current	I_{data}		50	mA
Receiver Optical Input Power	$Rx_P\ max$		3	dBm

¹⁾ Operating case temperature measured at transceiver reference point (in cage through 2nd centre hole from rear, see **Figure 9**).

Exceeding any one of these values may permanently destroy the device.

Electrical Characteristics ($V_{CC} = 2.97$ V to 3.63 V, $T_C = -40^\circ\text{C}$ to 85°C)

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

Common

Supply Voltage	$V_{CC} - V_{EE}$	2.97	3.3	3.63	V
In-rush Current ¹⁾	$I_{IR\ max}$			30	mA
Power Dissipation	P			1	W

Transmitter

Differential Data Input Voltage Swing ²⁾	$V_{ID\ pk-pk}$	500		3200	mV
Tx Disable Voltage	Tx_{Dis}	2		V_{CC}	V
Tx Enable Voltage	Tx_{En}	V_{EE}		0.8	V
Tx Fault High Voltage	Tx_{FH}	2.4		V_{CC}	V
Tx Fault Low Voltage	Tx_{FL}	V_{EE}		0.5	V
Supply Current ³⁾	I_{Tx}			150	mA

Receiver

Differential Data Output Voltage Swing ⁴⁾	$V_{OD\ pk-pk}$	500		1000	mV
LOS Active	LOS_A	2.4		V_{CC}	V
LOS Normal	LOS_N	V_{EE}		0.5	V
Rise Time ⁵⁾	t_{R-Rx}		120		ps
Fall Time ⁵⁾	t_{F-Rx}		120		ps
Power Supply Noise Rejection ⁶⁾	PSNR		100		mV_{pp}
Supply Current ^{3) 7)}	I_{Rx}			130	mA

¹⁾ Measured with MSA recommended supply filter network (**Figure 7**). Maximum value above that of the steady state value.

²⁾ Internally AC coupled. Typical 100 Ω differential input impedance.

³⁾ MSA defines maximum current at 300 mA.

⁴⁾ Internally AC coupled. Load 50 Ω to GND or 100 Ω differential. For dynamic measurement a tolerance of 50 mV should be added.

⁵⁾ Measured values are 20% - 80%.

⁶⁾ Measured using a 20 Hz to 1 MHz sinusoidal modulation with the MSA recommended power supply filter network (**Figure 7**) in place. A change in sensitivity of less than 1 dB can be typically expected.

⁷⁾ Supply current excluding Rx output load.

Optical Characteristics ($V_{CC} = 2.97$ V to 3.63 V, $T_C = -40^\circ\text{C}$ to 85°C)

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Transmitter					
Launched Power (Average) ¹⁾	P_O	-15		-8	dBm
Extinction Ratio (Dynamic)	ER	8.2			dB
Center Wavelength	λ_C	1274		1356	nm
Spectral Width (rms)	σ_I			2.5	nm
Tx Disable Laser Output Power	$P_{O-TxDis}$			-50	dBm
Optical Eye Mask ²⁾	According to standards				
Jitter Generation (pk-pk) ³⁾	$J_{pk-pk\ Tx}$		0.055	0.065	UI
Jitter Generation (rms) ³⁾	$J_{rms\ Tx}$		0.003	0.0045	UI
Rise Time ⁴⁾	t_{R-Tx}		40		ps
Fall Time ⁴⁾	t_{F-Tx}		150		ps
Receiver⁵⁾					
Saturation (Average Power) ⁶⁾	P_{SAT}	-8			dBm
Sensitivity (Average Power) ⁷⁾ @ 622 Mbit/s @ 155 Mbit/s @ 125 Mbit/s	P_{IN}		-30.5 -31.5 -31.5	-28 -28 -28	dBm
LOS Assert Level ⁸⁾	P_{LOSA}	-37			dBm
LOS Deassert Level ⁸⁾	P_{LOSD}			-28	dBm
LOS Hysteresis ⁸⁾	$P_{LOSA} - P_{LOSD}$	0.5	3		dB
Input Center Wavelength	λ_C	1260		1580	nm
Path Penalty	R_{PEN}			1	dB

¹⁾ Into single mode fiber, 9 μm diameter.

²⁾ Transmitter eye is according to ITU-T G.957 S-4.1 and SONET OC-12 IR-1. Measured with 20% eye mask margin.

³⁾ The transceiver is specified to meet the SONET/SDH Jitter performance as outlined in ITU-T G.958 and Telcordia GR-253. Jitter Generation is defined as the amount of jitter that is generated by the transceiver. The Jitter Generation specifications are referenced to the optical OC-12 signals. If no or minimum jitter is applied to the electrical inputs of the transmitter, then Jitter Generation can simply be defined as the amount of jitter on the Tx optical output. The SONET specifications for Jitter Generation are 0.01 UI rms, maximum and 0.1 UI pk-pk, maximum. For SDH, 10 mUI rms, maximum. Both are measured with a 12 kHz - 5 MHz filter in line. A UI is a Unit Interval, which is equivalent to one bit slot.

⁴⁾ Values are 20% - 80%, filtered and measured at nominal data rate.

⁵⁾ Receiver characteristics are measured with a worst case reference laser.

⁶⁾ At 9 dB Extinction Ratio of the incoming signal.

Technical Data

⁷⁾ Minimum average optical power at which the BER is less than 1×10^{-10} . Measured with a 2²³-1 NRZ PRBS as recommended by ANSI T1E1.2, SONET, and ITU-T G.957.

⁸⁾ See **Figure 3**.

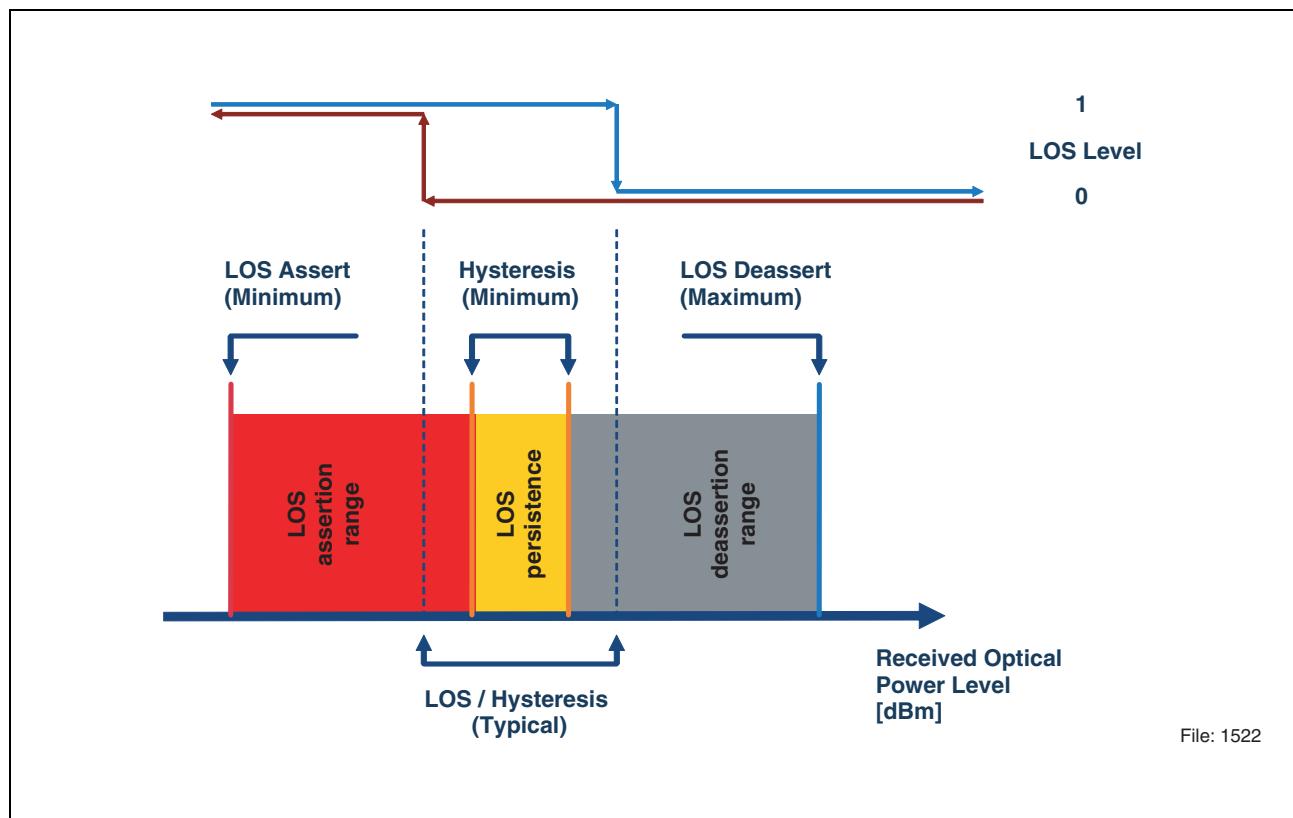


Figure 3

Timing of Control and Status I/O

Parameter	Symbol	Values		Unit	Condition
		min.	max.		
Tx Disable Assert Time	t_off		10	μs	Time from rising edge of Tx Disable to when the optical output falls below 10% of nominal
Tx Disable Negate Time	t_on		1	ms	Time from falling edge of Tx Disable to when the modulated optical output rises above 90% of nominal
Time to Initialize, Including Reset of Tx Fault	t_init		300	ms	From power on or negation of Tx Fault using Tx Disable
Tx Fault Assert Time	t_fault		100	μs	Time from fault to Tx Fault on
Tx Disable to Reset	t_reset	10		μs	Time Tx Disable must be held high to reset Tx Fault
LOS Assert Time	t_loss_on		100	μs	Time from LOS state to Rx LOS assert
LOS Deassert Time	t_loss_off		100	μs	Time from non-LOS state to Rx LOS deassert

I/O Timing of Soft Control and Status Functions

Parameter	Symbol	Max. Value	Unit	Condition
Tx Disable assert time	t_off	100	ms	Time from Tx Disable bit set ¹⁾ until optical output falls below 10% of nominal
Tx Disable deassert time	t_on	100	ms	Time from Tx Disable bit cleared until optical output rises above 90% of nominal
Time to initialize, including reset of Tx Fault	t_init	300	ms	Time from power on or negation of Tx Fault using Tx Disable until transmitter output is stable ²⁾
Tx Fault assert time	t_fault	100	ms	Time from fault to Tx Fault bit set
LOS assert time	t_loss_on	100	ms	Time from LOS state to Rx LOS bit set
LOS deassert time	t_loss_off	100	ms	Time from non-LOS state to Rx LOS bit cleared
Rate select change time ³⁾	t_rate_sel	100	ms	Time from change of state of Rate Select bit ¹⁾ until receiver bandwidth is in conformance with appropriate specification
Serial ID clock rate ⁴⁾	f_serial_clock	400	kHz	N/A
Analog parameter data ready	t_data	1000	ms	From power on to data ready, bit 0 of byte 110 set
Serial bus hardware ready	t_serial	300	ms	Time from power on until module is ready for data transmission

¹⁾ Measured from falling clock edge after stop bit of write transaction.

²⁾ See Gigabit Interface Converter (GBIC). SFF-0053, Rev. 5.5, September 27, 2000.

³⁾ Not implemented.

⁴⁾ The maximum clock rate of the serial interface is defined by the I²C bus interface standard.

Eye Safety

This laser based single mode transceiver is a Class 1 product. It complies with IEC 60825-1/A2: 2001 and FDA performance standards for laser products (21 CFR 1040.10 and 1040.11) except for deviations pursuant to Laser Notice 50, dated July 26, 2001.

CLASS 1 LASER PRODUCT

To meet laser safety requirements the transceiver shall be operated within the Absolute Maximum Ratings.

*Note: All adjustments have been made at the factory prior to shipment of the devices.
No maintenance or alteration to the device is required.*

Tampering with or modifying the performance of the device will result in voided product warranty.

Failure to adhere to the above restrictions could result in a modification that is considered an act of "manufacturing", and will require, under law, recertification of the modified product with the U.S. Food and Drug Administration (ref. 21 CFR 1040.10 (i)).

Laser Emission Data

Wavelength	1310 nm
Maximum total output power (as defined by IEC: 7 mm aperture at 14 mm distance)	15.6 mW / 11.9 dBm
Beam divergence (full angle) / NA (half angle)	11° / 0.1 rad

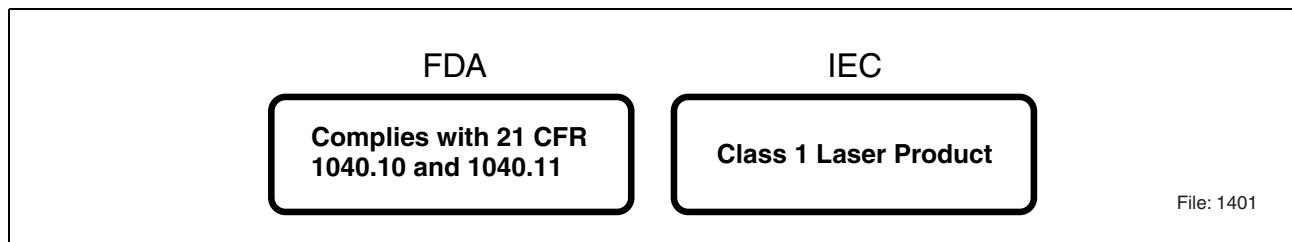


Figure 4 Required Labels

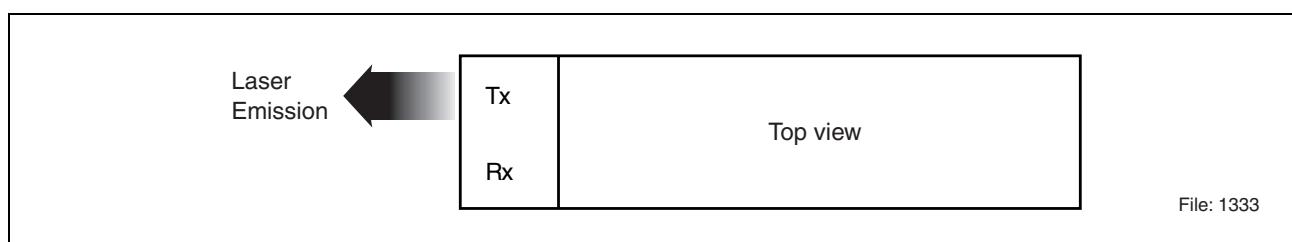


Figure 5 Laser Emission

Application Notes

EMI Recommendations

To avoid electromagnetic radiation exceeding the required limits set by the standards, please take note of the following recommendations.

When Gigabit switching components are found on a PCB (e.g. multiplexer, serializer-deserializer, clock data recovery, etc.), any opening of the chassis may leak radiation; this may also occur at chassis slots other than that of the device itself. Thus every mechanical opening or aperture should be as small as feasible and its length carefully considered.

On the board itself, every data connection should be an impedance matched line (e.g. strip line or coplanar strip line). Data (D) and Data-not (Dn) should be routed symmetrically. Vias should be avoided. Where internal termination inside an IC or a transceiver is not present, a line terminating resistor must be provided. The decision of how best to establish a ground depends on many boundary conditions. This decision may turn out to be critical for achieving lowest EMI performance. At RF frequencies the ground plane will always carry some amount of RF noise. Thus the ground and V_{CC} planes are often major radiators inside an enclosure. As a general rule, for small systems such as PCI cards placed inside poorly shielded enclosures, the common ground scheme has often proven to be most effective in reducing RF emissions. In a common ground scheme, the PCI card becomes more equipotential with the chassis ground. As a result, the overall radiation will decrease. In a common ground scheme, it is strongly recommended to provide a proper contact between signal ground and chassis ground at every location where possible. This concept is designed to avoid hotspots which are places of highest radiation, caused when only a few connections between chassis and signal grounds exist. Compensation currents would concentrate at these connections, causing radiation. However, as signal ground may be the main cause for parasitic radiation, connecting chassis ground and signal ground at the wrong place may result in enhanced RF emissions.

For example, connecting chassis ground and signal ground at a front panel/bezel/chassis by means of a fiber optic transceiver/cage may result in a large amount of radiation especially where combined with an inadequate number of grounding points between signal ground and chassis ground. Thus the transceiver becomes a single contact point increasing radiation emissions. Even a capacitive coupling between signal ground and chassis ground may be harmful if it is too close to an opening or an aperture. For a number of systems, enforcing a strict separation of signal ground from chassis ground may be advantageous, providing the housing does not present any slots or other discontinuities. This separate ground concept seems to be more suitable in large systems where appropriate shielding measures have also been implemented.

Application Notes

In many situations the question on which ground concept to implement in the design cannot be easily decided prior to the receipt of first EMI measurement results. Infineon thus offers both module versions; V23848-Xx8-Xxx for common ground and V23848-Xx9-Xxx for separate ground concept.

The return path of RF current must also be considered. Thus a split ground plane between Tx and Rx paths may result in severe EMI problems irrespective of which module ground concept has been applied.

The bezel opening for a transceiver should be sized so that all contact springs of the transceiver cage make good electrical contact with the face plate. Please consider that the PCB may behave like a dielectric waveguide. With a dielectric constant of 4, the wavelength of the harmonics inside the PCB will be half of that in free space. Thus even the smallest PCBs may have unexpected resonances.

Large systems can have many openings in the front panel for SFP transceivers. In typical applications, not all of these ports will hold transceivers; some may be intentionally left empty. These empty slots may emit significant amounts of radiation. Thus it is recommended that empty ports be plugged with an EMI plug as shown in **Figure 6**. Infineon offers an EMI/dust plug, P/N V23818-S5-B1.

SFP Accessories

Cage:

Infineon Technologies
Part Number: V23838-S5-N1/V23838-S5-N1-BB

Host Board Connector:

Tyco Electronics
Part Number: 1367073-1

Cage EMI/Dust Plug:

Infineon Technologies
Part Number: V23818-S5-B1

Cage Dust Plug:

Infineon Technologies
Part Number: V23818-S5-B2

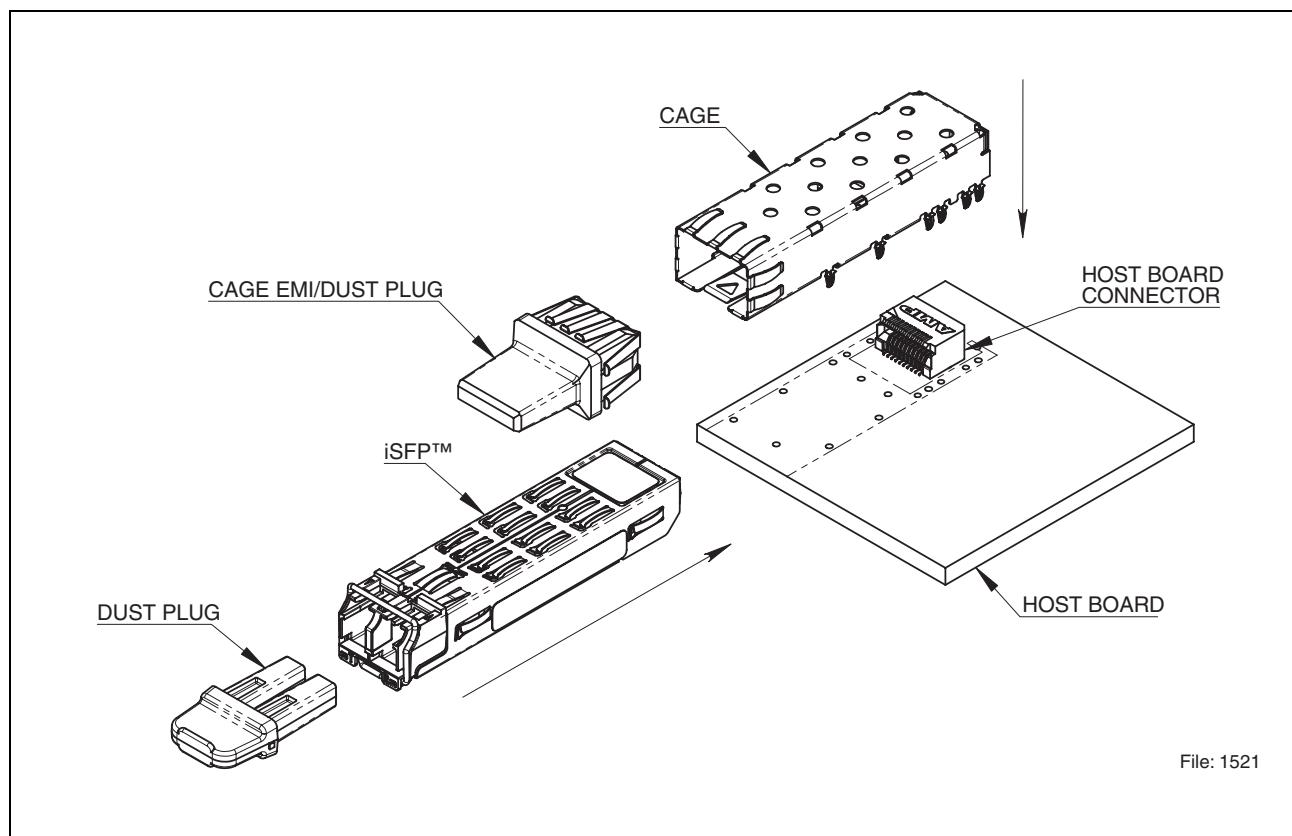


Figure 6

EEPROM Serial ID Memory Contents (A0h), V23848-H18-C56

Addr.	Hex	ASCII	Name/Description
0	03		Identifier
1	04		Extended identifier
2	07		Connector
3	00		Transceiver optical compatibility
4	10		
5	22		
6	00		
7	00		
8	00		
9	00		
10	00		
11	05		Encoding
12	06		BR, nominal
13	00		Reserved
14	0F		Length (9 µm) - km
15	96		Length (9 µm)
16	00		Length (50 µm)
17	00		Length (62.5 µm)
18	00		Length (copper)
19	00		Reserved
20	49	I	Vendor name
21	6E	n	
22	66	f	
23	69	i	
24	6E	n	
25	65	e	
26	6F	o	
27	6E	n	
28	20		
29	46	F	
30	4F	O	
31	20		

Addr.	Hex	ASCII	Name/Description
32	47	G	Vendor name
33	6D	m	
34	62	b	
35	48	H	
36	00		
37	00		
38	03		
39	19		
40	56	V	
41	32	2	
42	33	3	
43	38	8	
44	34	4	
45	38	8	
46	2D	-	
47	48	H	
48	31	1	
49	38	8	
50	2D	-	
51	43	C	
52	35	5	
53	36	6	
54	20		
55	20		
56	46	F	Vendor revision, product status dependent
57	33	3	
58	41	A	
59	39	9	
60	05		Wavelength
61	1E		
62	00		
63	E3		Check sum of bytes 0 - 62

EEPROM Serial ID Memory Contents (A0h), V23848-H18-C56 (cont'd)

Addr.	Hex	ASCII	Name/Description	Addr.	Hex	ASCII	Name/Description
64	00		Transceiver signal options	96	20		Vendor specific EEPROM
65	1A			97	20		
66	00		BR, maximum	98	20		
67	50		BR, minimum	99	20		
68			Vendor serial number	100	20		
69				101	20		
70				102	20		
71				103	20		
72				104	20		
73				105	20		
74				106	20		
75				107	20		
76	20			108	20		
77	20			109	20		
78	20			110	20		
79	20			111	20		
80	20			112	20		
81	20			113	20		
82	20			114	20		
83	20			115	20		
84			Vendor manufacturing date code	116	20		
85				117	20		
86				118	20		
87				119	20		
88				120	20		
89				121	20		
90	20			122	20		
91	20			123	20		
92	68		Diagnostic monitoring type	124	20		
93	B0			125	20		
94	01			126	20		
95			Low order 8 bits of the sum of the contents of all the bytes from byte 64 to byte 94, inclusive	127	20		Vendor specific. Reserved for future use
				128 - 255	00		

EEPROM Serial ID Memory Contents (A0h), V23848-H19-C56

Addr.	Hex	ASCII	Name/Description
0	03		Identifier
1	04		Extended identifier
2	07		Connector
3	00		Transceiver optical compatibility
4	10		
5	22		
6	00		
7	00		
8	00		
9	00		
10	00		
11	05		Encoding
12	06		BR, nominal
13	00		Reserved
14	0F		Length (9 µm) - km
15	96		Length (9 µm)
16	00		Length (50 µm)
17	00		Length (62.5 µm)
18	00		Length (copper)
19	00		Reserved
20	49	I	Vendor name
21	6E	n	
22	66	f	
23	69	i	
24	6E	n	
25	65	e	
26	6F	o	
27	6E	n	
28	20		
29	46	F	
30	4F	O	
31	20		

Addr.	Hex	ASCII	Name/Description
32	47	G	Vendor name
33	6D	m	
34	62	b	
35	48	H	
36	00		
37	00		
38	03		
39	19		
40	56	V	
41	32	2	
42	33	3	
43	38	8	
44	34	4	
45	38	8	
46	2D	-	
47	48	H	
48	31	1	
49	39	9	
50	2D	-	
51	43	C	
52	35	5	
53	36	6	
54	20		
55	20		
56	46	F	Vendor revision, product status dependent
57	33	3	
58	41	A	
59	39	9	
60	05		Wavelength
61	1E		
62	00		
63	E4		Check sum of bytes 0 - 62

Application Notes
EEPROM Serial ID Memory Contents (A0h), V23848-H19-C56 (cont'd)

Addr.	Hex	ASCII	Name/Description	Addr.	Hex	ASCII	Name/Description
64	00		Transceiver signal options	96	20		Vendor specific EEPROM
65	1A			97	20		
66	00		BR, maximum	98	20		
67	50		BR, minimum	99	20		
68			Vendor serial number	100	20		
69				101	20		
70				102	20		
71				103	20		
72				104	20		
73				105	20		
74				106	20		
75				107	20		
76	20			108	20		
77	20			109	20		
78	20			110	20		
79	20			111	20		
80	20			112	20		
81	20			113	20		
82	20			114	20		
83	20			115	20		
84			Vendor manufacturing date code	116	20		
85				117	20		
86				118	20		
87				119	20		
88				120	20		
89				121	20		
90	20			122	20		
91	20			123	20		
92	68		Diagnostic monitoring type	124	20		
93	B0			125	20		
94	01			126	20		
95			Low order 8 bits of the sum of the contents of all the bytes from byte 64 to byte 94, inclusive	127	20		Vendor specific. Reserved for future use
128 - 255	00			128 - 255	00		

Digital Diagnostic Monitoring Interface – Intelligent

Alarm and Warning Thresholds (2-Wire Address A2h)

Address	# Bytes	Name	Description	Value
00 - 01	2	Temp High Alarm	MSB at low address	95°C ¹⁾
02 - 03	2	Temp Low Alarm	MSB at low address	-40°C ¹⁾
04 - 05	2	Temp High Warning	MSB at low address	90°C ¹⁾
06 - 07	2	Temp Low Warning	MSB at low address	-35°C ¹⁾
08 - 09	2	Voltage High Alarm	MSB at low address	3.7 V ²⁾
10 - 11	2	Voltage Low Alarm	MSB at low address	2.85 V ²⁾
12 - 13	2	Voltage High Warning	MSB at low address	3.63 V ²⁾
14 - 15	2	Voltage Low Warning	MSB at low address	2.97 V ²⁾
16 - 17	2	Bias High Alarm	MSB at low address	70 mA
18 - 19	2	Bias Low Alarm	MSB at low address	4 mA
20 - 21	2	Bias High Warning	MSB at low address	60 mA
22 - 23	2	Bias Low Warning	MSB at low address	5 mA
24 - 25	2	Tx Power High Alarm	MSB at low address	-7 dBm
26 - 27	2	Tx Power Low Alarm	MSB at low address	-16 dBm
28 - 29	2	Tx Power High Warning	MSB at low address	-8 dBm
30 - 31	2	Tx Power Low Warning	MSB at low address	-15 dBm
32 - 33	2	Rx Power High Alarm	MSB at low address	-7 dBm
34 - 35	2	Rx Power Low Alarm	MSB at low address	-31 dBm
36 - 37	2	Rx Power High Warning	MSB at low address	-8 dBm
38 - 39	2	Rx Power Low Warning	MSB at low address	-28 dBm
40 - 55	16	Reserved	Reserved for future monitored quantities	

¹⁾ A delta exists between actual transceiver temperature and value shown as measurement is taken internal to an IC located on the underside of the iSFP™ PCB.

²⁾ Transceiver voltage measured after input filter with typical 0.1 V voltage drop.

Calibration Constants for External Calibration Option (2-Wire Address A2h)

Address	# Bytes	Name	Description	Value
56 - 59	4	Rx_PWR (4)	Single precision floating point calibration data, Rx optical power.	0
60 - 63	4	Rx_PWR (3)		0
64 - 67	4	Rx_PWR (2)		0
68 - 71	4	Rx_PWR (1)		1
72 - 75	4	Rx_PWR (0)		0
76 - 77	2	Tx_I (Slope)	Fixed decimal (unsigned) calibration data, laser bias current.	1
78 - 79	2	Tx_I (Offset)	Fixed decimal (signed two's complement) calibration data, laser bias current.	0
80 - 81	2	Tx_PWR (Slope)	Fixed decimal (unsigned) calibration data, transmitter coupled output power.	1
82 - 83	2	Tx_PWR (Offset)	Fixed decimal (signed two's complement) calibration data, transmitter coupled output power.	0
84 - 85	2	T (Slope)	Fixed decimal (unsigned) calibration data, internal module temperature.	1
86 - 87	2	T (Offset)	Fixed decimal (signed two's complement) calibration data, internal module temperature.	0
88 - 89	2	V (Slope)	Fixed decimal (unsigned) calibration data, internal module supply voltage.	1
90 - 91	2	V (Offset)	Fixed decimal (signed two's complement) calibration data, internal module supply voltage.	0
92 - 94	3	Reserved	Reserved	
95	1	Check sum	Byte 95 contains the low order 8 bits of the sum of bytes 0 - 94.	

A/D Values and Status Bits (2-Wire Address A2h)

Byte	Bit	Name	Description
Converted Analog Values. Calibrated 16 Bit Data.			
96	All	Temperature MSB	Internally measured module temperature ¹⁾
97	All	Temperature LSB	
98	All	V_{CC} MSB	Internally measured supply voltage in transceiver
99	All	V_{CC} LSB	
100	All	Tx Bias MSB	Internally measured Tx Bias Current
101	All	Tx Bias LSB	
102	All	Tx Power MSB	Measured Tx output power
103	All	Tx Power LSB	
104	All	Rx Power MSB	Measured Rx input power
105	All	Rx Power LSB	
106	All	Reserved MSB	Reserved for 1st future definition of digitized analog input
107	All	Reserved LSB	Reserved for 1st future definition of digitized analog input
108	All	Reserved MSB	Reserved for 2nd future definition of digitized analog input
109	All	Reserved LSB	Reserved for 2nd future definition of digitized analog input

Optional Status/Control Bits

110	7	Tx Disable State ²⁾	Digital state of the Tx Disable Input Pin
110	6	Soft Tx Disable ²⁾	Read/write bit that allows software disable of laser. Writing 1 disables laser
110	5	Reserved	
110	4	Rx Rate Select State ²⁾	Digital state of the SFP Rx Rate Select Input Pin
110	3	Soft Rx Rate Select ²⁾	Read/write bit that allows software Rx rate select. Writing 1 selects full bandwidth operation. Not implemented.

A/D Values and Status Bits (2-Wire Address A2h) (cont'd)

Byte	Bit	Name	Description
110	2	Tx Fault	Digital state of the Tx Fault Output Pin
110	1	LOS	Digital state of the LOS Output Pin
110	0	Data_Ready_Bar	Indicates transceiver has achieved power up and data is ready
111	7 - 0	Reserved	Reserved

¹⁾ Temperature measurement is performed on an IC located on the underside of the iSFP™ PCB.

²⁾ Not implemented.

Alarm and Warning Flags (2-Wire Address A2h)

Byte	Bit	Name	Description
112	7	Temp High Alarm	Set when internal temperature exceeds high alarm level
112	6	Temp Low Alarm	Set when internal temperature is below low alarm level
112	5	V_{CC} High Alarm	Set when internal supply voltage exceeds high alarm level
112	4	V_{CC} Low Alarm	Set when internal supply voltage is below low alarm level
112	3	Tx Bias High Alarm	Set when Tx Bias current exceeds high alarm level
112	2	Tx Bias Low Alarm	Set when Tx Bias current is below low alarm level
112	1	Tx Power High Alarm	Set when Tx output power exceeds high alarm level
112	0	Tx Power Low Alarm	Set when Tx output power is below low alarm level
113	7	Rx Power High Alarm	Set when received power exceeds high alarm level
113	6	Rx Power Low Alarm	Set when received power is below low alarm level
113	5	Reserved Alarm	
113	4	Reserved Alarm	
113	3	Reserved Alarm	
113	2	Reserved Alarm	
113	1	Reserved Alarm	
113	0	Reserved Alarm	
114	All	Reserved	
115	All	Reserved	
116	7	Temp High Warning	Set when internal temperature exceeds high warning level
116	6	Temp Low Warning	Set when internal temperature is below low warning level
116	5	V_{CC} High Warning	Set when internal supply voltage exceeds high warning level

Alarm and Warning Flags (2-Wire Address A2h) (cont'd)

Byte	Bit	Name	Description
116	4	V_{CC} Low Warning	Set when internal supply voltage is below low warning level
116	3	Tx Bias High Warning	Set when Tx bias current exceeds high warning level
116	2	Tx Bias Low Warning	Set when Tx bias current is below low warning level
116	1	Tx Power High Warning	Set when Tx output power exceeds high warning level
116	0	Tx Power Low Warning	Set when Tx output power is below low warning level
117	7	Rx Power High Warning	Set when received power exceeds high warning level
117	6	Rx Power Low Warning	Set when received power is below low warning level
117	5	Reserved Warning	
117	4	Reserved Warning	
117	3	Reserved Warning	
117	2	Reserved Warning	
117	1	Reserved Warning	
117	0	Reserved Warning	
118	All	Reserved	
119	All	Reserved	

Vendor Specific Memory Addresses (2-Wire Address A2h)

Address	# Bytes	Name	Description
120 -127	8	Vendor Specific	Vendor specific

User EEPROM (2-Wire Address A2h)

Address	# Bytes	Name	Description
128 - 247	120	User EEPROM	User writable EEPROM
248 - 255	8	Vendor Specific	Vendor specific control functions

Single Mode 1310 nm iSFP™ Transceiver, AC/AC TTL

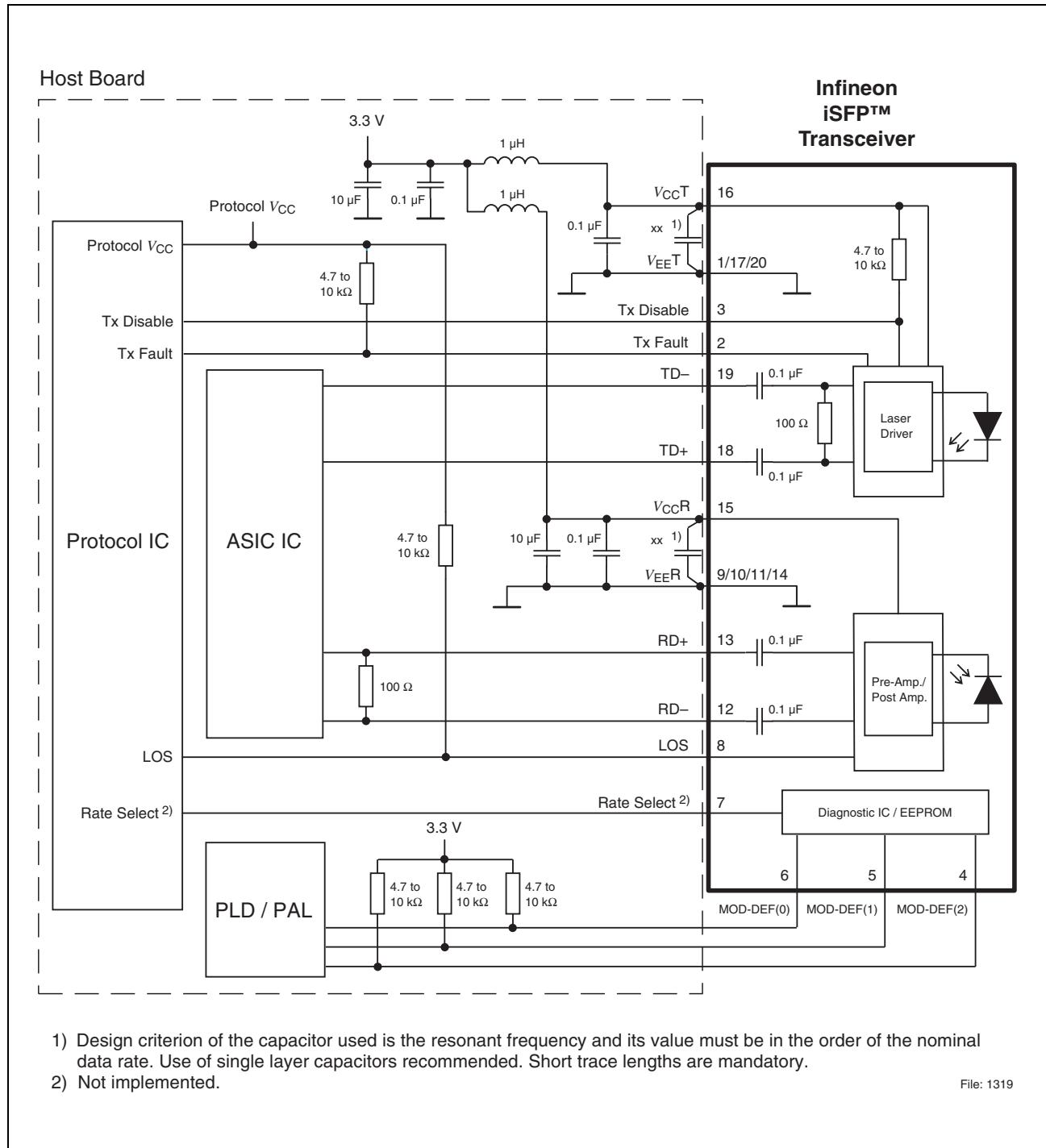
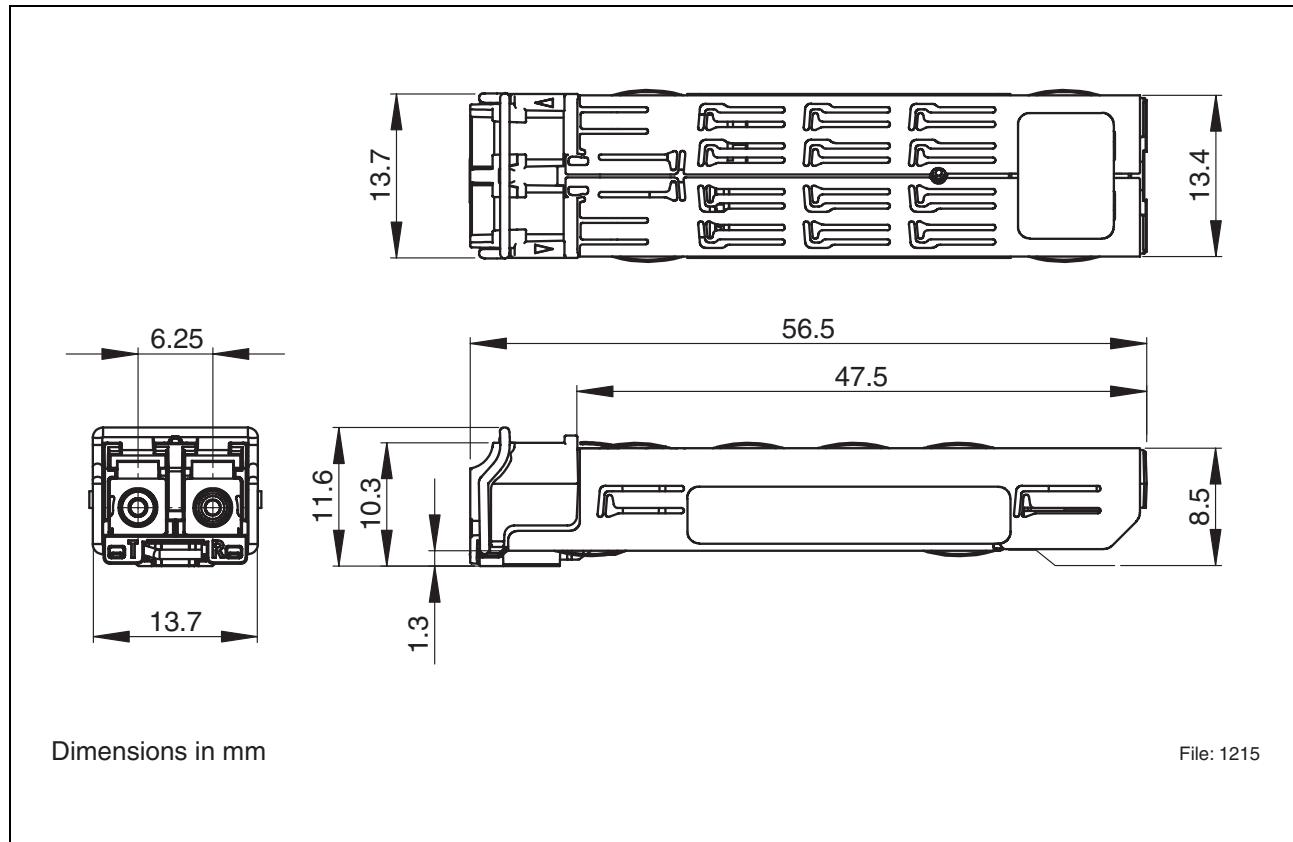
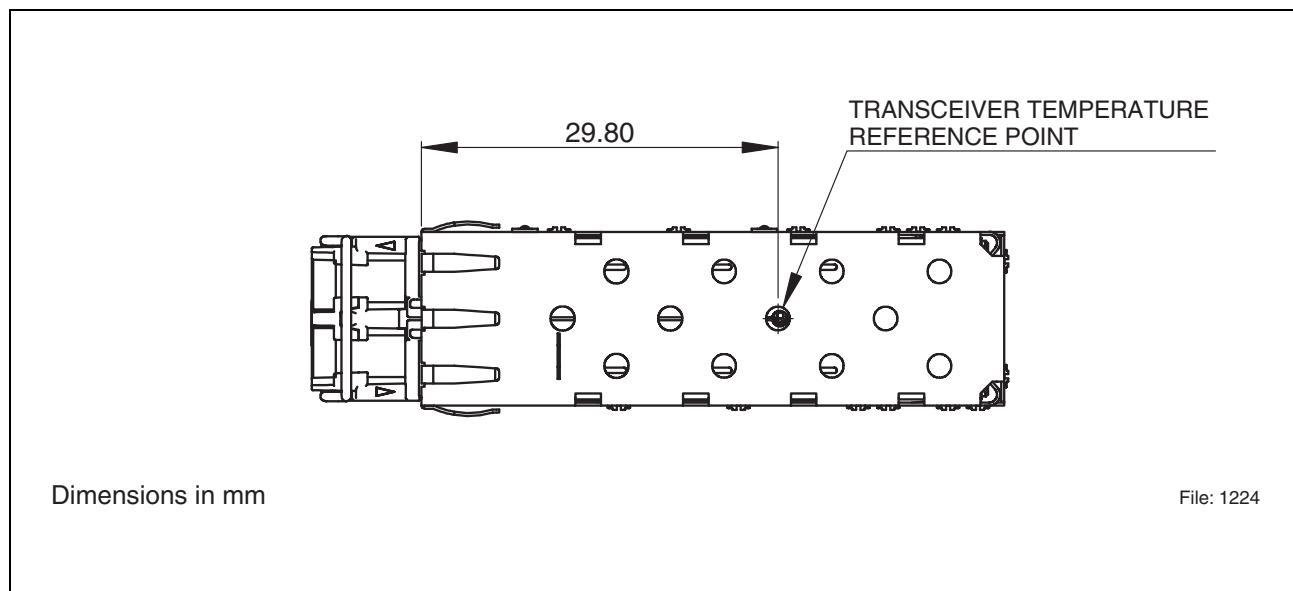


Figure 7 Example iSFP™ Host Board Schematic and Recommended Host Board Supply Filtering Network

Package Outlines

Figure 8

Figure 9

V23848-H18-C56

V23848-H19-C56

Revision History: **2004-06-25**

DS4

Previous Version: 2003-08-13

Page	Subjects (major changes since last revision)
	V23848-H19-C56 added
	“Preliminary Data Sheet” removed
	iSFP™ trademark added
1	Title changed
7, 9, 10, 18, 22, 24	Tables changed
11	Figure 3 added
15	EMI Recommendations changed
17	SFP Accessories changed
28	Figure 7 Host Board Schematic changed

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