



# DAC7631

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## Serial Input, 16-Bit, Voltage Output DIGITAL-TO-ANALOG CONVERTER

### FEATURES

- LOW POWER: 2.5mW
- UNIPOLAR OR BIPOLAR OPERATION
- SETTLING TIME: 10 $\mu$ s to 0.003%
- 15-BIT LINEARITY AND MONOTONICITY:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- USER SELECTABLE RESET TO MID-SCALE OR ZERO-SCALE
- SMALL SSOP-20 PACKAGE

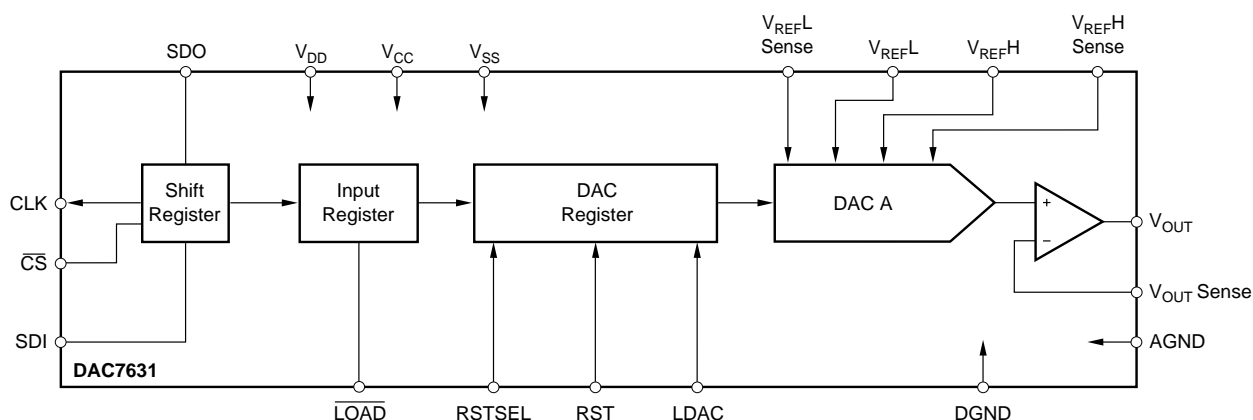
### APPLICATIONS

- ATE PIN ELECTRONICS
- PROCESS CONTROL
- CLOSED-LOOP SERVO-CONTROL
- MOTOR CONTROL
- DATA ACQUISITION SYSTEMS

### DESCRIPTION

The DAC7631 is a serial input, 16-bit, voltage output Digital-to-Analog Converter (D/A) with guaranteed 15-bit monotonic performance over the  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range. An asynchronous reset clears all registers to either mid-scale ( $8000_{\text{H}}$ ) or zero-scale ( $0000_{\text{H}}$ ), selectable via the RESETSEL pin. The device can be powered from a single +5V supply or from dual +5V and  $-5\text{V}$  supplies.

Low power and small size makes the DAC7631 ideal for process control, data acquisition systems, and closed-loop servo-control. The device is available in a SSOP-20 package, and is guaranteed over the  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range.



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# SPECIFICATIONS (Dual Supply)

At  $T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{DD} = V_{CC} = +5V$ ,  $V_{SS} = -5V$ ,  $V_{REFH} = +2.5V$ , and  $V_{REFL} = -2.5V$ , unless otherwise noted.

| PARAMETER   | CONDITIONS   | DAC7631E  |  |   | DAC7631EB                       |   |   | UNITS   |
|---|--|---|--|---|---------------------------------|---|---|---|
|   |  | MIN   | TYP  | MAX   | MIN                             | TYP   | MAX   |   |
| <b>ACCURACY</b><br>Linearity Error<br>Differential Linearity Error<br>Monotonicity, $T_{MIN}$ to $T_{MAX}$<br>Bipolar Zero Error<br>Bipolar Zero Error Drift<br>Full-Scale Error<br>Full-Scale Error Drift<br>Power Supply Rejection Ratio (PSRR) | At Full Scale  | 14  | $\pm 3$<br>$\pm 2$<br>$\pm 1$<br>5<br>$\pm 1$<br>5<br>10 | $\pm 4$<br>$\pm 3$<br>$\pm 2$<br>10<br>$\pm 2$<br>10<br>100 | 15                              | $\pm 2$<br>$\pm 1$<br>*<br>*<br>*<br>*<br>* | $\pm 3$<br>$\pm 2$<br>*<br>*<br>*<br>*<br>* | LSB<br>LSB<br>Bits<br>mV<br>ppm/°C<br>mV<br>ppm/°C<br>ppm/V |
| <b>ANALOG OUTPUT</b><br>Voltage Output<br>Output Current<br>Maximum Load Capacitance<br>Short-Circuit Current<br>Short-Circuit Duration   | $V_{REF} = -2.5V$ , $R_L = 10k\Omega$ , $V_{SS} = -5V$<br><br>No Oscillation<br><br>GND or $V_{CC}$ or $V_{SS}$                          | $V_{REFL} - 1.25$                                 | 500<br>-10, +30<br>Indefinite                            | $V_{REFH} + 1.25$   | *<br>*                          | *<br>*<br>*<br>*                            | *<br>*                                      | V<br>mA<br>pF<br>mA   |
| <b>REFERENCE INPUT</b><br>Ref High Input Voltage Range<br>Ref Low Input Voltage Range<br>Ref High Input Current<br>Ref Low Input Current  |  | $V_{REFL} + 1.25$<br>-2.5                         | 500<br>-500  | +2.5<br>$V_{REFH} - 1.25$                                   | *<br>*                          | *<br>*<br>*<br>*                            | *<br>*                                      | V<br>V<br>μA<br>μA  |
| <b>DYNAMIC PERFORMANCE</b><br>Settling Time<br>Digital Feedthrough<br>Output Noise Voltage<br>DAC Glitch  | To $\pm 0.003\%$ , 5V Output Step<br><br>$f = 10kHz$<br>7FFF <sub>H</sub> to 8000 <sub>H</sub> or 8000 <sub>H</sub> to 7FFF <sub>H</sub> |   | 8<br>2<br>60<br>40                                       | 10  |                                 | *<br>*<br>*<br>*                            | *<br>*                                      | μs<br>nV-s<br>nV/√Hz<br>nV-s                                |
| <b>DIGITAL INPUT</b><br>$V_{IH}$<br>$V_{IL}$<br>$I_{IH}$<br>$I_{IL}$  |  | $0.7 \cdot V_{DD}$                                |  | $0.3 \cdot V_{DD}$<br>$\pm 10$<br>$\pm 10$                  | *                               |   | *<br>*<br>*                                 | V<br>V<br>μA<br>μA  |
| <b>DIGITAL OUTPUT</b><br>$V_{OH}$<br>$V_{OL}$   | $I_{OH} = -0.8mA$<br>$I_{OL} = 1.6mA$  | 3.6   | 4.5<br>0.3   | 0.4   | *<br>*                          | *<br>*                                      | *<br>*                                      | V<br>V  |
| <b>POWER SUPPLY</b><br>$V_{DD}$<br>$V_{CC}$<br>$V_{SS}$<br>$I_{CC}$<br>$I_{DD}$<br>$I_{SS}$<br>Power  |  | +4.75<br>+4.75<br>-5.25<br>0.4<br>50<br>-0.6<br>4 | +5.0<br>+5.0<br>-5.0<br>0.4<br>50<br>-0.5<br>4           | +5.25<br>+5.25<br>-4.75<br>0.5                              | *<br>*<br>*<br>*<br>*<br>*<br>* | *<br>*<br>*<br>*<br>*<br>*<br>*             | *<br>*<br>*<br>*<br>*<br>*<br>*             | V<br>V<br>V<br>mA<br>μA<br>mA<br>mW                         |
| <b>TEMPERATURE RANGE</b><br>Specified Performance   |  | -40   |  | +85   | *                               |   | *   | °C  |

\* Specifications same as DAC7631E.

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# SPECIFICATIONS (Single Supply)

At  $T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{DD} = V_{CC} = +5V$ ,  $V_{SS} = 0V$ ,  $V_{REFH} = +2.5V$ , and  $V_{REFL} = 0V$ , unless otherwise noted.

| PARAMETER  | CONDITIONS  | DAC7631E               |  |   | DAC7631EB   |   |   | UNITS   |
|--|---|------------------------|--|---|-------------|---|---|---|
|  |   | MIN                    | TYP  | MAX   | MIN         | TYP   | MAX   |   |
| <b>ACCURACY</b><br>Linearity Error <sup>(1)</sup><br>Differential Linearity Error<br>Monotonicity, $T_{MIN}$ to $T_{MAX}$<br>Zero Scale Error<br>Zero Scale Error Drift<br>Full-Scale Error<br>Full-Scale Error Drift<br>Power Supply Rejection Ratio (PSRR) | At Full Scale   | 14                     | $\pm 3$<br>$\pm 2$<br>$\pm 1$<br>5<br>$\pm 1$<br>5<br>10 | $\pm 4$<br>$\pm 3$<br>$\pm 2$<br>10<br>$\pm 2$<br>10<br>100 | 15          | $\pm 2$<br>$\pm 1$<br>*<br>*<br>*<br>*<br>* | $\pm 3$<br>$\pm 2$<br>*<br>*<br>*<br>*<br>* | LSB<br>LSB<br>Bits<br>mV<br>ppm/°C<br>mV<br>ppm/°C<br>ppm/V |
| <b>ANALOG OUTPUT</b><br>Voltage Output<br>Output Current<br>Maximum Load Capacitance<br>Short-Circuit Current<br>Short-Circuit Duration  | $V_{REFL} = 0V$ , $V_{SS} = 0V$ , $R_L = 10k\Omega$<br><br>No Oscillation<br><br>GND or $V_{CC}$                                | 0<br>-1.25             | 500<br>$\pm 30$<br>Indefinite                            | $V_{REFH}$<br>+1.25   | *<br>*      | *<br>*<br>*<br>*                            | *<br>*                                      | V<br>mA<br>pF<br>mA   |
| <b>REFERENCE INPUT</b><br>Ref High Input Voltage Range<br>Ref Low Input Voltage Range<br>Ref High Input Current<br>Ref Low Input Current   |   | $V_{REFL} + 1.25$<br>0 | 250<br>-250  | +2.5<br>$V_{REFH} - 1.25$                                   | *<br>*      | *<br>*<br>*                                 | *<br>*                                      | V<br>V<br>$\mu A$<br>$\mu A$                                |
| <b>DYNAMIC PERFORMANCE</b><br>Settling Time<br>Digital Feedthrough<br>Output Noise Voltage, $f = 10kHz$<br>DAC Glitch  | To $\pm 0.003\%$ , 2.5V Output Step<br><br><br>7FFF <sub>H</sub> to 8000 <sub>H</sub> or 8000 <sub>H</sub> to 7FFF <sub>H</sub> |                        | 8<br>2<br>60<br>40                                       | 10  |             | *<br>*<br>*<br>*                            | *<br>*                                      | $\mu s$<br>nV-s<br>nV/ $\sqrt{Hz}$<br>nV-s                  |
| <b>DIGITAL INPUT</b><br>$V_{IH}$<br>$V_{IL}$<br>$I_{IH}$<br>$I_{IL}$   |   | $0.7 \cdot V_{DD}$     |  | $0.3 \cdot V_{DD}$<br>$\pm 10$<br>$\pm 10$                  | *           |   | *<br>*<br>*                                 | V<br>V<br>$\mu A$<br>$\mu A$                                |
| <b>DIGITAL OUTPUT</b><br>$V_{OH}$<br>$V_{OL}$  | $I_{OH} = -0.8mA$<br>$I_{OL} = 1.6mA$   | 3.6                    | 4.5<br>0.3   | 0.4   | *           | *<br>*                                      | *<br>*                                      | V<br>V  |
| <b>POWER SUPPLY</b><br>$V_{DD}$<br>$V_{CC}$<br>$V_{SS}$<br>$I_{CC}$<br>$I_{DD}$<br>Power   |   | +4.75<br>+4.75<br>0    | +5.0<br>+5.0<br>0<br>0.4<br>50<br>1.8                    | +5.25<br>+5.25<br>0<br>0.5<br>2.5                           | *<br>*<br>* | *<br>*<br>*<br>*<br>*<br>*                  | *<br>*<br>*<br>*<br>*<br>*                  | V<br>V<br>V<br>mA<br>$\mu A$<br>mW                          |
| <b>TEMPERATURE RANGE</b><br>Specified Performance  |   | -40                    |  | +85   | *           |   | *   | °C  |

NOTE: (1) If  $V_{SS} = 0V$  specification applies at Code 0040<sub>H</sub> and above due to possible negative zero-scale error.

\* Specifications same as DAC7631E.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

|   |                                |
|---|--------------------------------|
| $V_{DD}$ to $V_{SS}$ .....              | -0.3V to +11V                  |
| $V_{DD}$ to GND .....                   | -0.3V to +5.5V                 |
| $V_{REFL}$ to $V_{SS}$ .....            | -0.3V to ( $V_{DD} - V_{SS}$ ) |
| $V_{DD}$ to $V_{REFH}$ .....            | -0.3V to ( $V_{DD} - V_{SS}$ ) |
| $V_{REFH}$ to $V_{REFL}$ .....          | -0.3V to ( $V_{DD} - V_{SS}$ ) |
| Digital Input Voltage to GND .....      | -0.3V to $V_{DD} + 0.3V$       |
| Maximum Junction Temperature .....      | +150°C                         |
| Operating Temperature Range .....       | -40°C to +85°C                 |
| Storage Temperature Range .....         | -65°C to +150°C                |
| Lead Temperature (soldering, 10s) ..... | +300°C                         |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

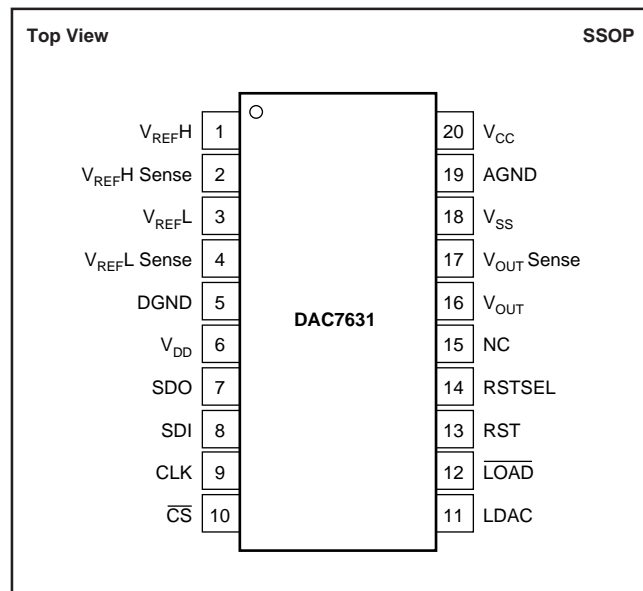
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

| PRODUCT        | MAXIMUM LINEARITY ERROR (LSB) | MAXIMUM DIFFERENTIAL LINEARITY (LSB) | PACKAGE      | PACKAGE DRAWING NUMBER | SPECIFICATION TEMPERATURE RANGE | ORDERING NUMBER <sup>(1)</sup> | TRANSPORT MEDIA        |
|----------------|-------------------------------|--------------------------------------|--------------|------------------------|---------------------------------|--------------------------------|------------------------|
| DAC7631E<br>"  | ±4<br>"                       | ±3<br>"                              | SSOP-20<br>" | 334<br>"               | -40°C to +85°C<br>"             | DAC7631E<br>DAC7631E/1K        | Rails<br>Tape and Reel |
| DAC7631EB<br>" | ±3<br>"                       | ±2<br>"                              | SSOP-20<br>" | 334<br>"               | -40°C to +85°C<br>"             | DAC7631EB<br>DAC7631EB/1K      | Rails<br>Tape and Reel |

NOTE : (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "DAC7631E/1K" will get a single 1000-piece Tape and Reel.

## PIN CONFIGURATION

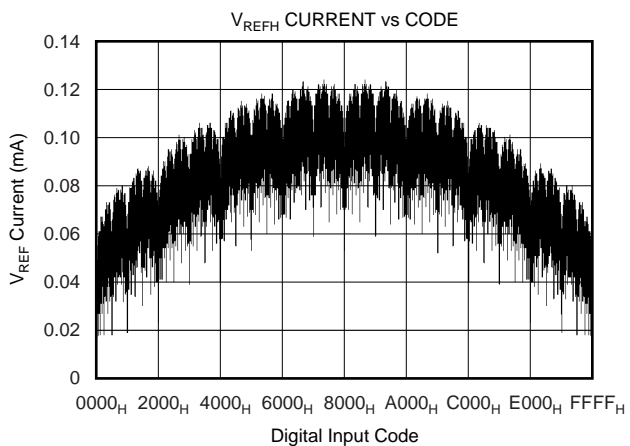
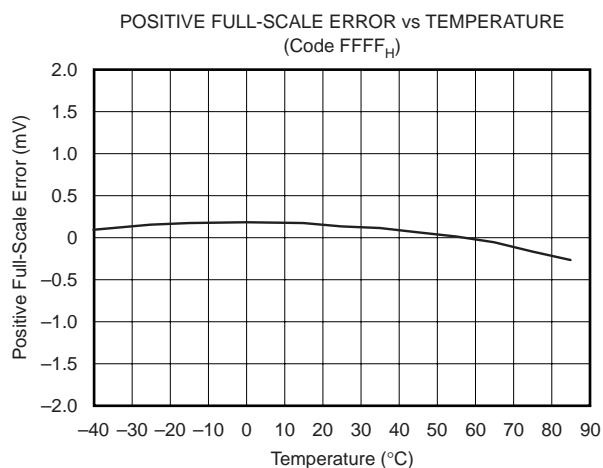
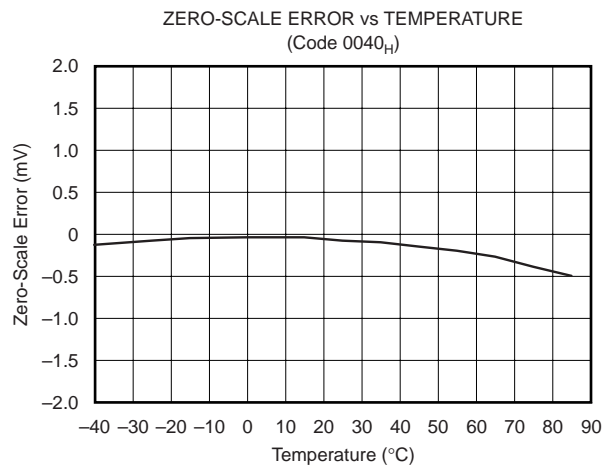
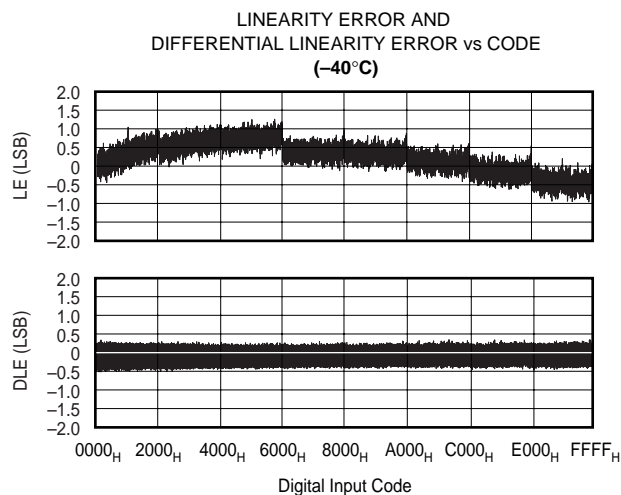
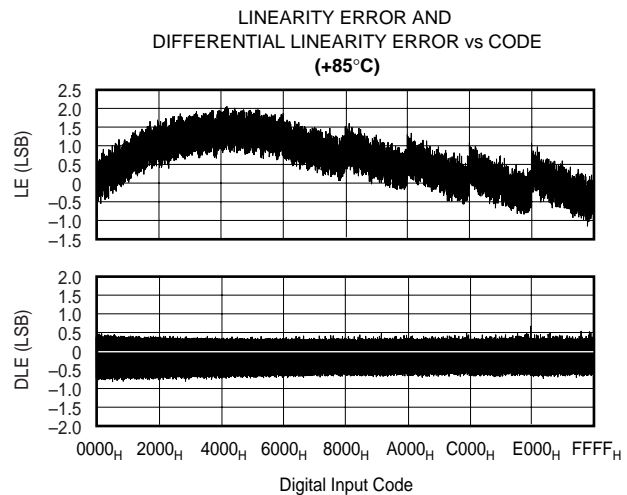
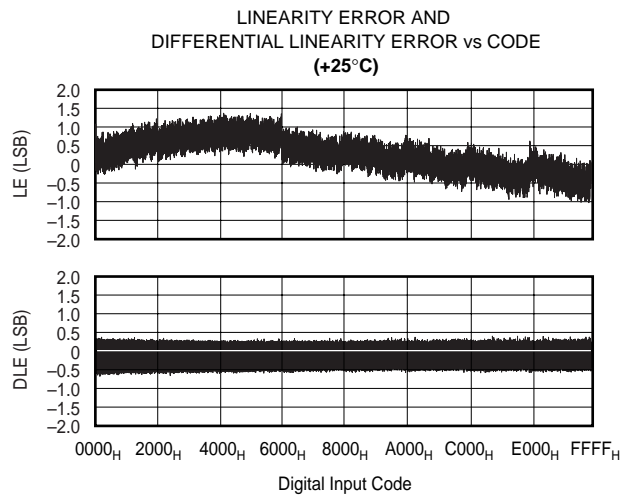


## PIN DESCRIPTIONS

| PIN | LABEL             | DESCRIPTION  |
|-----|-------------------|--|
| 1   | $V_{REFH}$        | DAC Reference High Input   |
| 2   | $V_{REFH}$ Sense  | DAC Reference Sense High Input   |
| 3   | $V_{REFL}$        | DAC Reference Low Input  |
| 4   | $V_{REFL}$ Sense  | DAC Reference Sense Low Input  |
| 5   | DGND              | Digital Ground   |
| 6   | $V_{DD}$          | Logic Power Supply   |
| 7   | SDO               | Serial Data Output   |
| 8   | SDI               | Serial Data Input  |
| 9   | CLK               | Data Clock   |
| 10  | $\overline{CS}$   | Chip Select, Active LOW.   |
| 11  | LDAC              | DAC Register Load Control, Rising Edge Triggered.  |
| 12  | $\overline{LOAD}$ | DAC Input Register Load Control, Active LOW.   |
| 13  | RST               | Reset, Rising Edge. Depending on the state of RSTSEL, the DAC Register is set to either midscale or zero.  |
| 14  | RSTSEL            | Reset Select. Determines the action of RST. If HIGH, a RST command will set the DAC register to midscale. If low, a RST command will set the DAC register to zero. |
| 15  | NC                | No Connection  |
| 16  | $V_{OUT}$         | DAC Voltage Output   |
| 17  | $V_{OUT}$ Sense   | DAC Output Amplifier Inverting Input, Used to Close the Feedback Loop at the Load.   |
| 18  | $V_{SS}$          | Negative Power Supply  |
| 19  | AGND              | Analog Ground  |
| 20  | $V_{CC}$          | Positive Power Supply  |

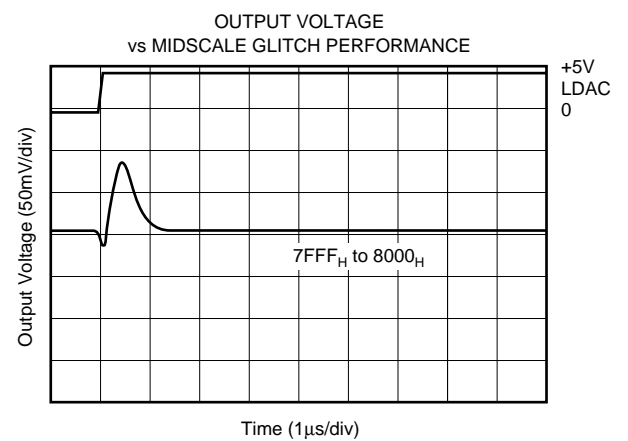
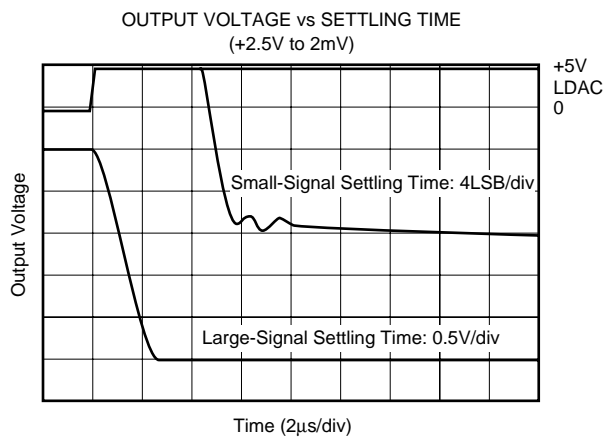
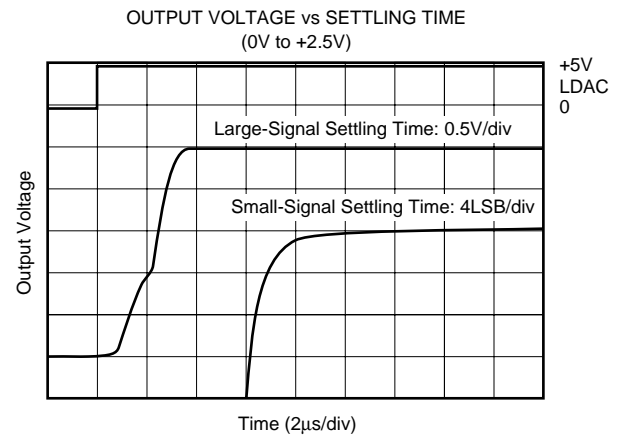
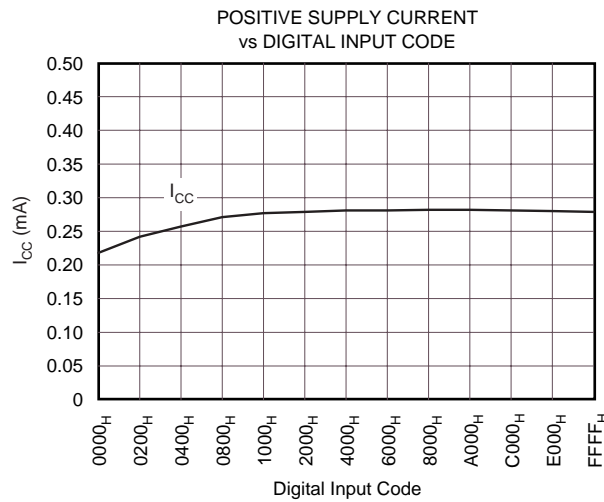
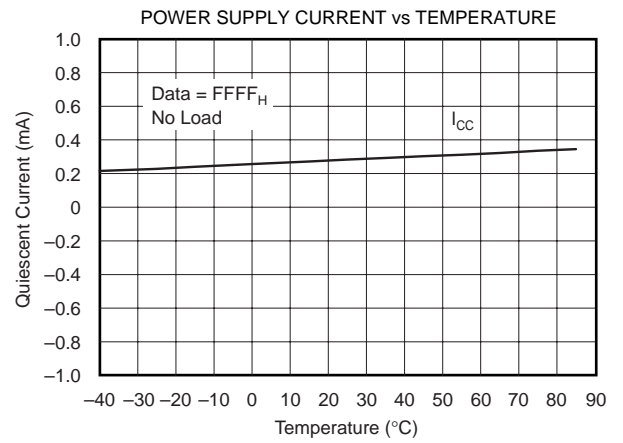
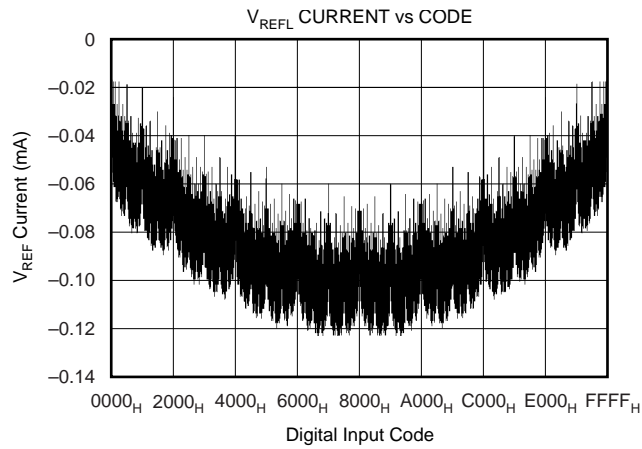
# TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$

At  $T_A = +25^\circ C$ ,  $V_{DD} = V_{CC} = +5V$ ,  $V_{SS} = 0V$ ,  $V_{REFH} = +2.5V$ , and  $V_{REFL} = 0V$ , representative unit, unless otherwise specified.



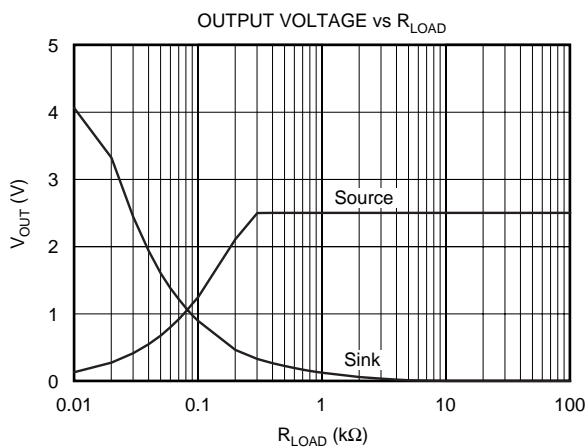
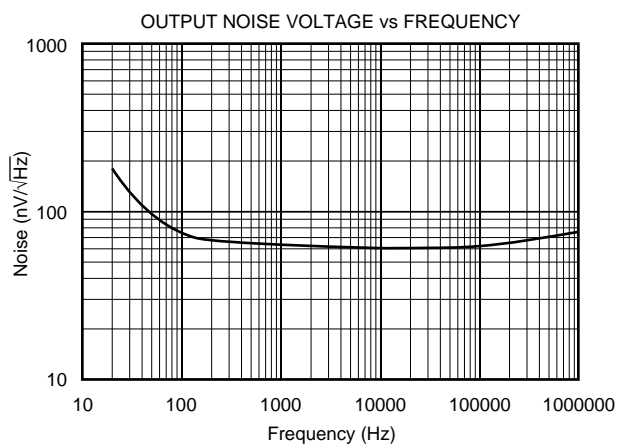
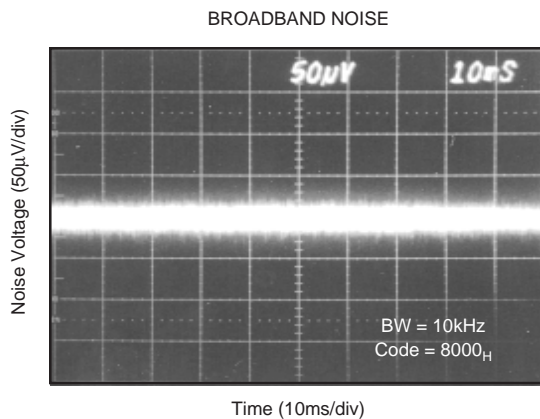
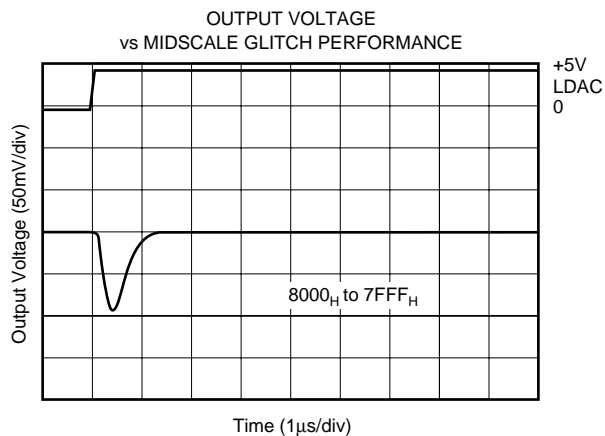
# TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (Cont.)

At  $T_A = +25^\circ C$ ,  $V_{DD} = V_{CC} = +5V$ ,  $V_{SS} = 0V$ ,  $V_{REFH} = +2.5V$ , and  $V_{REFL} = 0V$ , representative unit, unless otherwise specified.



# TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (Cont.)

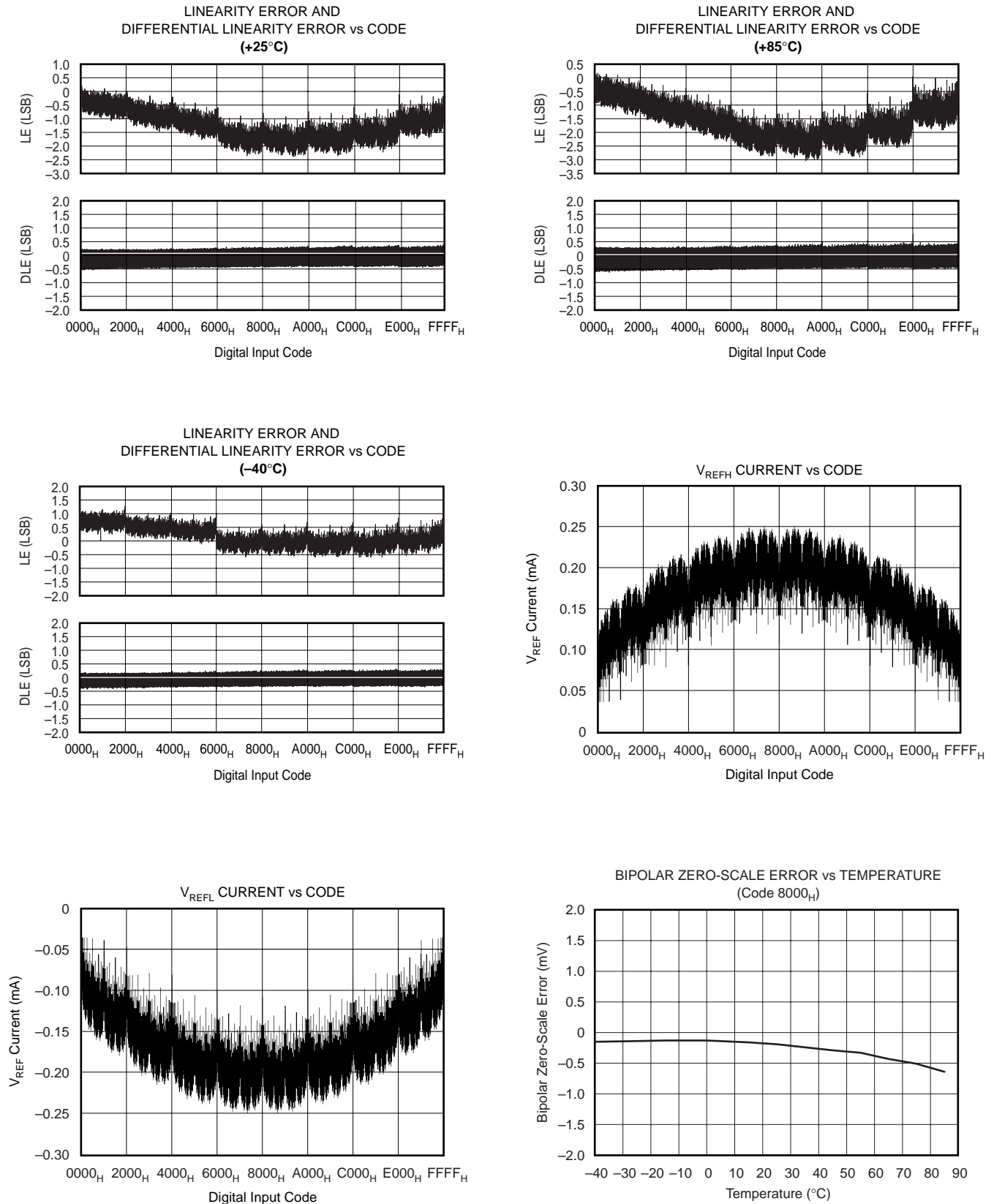
At  $T_A = +25^\circ C$ ,  $V_{DD} = V_{CC} = +5V$ ,  $V_{SS} = 0V$ ,  $V_{REFH} = +2.5V$ , and  $V_{REFL} = 0V$ , representative unit, unless otherwise specified.





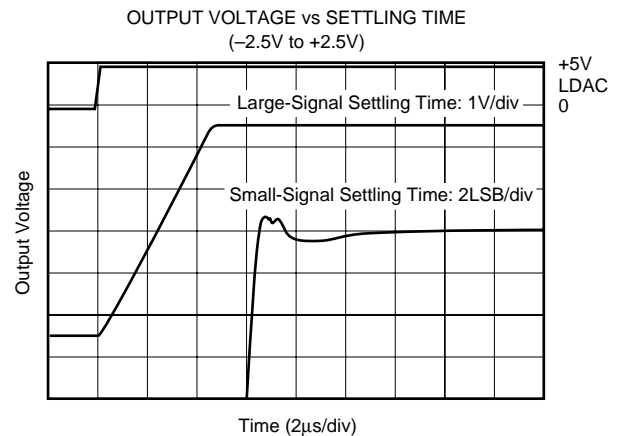
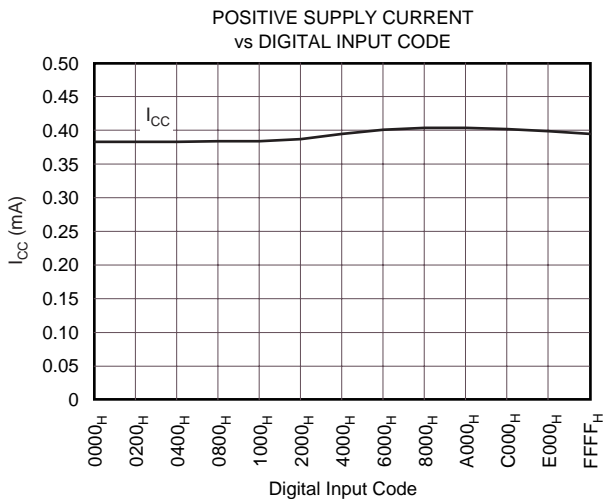
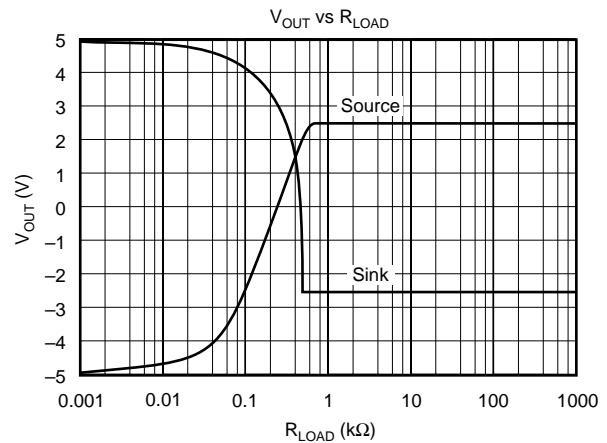
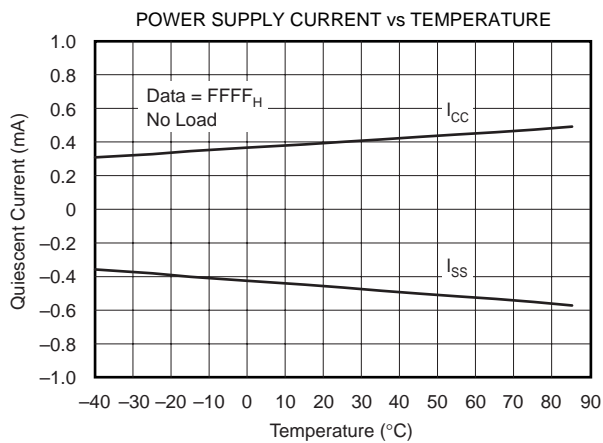
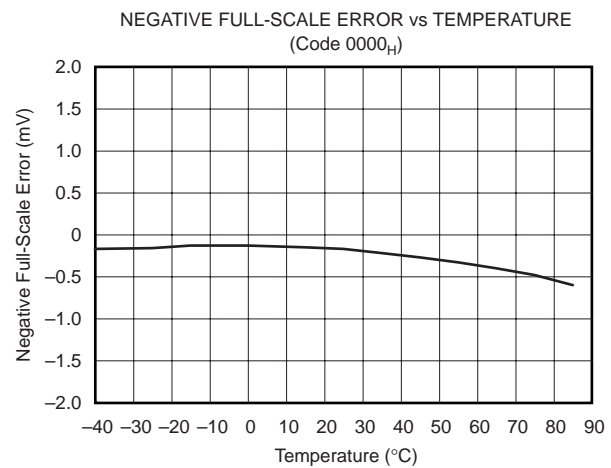
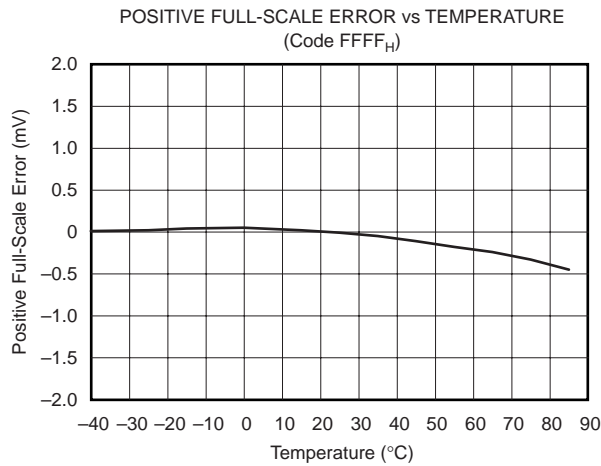
# TYPICAL PERFORMANCE CURVES: $V_{SS} = -5V$

At  $T_A = +25^\circ C$ ,  $V_{DD} = V_{CC} = +5V$ ,  $V_{SS} = -5V$ ,  $V_{REFH} = +2.5V$ , and  $V_{REFL} = -2.5V$ , representative unit, unless otherwise specified.



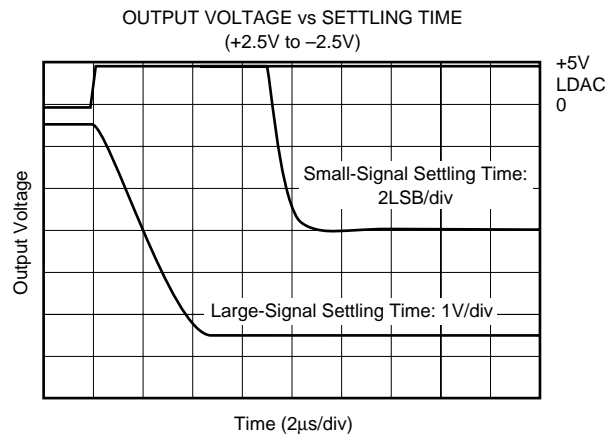
# TYPICAL PERFORMANCE CURVES: $V_{SS} = -5V$ (Cont.)

At  $T_A = +25^\circ C$ ,  $V_{DD} = V_{CC} = +5V$ ,  $V_{SS} = -5V$ ,  $V_{REFH} = +2.5V$ , and  $V_{REFL} = -2.5V$ , representative unit, unless otherwise specified.



## TYPICAL PERFORMANCE CURVES: $V_{SS} = -5V$ (Cont.)

At  $T_A = +25^\circ C$ ,  $V_{DD} = V_{CC} = +5V$ ,  $V_{SS} = -5V$ ,  $V_{REFH} = +2.5V$ , and  $V_{REFL} = -2.5V$ , representative unit, unless otherwise specified.



## THEORY OF OPERATION

The DAC7631 is a 16-bit voltage-output Digital-to-Analog Converter (DAC). The architecture is an R-2R ladder configuration with the three MSB's segmented, followed by an operational amplifier that serves as a buffer, as shown in Figure 1. The minimum voltage output (zero-scale) and maximum voltage output (full-scale) are set by external voltage references at  $V_{REFL}$  and  $V_{REFH}$ , respectively.

The digital input is a 16-bit serial word representing the 16-bit DAC input code, sent MSB first. The DAC7631 can be powered from either a single +5V supply or a dual  $\pm 5V$  supply. The device offers a reset function which immediately sets the output voltage and DAC register to mid-scale code (8000H) or to zero-scale code (0000H). See Figures 2 and 3 for the basic operation of the DAC7631.

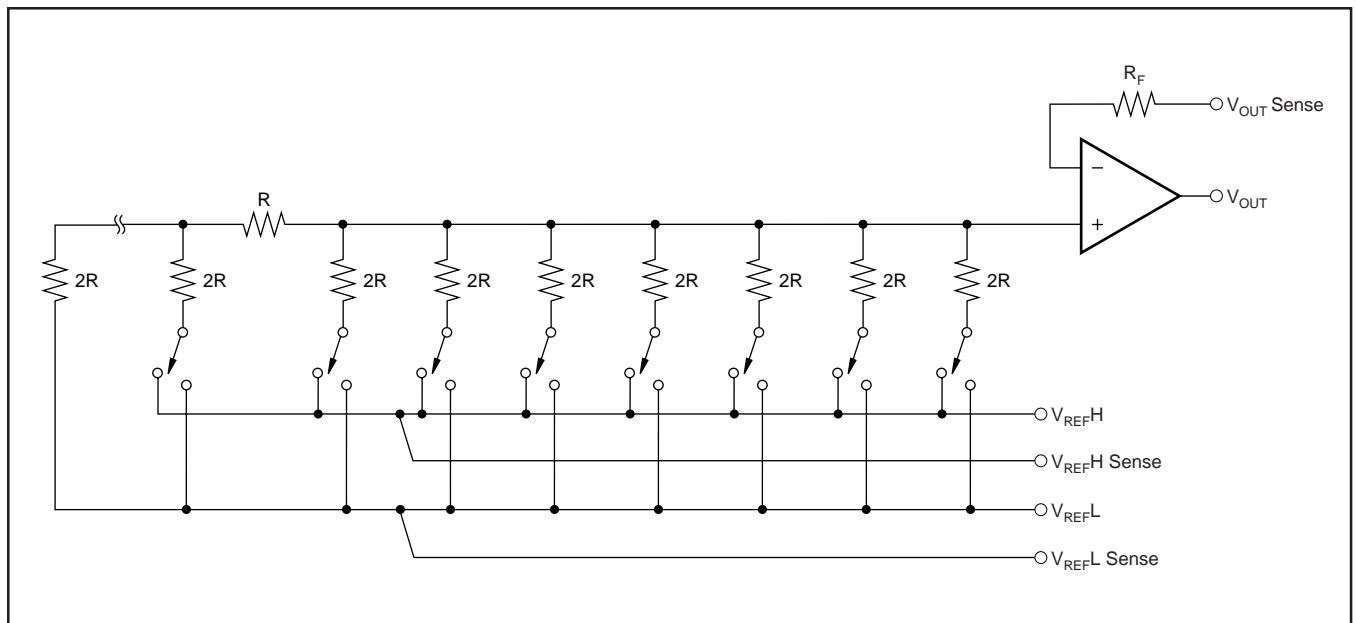


FIGURE 1. DAC7631 Architecture.

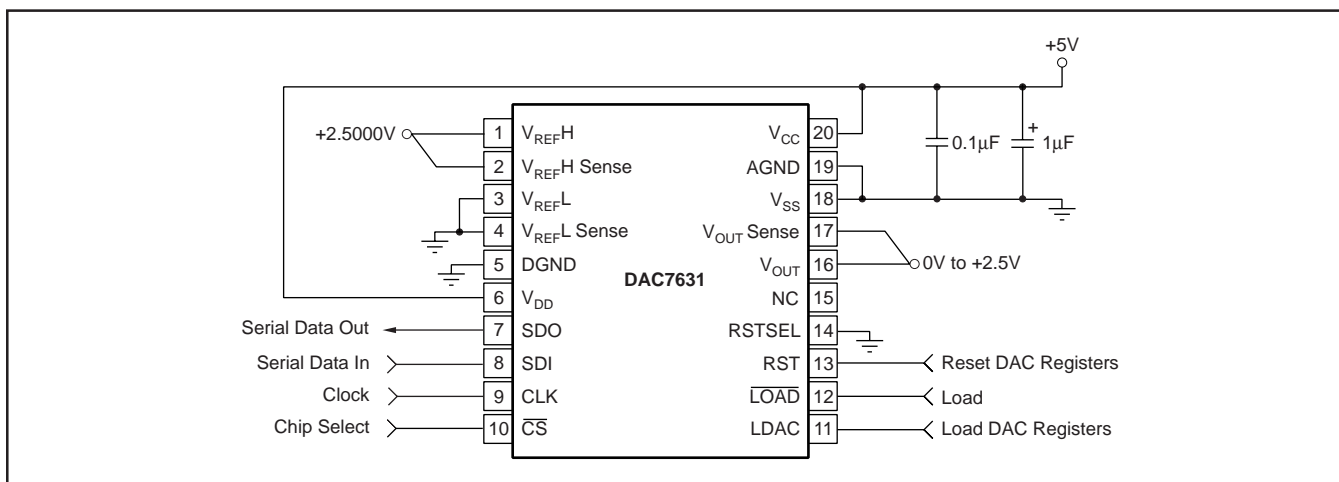


FIGURE 2. Basic Single-Supply Operation.

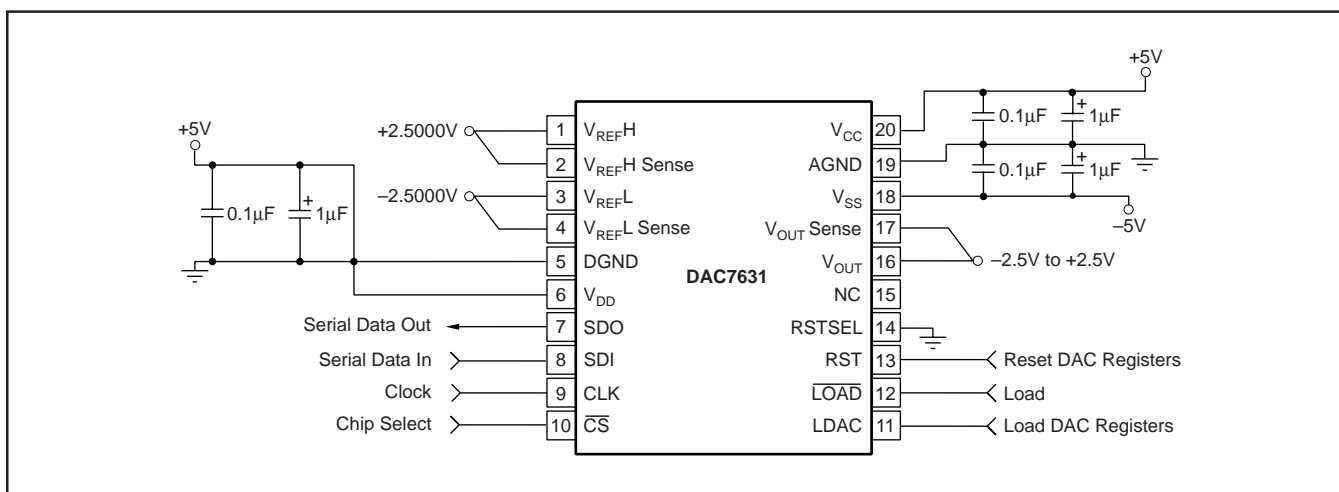


FIGURE 3. Basic Dual-Supply Operation.

## ANALOG OUTPUTS

When  $V_{SS} = -5V$  (dual supply operation), the output amplifier can swing to within 2.25V of the supply rails, guaranteed over the  $-40^{\circ}C$  to  $+85^{\circ}C$  temperature range. When  $V_{SS} = 0V$  (single-supply operation), and with  $R_{LOAD}$  also connected to ground, the output can swing to ground. Care must also be taken when measuring the zero-scale error when  $V_{SS} = 0V$ . Since the output voltage cannot swing below ground, the output voltage may not change for the first few digital input codes (0000<sub>H</sub>, 0001<sub>H</sub>, 0002<sub>H</sub>, etc.) if the output amplifier has a negative offset. At the negative limit of  $-2mV$ , the first specified output starts at code 0040<sub>H</sub>.

Due to the high accuracy of these D/A converters, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 2.5V full-scale range has a 1LSB value of  $38\mu V$ . With a load current of 1mA, series wiring and connector resistance of only  $40m\Omega$  ( $R_{W2}$ ) will cause a voltage drop of  $40\mu V$ , as shown in Figure 4. To understand what this means in terms of a system layout, the resistivity of a typical 1 ounce copper-clad printed circuit board is  $1/2 m\Omega$  per square. For a 1mA

load, a 10 milli-inch wide printed circuit conductor 600 milli-inches long will result in a voltage drop of  $30\mu V$ .

The DAC7631 offers a force and sense output configuration for the high open-loop gain output amplifier. This feature allows the loop around the output amplifier to be closed at the load (as shown in Figure 4), thus ensuring an accurate output voltage.

## REFERENCE INPUTS

The reference inputs,  $V_{REFL}$  and  $V_{REFH}$ , can be any voltage between  $V_{SS} + 2.5V$  and  $V_{CC} - 2.5V$ , provided that  $V_{REFH}$  is at least 1.25V greater than  $V_{REFL}$ . The minimum output of each DAC is equal to  $V_{REFL}$  plus a small offset voltage (essentially, the offset of the output op amp). The maximum output is equal to  $V_{REFH}$  plus a similar offset voltage. Note that  $V_{SS}$  (the negative power supply) must either be connected to ground or must be in the range of  $-4.75V$  to  $-5.25V$ . The voltage on  $V_{SS}$  sets several bias points within the converter. If  $V_{SS}$  is not in one of these two configurations, the bias values may be in error and proper operation of the device is not guaranteed.

The current into the  $V_{REFH}$  input and out of  $V_{REFL}$  depends on the DAC output voltage, and can vary from a few microamps to approximately 0.3mA in dual supply or 0.15mA in single-supply operation. The reference input appears as a varying load to the reference. If the reference can sink or source the required current, a reference buffer is not required. The DAC7631 features a reference drive and sense connection such that the internal errors caused by the changing reference current and the circuit impedances can be minimized. Figures 5 through 13 show different reference configurations, and the effect on the linearity and differential linearity.

## DIGITAL INTERFACE

Table I shows the basic control logic for the DAC7631. The interface consists of a serial clock input (CLK), serial data input (SDI), DAC input register load control signal ( $\overline{LOAD}$ ), and DAC load control signal (LDAC). In addition, a chip select input ( $\overline{CS}$ ) is provided to simplify device selection in systems with multiple devices. An asynchronous reset input (RST), triggered by a rising edge, is provided to force start-up conditions, periodic resets, or emergency resets to a known state. The action of RST can be selected using the reset select (RSTSEL) pin.

## SERIAL DATA INPUT

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| $\overline{CS}$ | RST        | RSTSEL | LDAC       | $\overline{LOAD}$ | INPUT REGISTER    | DAC REGISTER      | MODE              |
|-----------------|------------|--------|------------|-------------------|-------------------|-------------------|-------------------|
| L               | H          | X      | X          | L                 | Write             | Hold              | Write Input       |
| H               | H          | X      | $\uparrow$ | H                 | Hold              | Write             | Update            |
| H               | H          | X      | H          | H                 | Hold              | Hold              | Hold              |
| X               | $\uparrow$ | L      | X          | X                 | Reset to Zero     | Reset to Zero     | Reset to Zero     |
| X               | $\uparrow$ | H      | X          | X                 | Reset to Midscale | Reset to Midscale | Reset to Midscale |

TABLE I. DAC7631 Logic Truth Table.

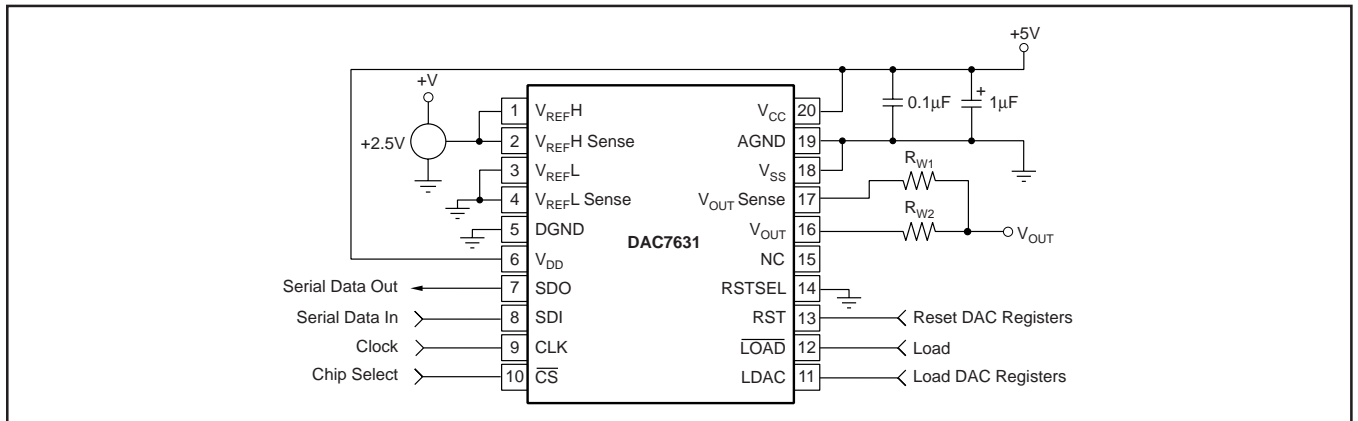


FIGURE 4. Analog Output Closed-loop Configuration.  $R_{W1}$  and  $R_{W2}$  represent wiring resistance.

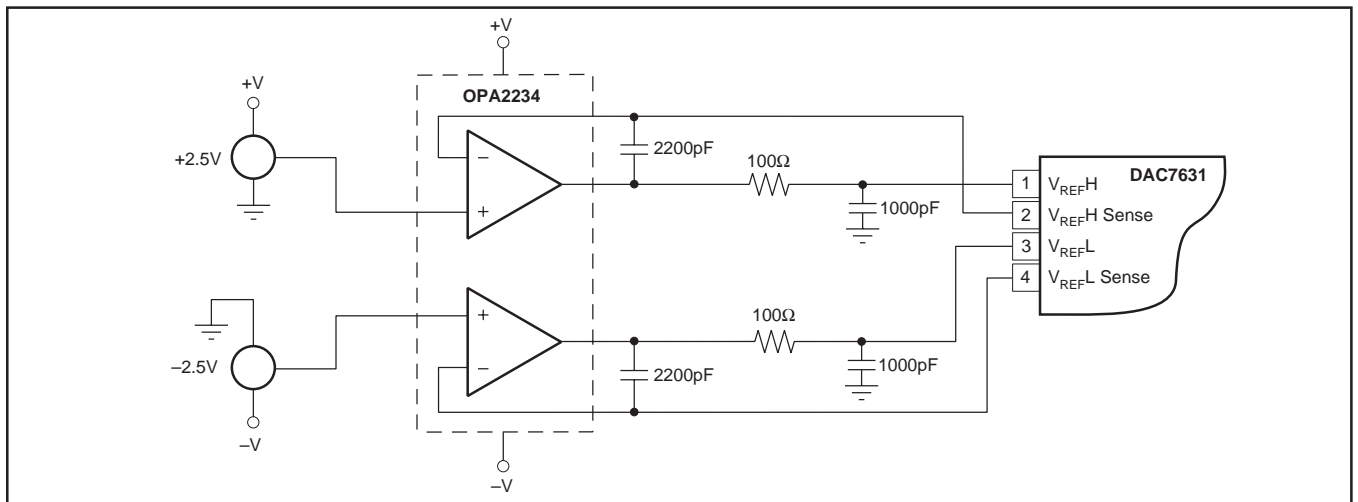


FIGURE 5. Dual-supply Buffered References.

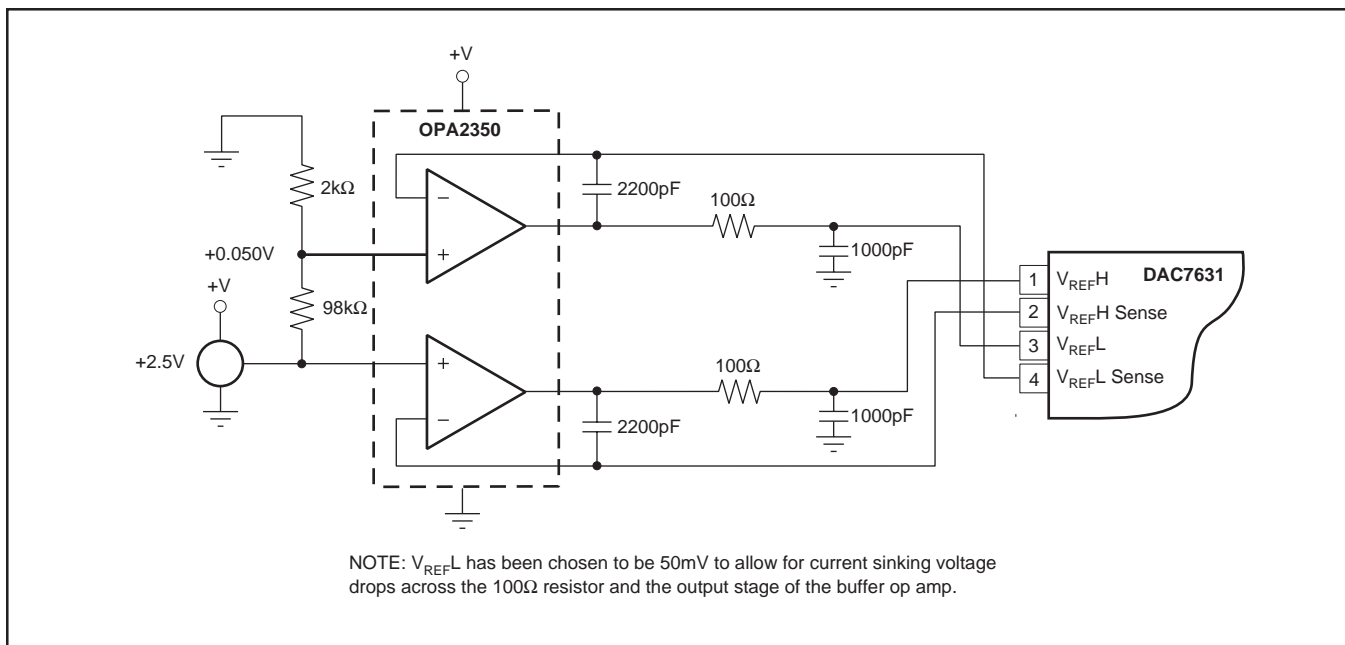


FIGURE 6. Single-supply Buffered Reference,  $V_{REFL} = 50\text{mV}$ .

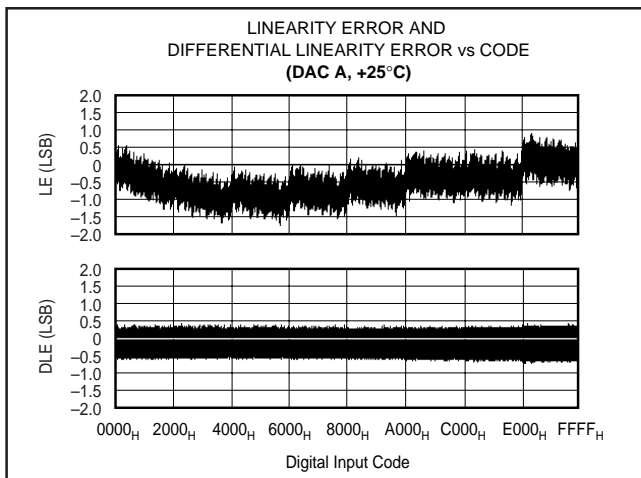


FIGURE 7. Integral Linearity and Differential Linearity Error Curves for Figure 6.

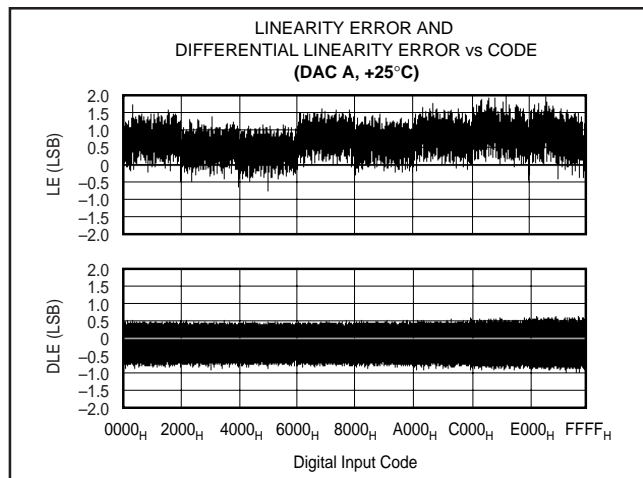


FIGURE 8. Integral Linearity and Differential Linearity Error Curves for Figure 9.

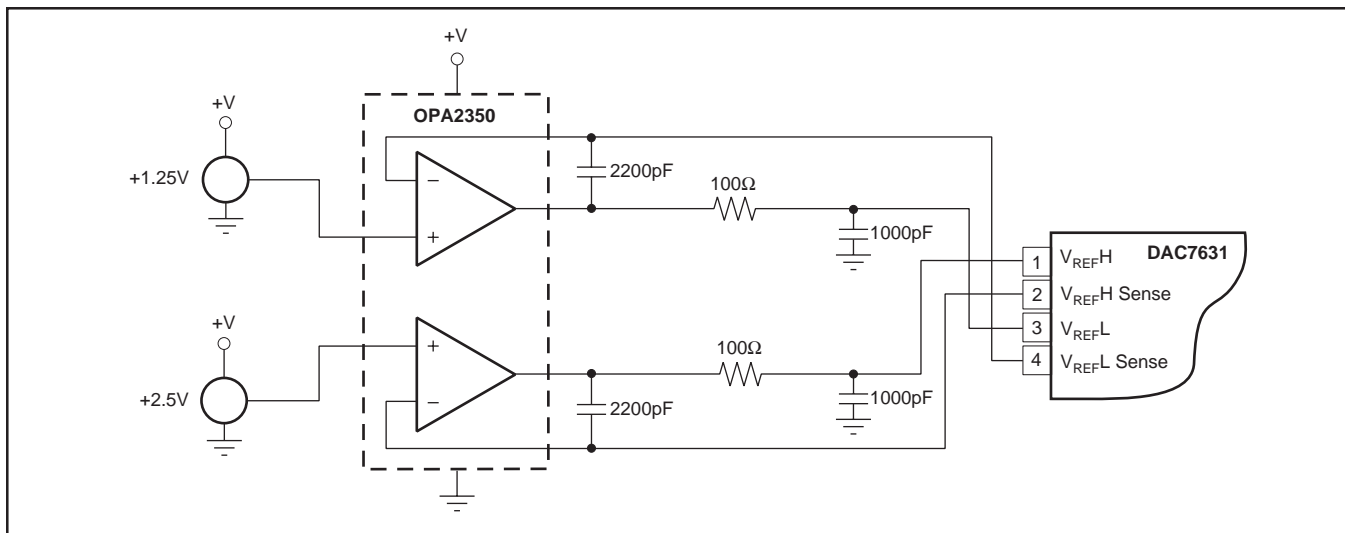


FIGURE 9. Single-supply Buffered Reference,  $V_{REFL} = +1.25\text{V}$ ,  $V_{REFH} = -1.25\text{V}$ .

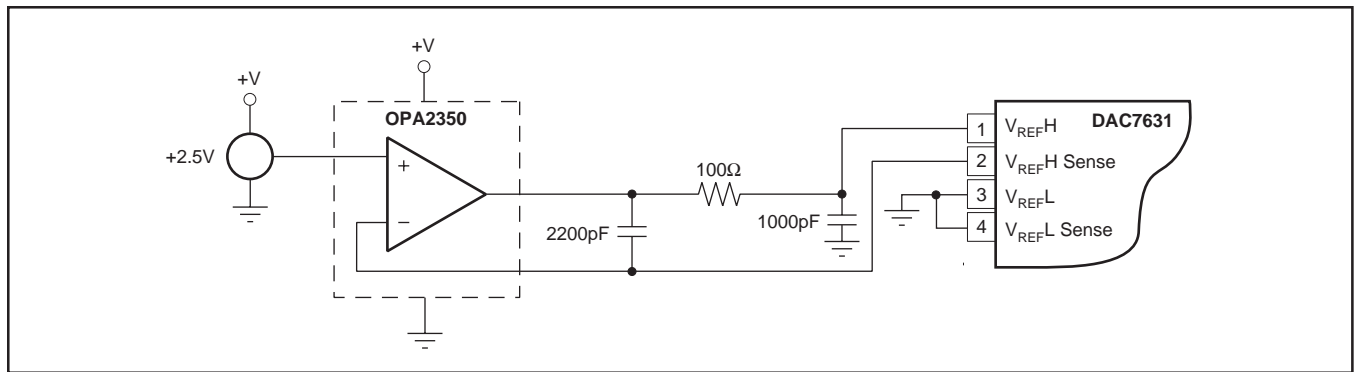


FIGURE 10. Single-supply Buffered  $V_{REFH}$ .

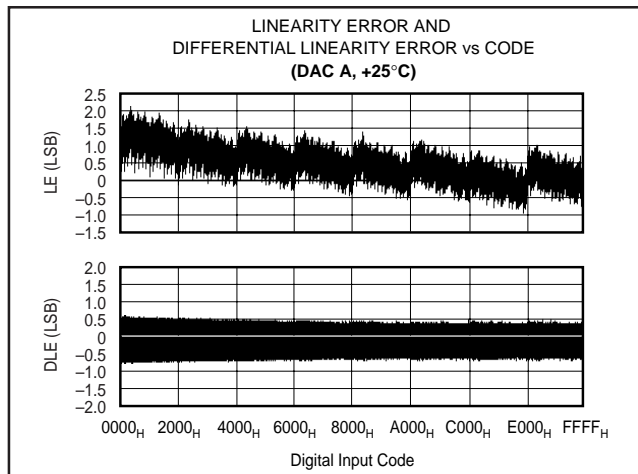


FIGURE 11. Linearity and Differential Error Curves for Figure 10.

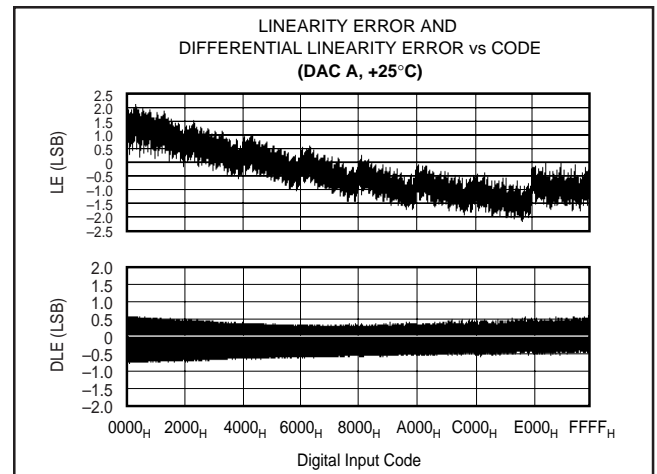


FIGURE 13. Linearity and Differential Error Curves for Figure 12.

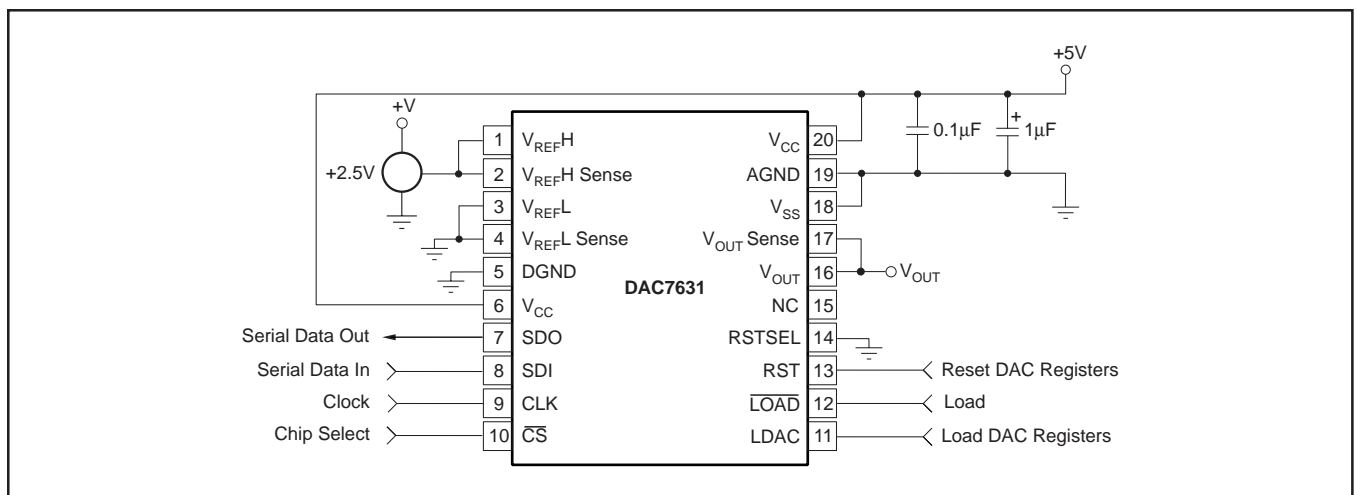


FIGURE 12. Low cost Single-supply Configuration.

Data is shifted into the device through the SDI and CLK pins and arrives in a shift register. Once all 16 bits have been transferred, the  $\overline{\text{LOAD}}$  pin, which is level-sensitive, should be brought low to latch the data into a buffer register called the DAC input register. To latch the new data into the DAC itself, the LDAC pin, which is edge-sensitive, must be brought high. When this is done, the DAC will assume the new value and the output voltage will change (provided that

the new value is different from the old one). Note that settling time is measured from the time that the LDAC pin is brought high, since the device's output does not begin to change until then.

The DAC7631's double-buffering scheme allows the device to be updated through the serial interface without disturbing the voltage on the output pin. It also allows the user to use separate logic for driving the serial input and triggering

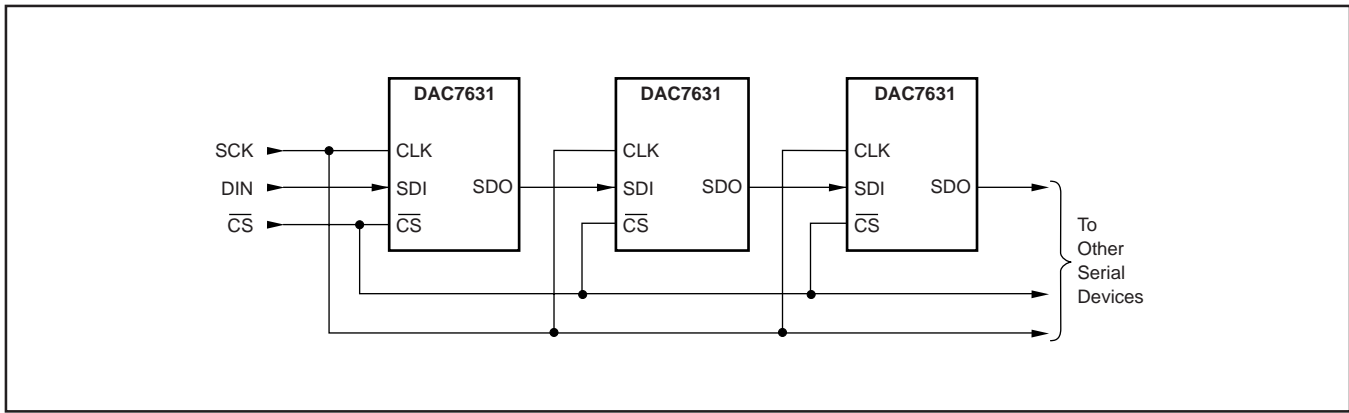


FIGURE 14. Daisy-chaining DAC7631.

DAC updates; i.e., the LDAC pin can be driven with a separate signal, such as a timing clock, which need not be directly related to the serial data timing. This makes it easy to synchronize DAC7631 updates with external events or with other DACs.

Note that  $\overline{CS}$  and CLK are combined with an OR gate, which controls the serial-to-parallel shift register. These two inputs are completely interchangeable. In addition, care must be taken with the state of CLK when  $\overline{CS}$  rises at the end of a serial transfer. If CLK is LOW when  $\overline{CS}$  rises, the OR gate will provide a rising edge to the shift register, shifting the internal data one additional bit. The result will be incorrect data and possible selection of the wrong input register(s). If both  $\overline{CS}$  and CLK are used,  $\overline{CS}$  should rise only when CLK is HIGH. If not, then either  $\overline{CS}$  or CLK can be used to operate the shift register. See Table II for more information.

| $\overline{CS}^{(1)}$ | CLK <sup>(1)</sup> | $\overline{LOAD}$ | RST              | SERIAL SHIFT REGISTER |
|-----------------------|--------------------|-------------------|------------------|-----------------------|
| H <sup>(2)</sup>      | X <sup>(3)</sup>   | H                 | H                | No Change             |
| L <sup>(4)</sup>      | L                  | H                 | H                | No Change             |
| L                     | ↑ <sup>(5)</sup>   | H                 | H                | Advanced One Bit      |
| ↑                     | L                  | H                 | H                | Advanced One Bit      |
| H <sup>(6)</sup>      | X                  | L <sup>(7)</sup>  | H                | No Change             |
| H <sup>(6)</sup>      | X                  | H                 | ↑ <sup>(8)</sup> | No Change             |

NOTES: (1)  $\overline{CS}$  and CLK are interchangeable. (2) H = Logic HIGH. (3) X = Don't Care. (4) L = Logic LOW (5) = Positive Logic Transition. (6) A HIGH value is suggested in order to avoid a "false clock" from advancing the shift register and changing the shift register. (7) If data is clocked into the serial register while  $\overline{LOAD}$  is LOW, the DAC register will change. This will corrupt the data in each DAC register that has been erroneously selected. (8) Rising edge of RST causes no change in the contents of the serial shift register.

TABLE II. Serial Shift Register Truth Table.

## SERIAL-DATA OUTPUT

The Serial-Data Output (SDO) is the internal shift register's output. For DAC7631, the SDO is a driven output and does not require an external pull-up. Any number of DAC7631's can be daisy chained by connecting the SDO pin of one device to the SDI pin of the following device in the chain, as shown in Figure 14.

## DIGITAL TIMING

Figure 15 and Table III provide detailed timing for the digital interface of the DAC7631.

## DIGITAL INPUT CODING

The DAC7631 input data is in Straight Binary format. The output voltage is given by Equation 1:

$$V_{OUT} = V_{REF}L + \frac{(V_{REF}H - V_{REF}L) \cdot N}{65,536} \quad (1)$$

where N is the digital input code. This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.

## DIGITALLY-PROGRAMMABLE CURRENT SOURCE

The DAC7631 offers a unique set of features that allows a wide range of flexibility in designing applications circuits such as programmable current sources. The DAC7631 offers both a differential reference input, as well as an open-loop configuration around the output amplifier. The open-loop configuration around the output amplifier allows a transistor to be placed within the loop to implement a digitally-programmable, unidirectional current source. The availability of a differential reference allows programmability for both the full-scale and zero-scale currents. The output current is calculated as:

$$I_{OUT} = \left( \left( \frac{V_{REF}H - V_{REF}L}{R_{SENSE}} \right) \cdot \left( \frac{N}{65,536} \right) \right) + (V_{REF}L / R_{SENSE}) \quad (2)$$



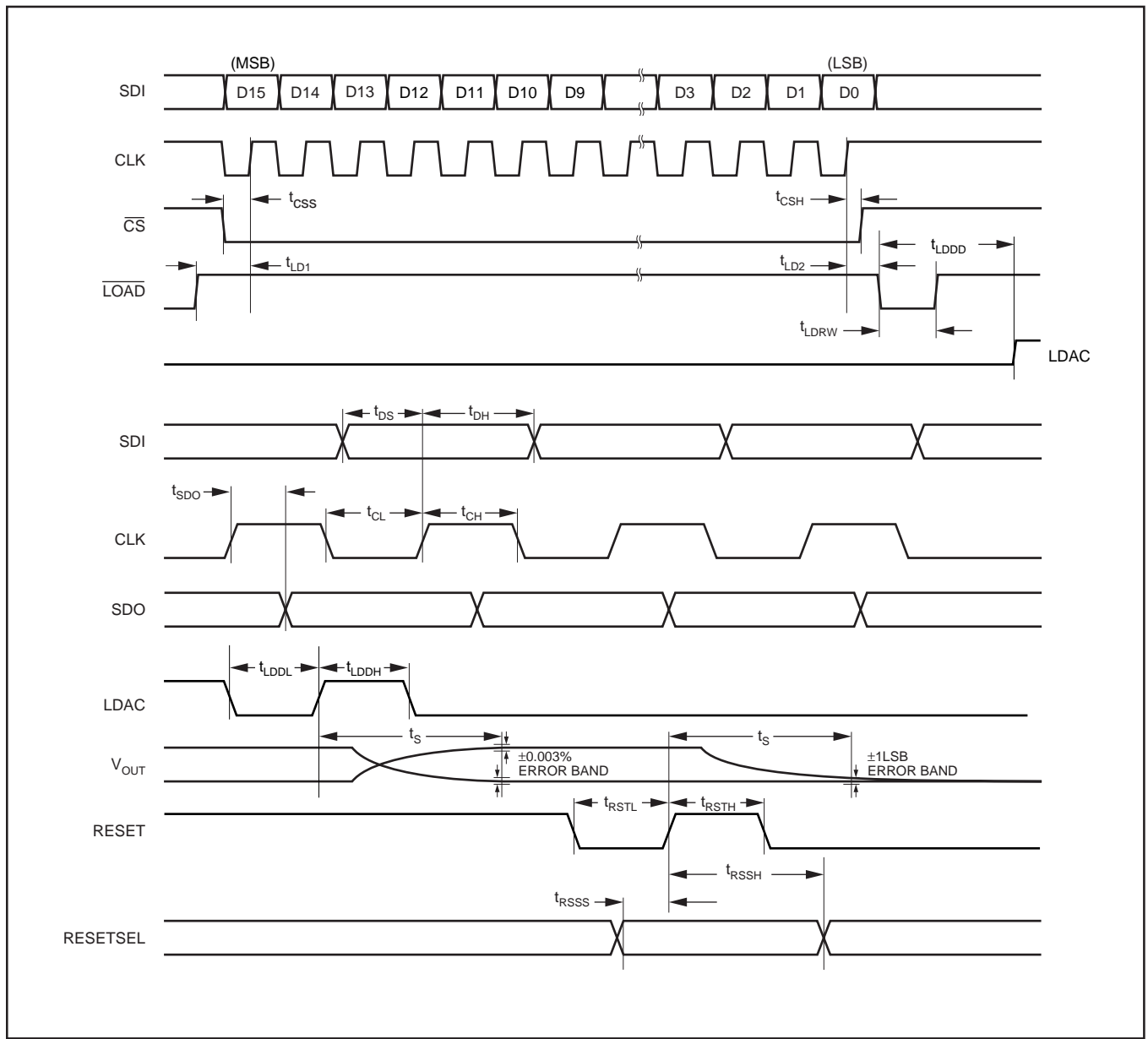


FIGURE 15. Digital Input and Output Timing.

| SYMBOL     | DESCRIPTION                               | MIN | MAX | UNITS   |
|------------|---|-----|-----|---------|
| $t_{DS}$   | Data Valid to CLK Rising                  | 10  |     | ns      |
| $t_{DH}$   | Data Held Valid after CLK Rises           | 20  |     | ns      |
| $t_{CH}$   | CLK HIGH                                  | 25  |     | ns      |
| $t_{CL}$   | CLK LOW                                   | 25  |     | ns      |
| $t_{CSS}$  | $\overline{CS}$ LOW to CLK Rising         | 15  |     | ns      |
| $t_{CSH}$  | CLK HIGH to $\overline{CS}$ Rising        | 0   |     | ns      |
| $t_{LD1}$  | $\overline{LOAD}$ HIGH to CLK Rising      | 10  |     | ns      |
| $t_{LD2}$  | CLK Rising to $\overline{LOAD}$ LOW       | 30  |     | ns      |
| $t_{LDRW}$ | $\overline{LOAD}$ LOW Time                | 30  |     | ns      |
| $t_{LDDL}$ | LDAC LOW Time                             | 100 |     | ns      |
| $t_{LDDH}$ | LDAC HIGH Time                            | 150 |     | ns      |
| $t_{SDO}$  | SDO Propagation Delay                     | 10  | 45  | ns      |
| $t_{RSSS}$ | RESETSEL Valid to RESET HIGH              | 0   |     | ns      |
| $t_{RSSH}$ | RESET HIGH to RESETSEL Not Valid          | 100 |     | ns      |
| $t_{RSTL}$ | RESET LOW Time                            | 10  |     | ns      |
| $t_{RSTH}$ | RESET HIGH Time                           | 10  |     | ns      |
| $t_{LDDD}$ | $\overline{LOAD}$ LOW to LDAC Rising Time | 40  |     | ns      |
| $t_S$      | Settling Time                             |     | 10  | $\mu$ s |

TABLE III. Timing Specifications ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ).

Figure 16 shows a DAC7631 in a 4mA to 20mA current output configuration. The output current can be determined by Equation 3:

At full-scale, the output current is 16mA, plus the 4mA, for the zero current. At zero scale the output current is the offset current of 4mA ( $0.5\text{V}/125\Omega$ ).

$$I_{OUT} = \left( \left( \frac{2.5V - 0.5V}{125\Omega} \right) \cdot \left( \frac{N}{65,536} \right) \right) + \left( \frac{0.5V}{125\Omega} \right) \quad (3)$$

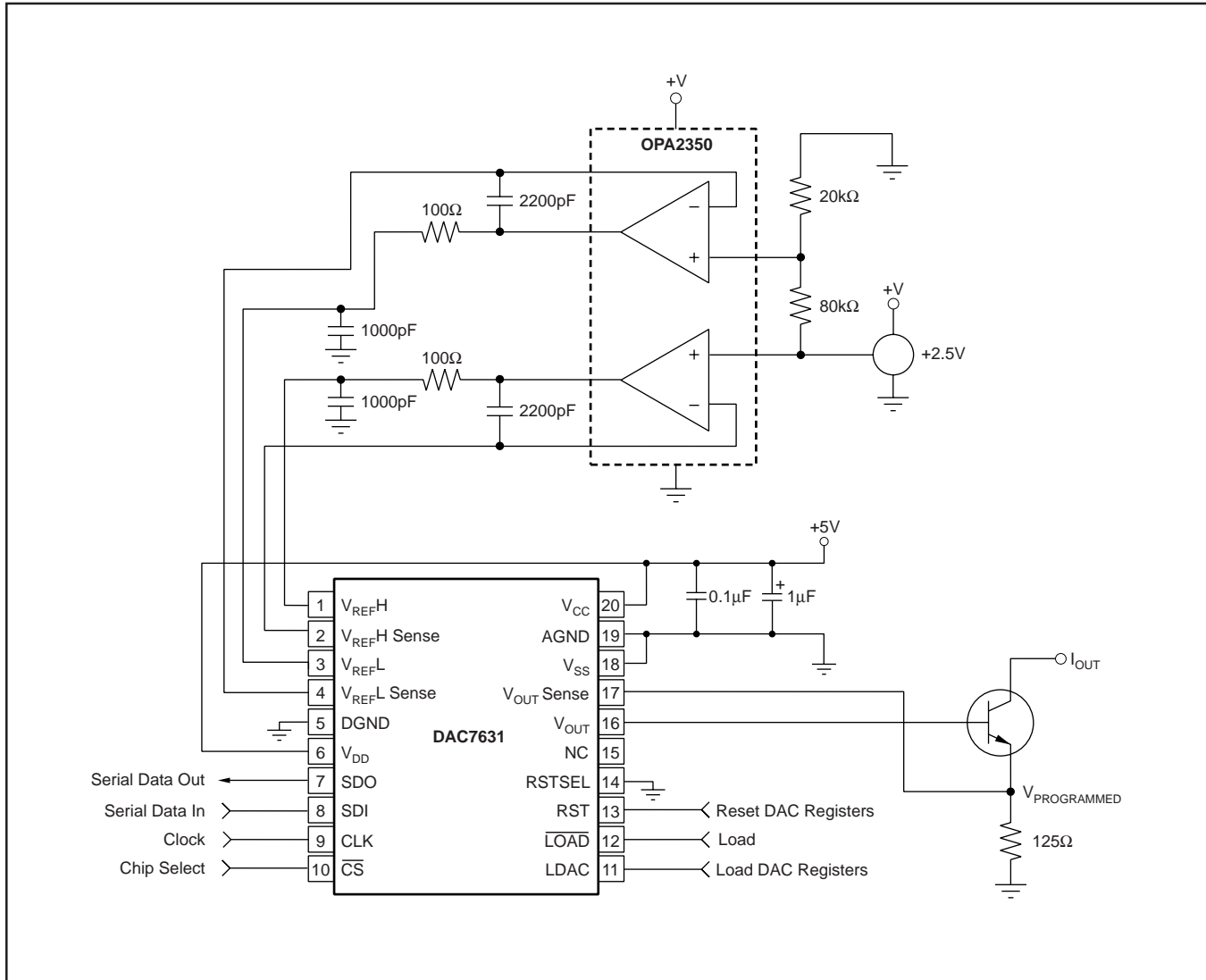


FIGURE 16. 4-to-20mA Digitally Controlled Current Source (1/2 DAC7631).

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">DAC7631E</a>     | Active        | Production           | SSOP (DB)   20 | 70   TUBE             | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 85    | DAC7631E            |
| DAC7631E.A                   | Active        | Production           | SSOP (DB)   20 | 70   TUBE             | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 85    | DAC7631E            |
| <a href="#">DAC7631E/1K</a>  | Active        | Production           | SSOP (DB)   20 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 85    | DAC7631E            |
| DAC7631E/1K.A                | Active        | Production           | SSOP (DB)   20 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 85    | DAC7631E            |
| DAC7631E/1K.B                | Active        | Production           | SSOP (DB)   20 | 1000   LARGE T&R      | -           | Call TI                              | Level-3-260C-168 HR               | -40 to 85    | DAC7631E            |
| <a href="#">DAC7631EB</a>    | Active        | Production           | SSOP (DB)   20 | 70   TUBE             | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 85    | DAC7631E<br>B       |
| DAC7631EB.A                  | Active        | Production           | SSOP (DB)   20 | 70   TUBE             | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 85    | DAC7631E<br>B       |
| <a href="#">DAC7631EB/1K</a> | Active        | Production           | SSOP (DB)   20 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 85    | DAC7631E<br>B       |
| DAC7631EB/1K.A               | Active        | Production           | SSOP (DB)   20 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 85    | DAC7631E<br>B       |
| DAC7631EG4                   | Active        | Production           | SSOP (DB)   20 | 70   TUBE             | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 85    | DAC7631E            |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DAC7631E/1K  | SSOP         | DB              | 20   | 1000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| DAC7631EB/1K | SSOP         | DB              | 20   | 1000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DAC7631E/1K  | SSOP         | DB              | 20   | 1000 | 353.0       | 353.0      | 32.0        |
| DAC7631EB/1K | SSOP         | DB              | 20   | 1000 | 353.0       | 353.0      | 32.0        |

## TUBE



\*All dimensions are nominal

| Device      | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| DAC7631E    | DB           | SSOP         | 20   | 70  | 530    | 10.5   | 4000   | 4.1    |
| DAC7631E.A  | DB           | SSOP         | 20   | 70  | 530    | 10.5   | 4000   | 4.1    |
| DAC7631EB   | DB           | SSOP         | 20   | 70  | 530    | 10.5   | 4000   | 4.1    |
| DAC7631EB.A | DB           | SSOP         | 20   | 70  | 530    | 10.5   | 4000   | 4.1    |
| DAC7631EG4  | DB           | SSOP         | 20   | 70  | 530    | 10.5   | 4000   | 4.1    |

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