

## 4-Mbit (512K x 8) Static RAM

### Features

- Pin- and function-compatible with CY7C1049CV33
- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - $I_{CC} = 90 \text{ mA @ } 10 \text{ ns (Industrial)}$
- Low CMOS standby power
  - $I_{SB2} = 10 \text{ mA}$
- 2.0V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Available in Lead-Free 36-lead (400-mil) Molded SOJ V36 and 44-pin TSOP II ZS44 packages

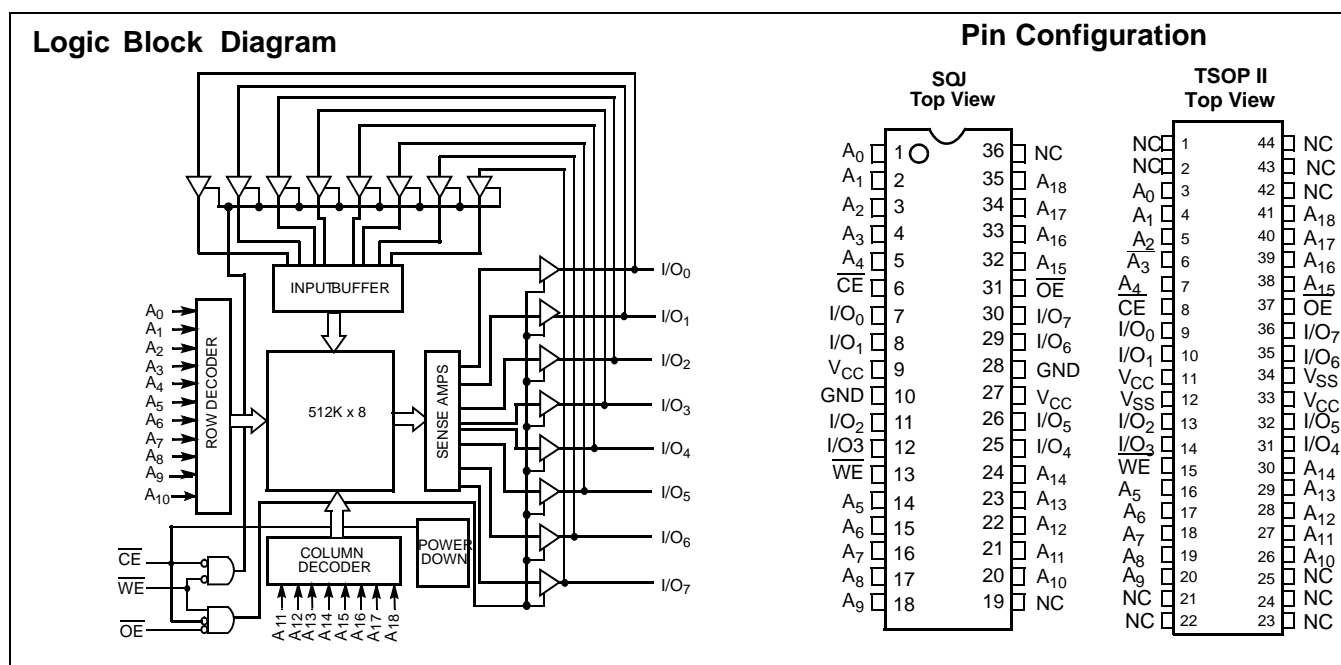
### Functional Description<sup>[1]</sup>

The CY7C1049DV33 is a high-performance CMOS Static RAM organized as 512K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}$ ), an active LOW Output Enable ( $\overline{OE}$ ), and tri-state drivers. Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a Write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1049DV33 is available in standard 400-mil-wide 36-pin SOJ package and 44-pin TSOP II package with center power and ground (revolutionary) pinout.



### Selection Guide

	-10 (Industrial)	-12 (Automotive) <sup>[2]</sup>	Unit
Maximum Access Time	10	12	ns
Maximum Operating Current	90	95	mA
Maximum CMOS Standby Current	10	15	mA

#### Notes:

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).
2. Automotive product information is Preliminary.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  to Relative GND<sup>[3]</sup> .... -0.3V to +4.6V

DC Voltage Applied to Outputs

in High-Z State<sup>[3]</sup> ..... -0.3V to  $V_{CC} + 0.3V$

DC Input Voltage<sup>[3]</sup> ..... -0.3V to  $V_{CC} + 0.3V$

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V

(per MIL-STD-883, Method 3015)

Latch-up Current ..... >200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$	Speed
Industrial	-40°C to +85°C	$3.3V \pm 0.3V$	10 ns
Automotive	-40°C to +125°C	$3.3V \pm 0.3V$	12 ns

## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-10 (Industrial)		-12 (Automotive)		Unit
			Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
$V_{IH}^{[3]}$	Input HIGH Voltage		2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	V
$V_{IL}^{[3]}$	Input LOW Voltage <sup>[3]</sup>		-0.3	0.8	-0.3	0.8	V
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	μA
$I_{OZ}$	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$ , Output Disabled	-1	+1	-1	+1	μA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, f = f_{MAX}$ $= 1/t_{RC}$	100MHz	90		-	mA
			83MHz	80		95	mA
			66MHz	70		85	mA
			40MHz	60		75	mA
$I_{SB1}$	Automatic CE Power-down Current — TTL Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{IH}$ ; $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$		20		25	mA
$I_{SB2}$	Automatic CE Power-down Current — CMOS Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ , or $V_{IN} \leq 0.3V$ , $f = 0$		10		15	mA

## Capacitance<sup>[4]</sup>

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz},$ $V_{CC} = 3.3V$	8	pF
$C_{OUT}$	I/O Capacitance		8	pF

## Thermal Resistance<sup>[4]</sup>

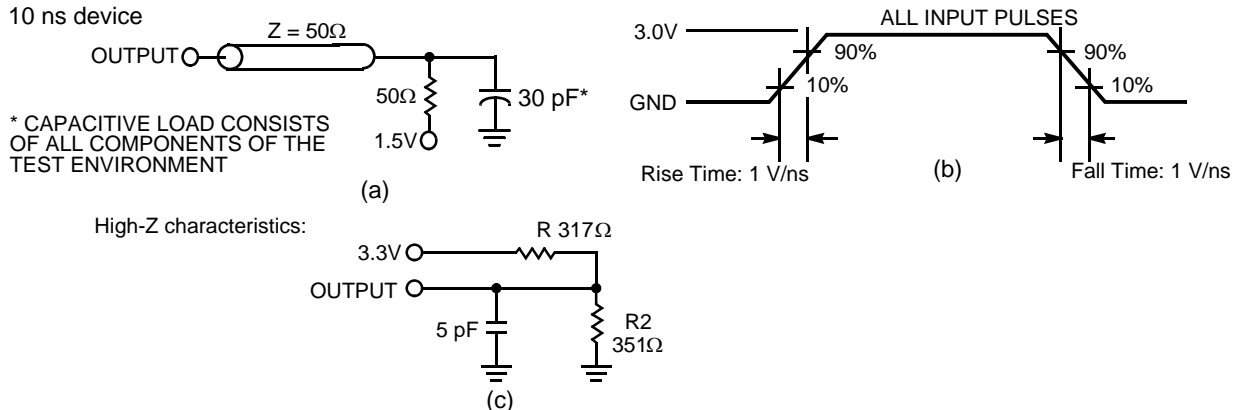
Parameter	Description	Test Conditions	SOJ Package	TSOP II Package	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient) <sup>[4]</sup>	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	57.91	50.66	°C/W
$\Theta_{JC}$	Thermal Resistance (Junction to Case) <sup>[4]</sup>		36.73	17.17	°C/W

### Notes:

3.  $V_{IL} (\text{min.}) = -2.0V$  and  $V_{IH} (\text{max.}) = V_{CC} + 2V$  for pulse durations of less than 20 ns.

4. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms<sup>[5]</sup>



## AC Switching Characteristics<sup>[6]</sup> Over the Operating Range

Parameter	Description	-10 (Industrial)		-12 (Automotive)		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t <sub>power</sub> <sup>[7]</sup>	V <sub>CC</sub> (typical) to the first access	100		100		μs
t <sub>RC</sub>	Read Cycle Time	10		12		ns
t <sub>AA</sub>	Address to Data Valid		10		12	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		ns
t <sub>ACE</sub>	$\overline{\text{CE}}$ LOW to Data Valid		10		12	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ LOW to Data Valid		5		6	ns
t <sub>LZOE</sub>	$\overline{\text{OE}}$ LOW to Low-Z	0		0		ns
t <sub>HZOE</sub>	$\overline{\text{OE}}$ HIGH to High-Z <sup>[8, 9]</sup>		5		6	ns
t <sub>LZCE</sub>	$\overline{\text{CE}}$ LOW to Low-Z <sup>[9]</sup>	3		3		ns
t <sub>HZCE</sub>	$\overline{\text{CE}}$ HIGH to High-Z <sup>[8, 9]</sup>		5		6	ns
t <sub>PU</sub>	$\overline{\text{CE}}$ LOW to Power-up	0		0		ns
t <sub>PD</sub>	$\overline{\text{CE}}$ HIGH to Power-down		10		12	ns
Write Cycle <sup>[10, 11]</sup>						
t <sub>WC</sub>	Write Cycle Time	10		12		ns
t <sub>SCE</sub>	$\overline{\text{CE}}$ LOW to Write End	7		8		ns
t <sub>AW</sub>	Address Set-up to Write End	7		8		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ Pulse Width	7		8		ns
t <sub>SD</sub>	Data Set-up to Write End	5		6		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>LZWE</sub>	$\overline{\text{WE}}$ HIGH to Low-Z <sup>[9]</sup>	3		3		ns
t <sub>HZWE</sub>	$\overline{\text{WE}}$ LOW to High-Z <sup>[8, 9]</sup>		5		6	ns

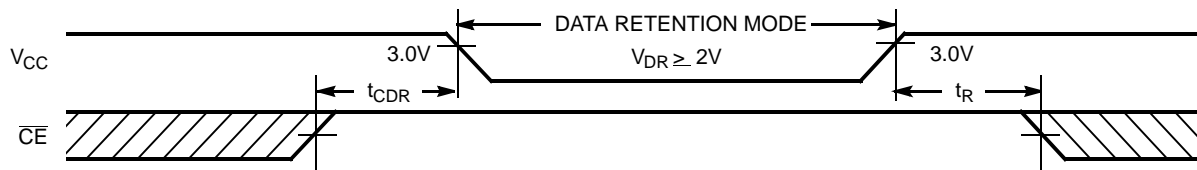
### Notes:

- AC characteristics (except High-Z) are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c).
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{\text{OL}}/I_{\text{OH}}$  and 30-pF load capacitance.
- $t_{\text{POWER}}$  gives the minimum amount of time that the power supply should be at stable, typical  $V_{\text{CC}}$  values until the first memory access can be performed.
- $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ , and  $t_{\text{HZWE}}$  are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured when the outputs enter a high impedance state.
- At any given temperature and voltage condition,  $t_{\text{HZCE}}$  is less than  $t_{\text{LZCE}}$ ,  $t_{\text{HZOE}}$  is less than  $t_{\text{LZOE}}$ , and  $t_{\text{HZWE}}$  is less than  $t_{\text{LZWE}}$  for any given device.
- The internal Write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW, and  $\overline{\text{WE}}$  LOW.  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum Write cycle time for Write Cycle No. 2 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

## Data Retention Characteristics Over the Operating Range

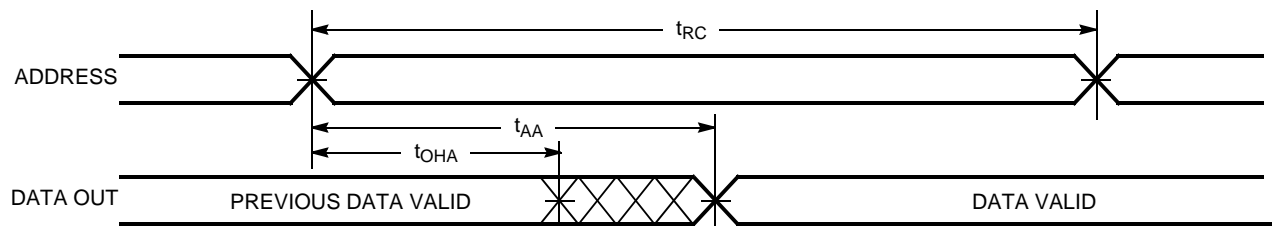
Parameter	Description	Conditions <sup>[13]</sup>	Min.	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0		V
$I_{CCDR}$	Data Retention Current	$V_{CC} = V_{DR} = 2.0V, \overline{CE} \geq V_{CC} - 0.3V$	Ind'l	10	mA
		$V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	Auto	15	mA
$t_{CDR}^{[4]}$	Chip Deselect to Data Retention Time		0		ns
$t_R^{[12]}$	Operation Recovery Time		$t_{RC}$		ns

## Data Retention Waveform

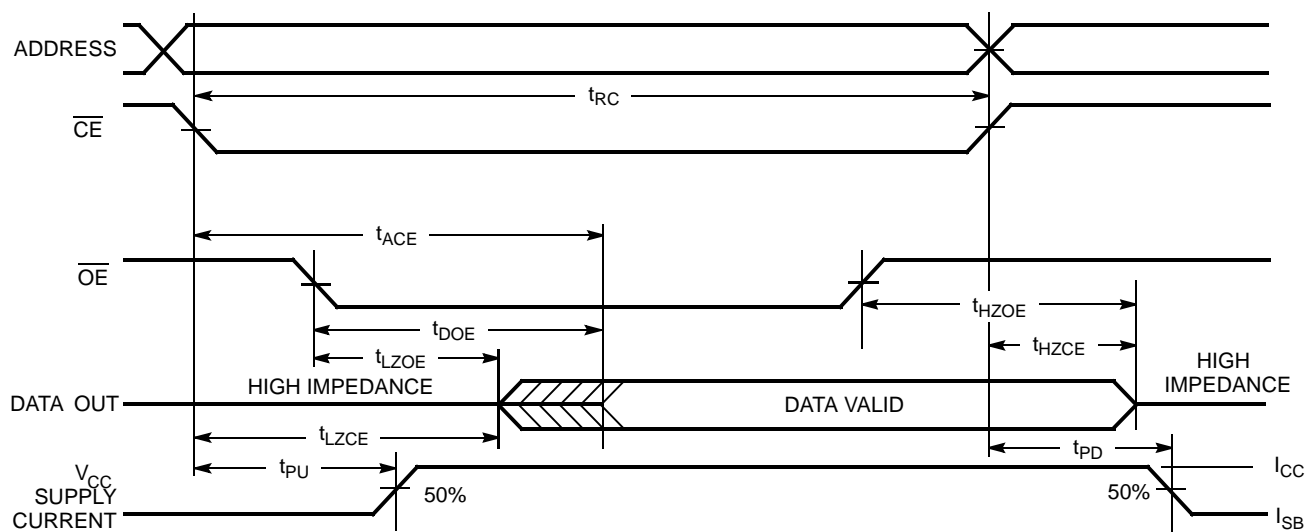


## Switching Waveforms

### Read Cycle No. 1<sup>[14, 15]</sup>



### Read Cycle No. 2 ( $\overline{OE}$ Controlled)<sup>[15, 16]</sup>

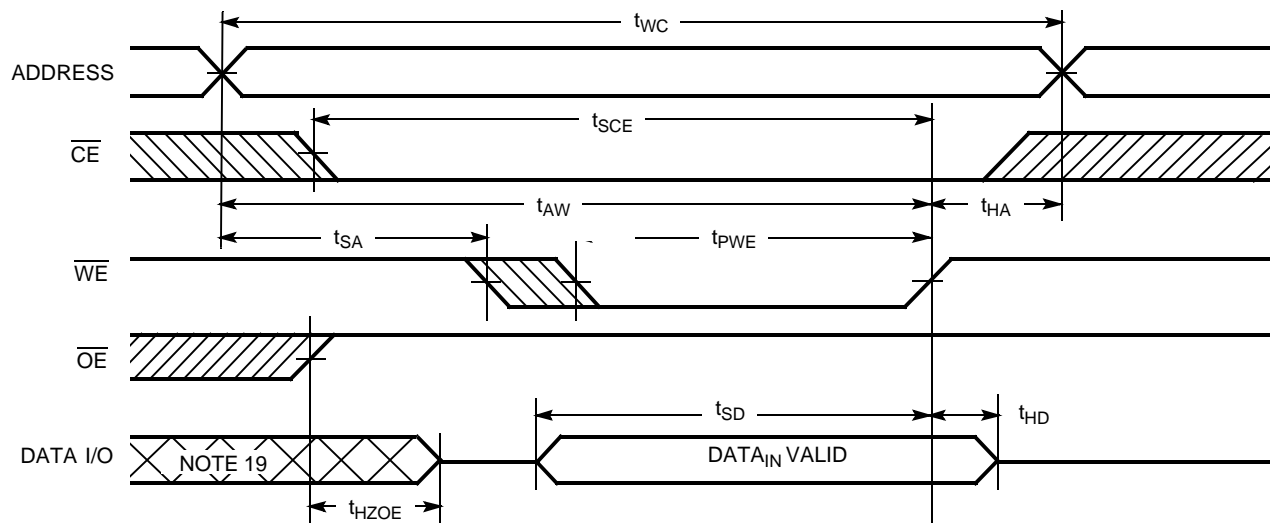


#### Notes:

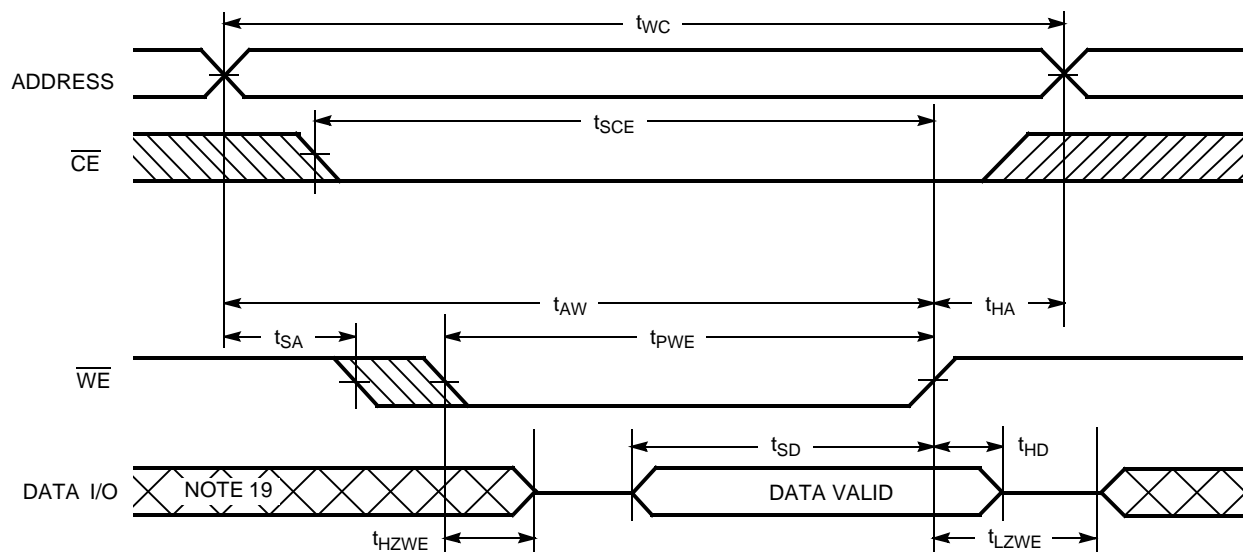
12. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 50 \mu s$  or stable at  $V_{CC(min.)} \geq 50 \mu s$
13. No input may exceed  $V_{CC} + 0.3V$ .
14. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
15.  $\overline{WE}$  is HIGH for Read cycle.
16. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

## Switching Waveforms(continued)

### Write Cycle No. 1 ( $\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)<sup>[17, 18]</sup>



### Write Cycle No. 2 ( $\overline{WE}$ Controlled, $\overline{OE}$ LOW)<sup>[18]</sup>

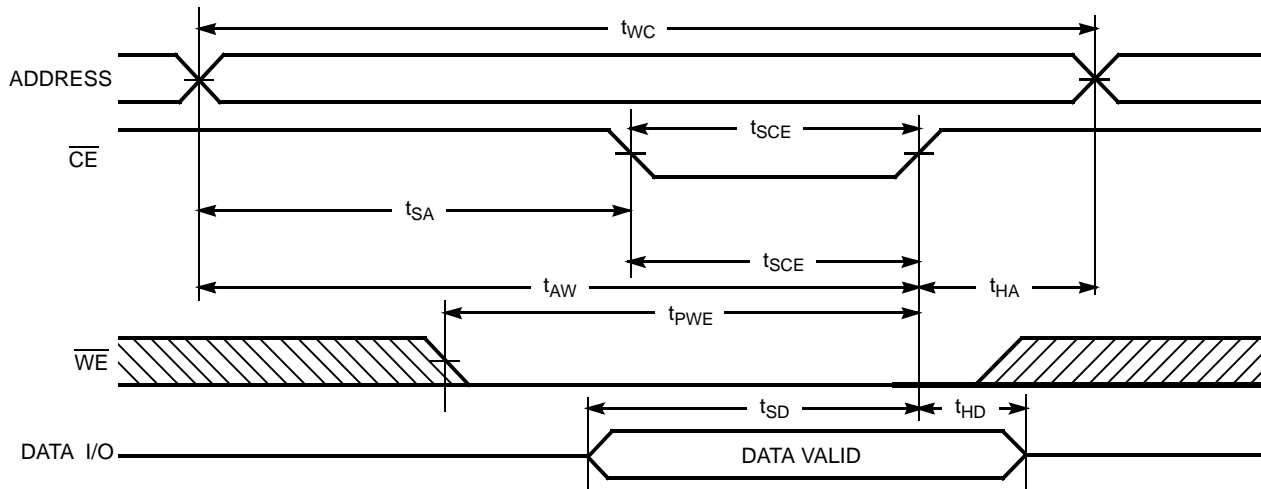


#### Notes:

17. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .
18. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
19. During this period the I/Os are in the output state and input signals should not be applied.

## Switching Waveforms(continued)

**Write Cycle No. 3 ( $\overline{\text{CE}}$  Controlled)<sup>[17, 18]</sup>**



## Truth Table

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O <sub>0</sub> -I/O <sub>7</sub>	Mode	Power
H	X	X	High-Z	Power-down	Standby ( $I_{SB}$ )
L	L	H	Data Out	Read	Active ( $I_{CC}$ )
L	X	L	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High-Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

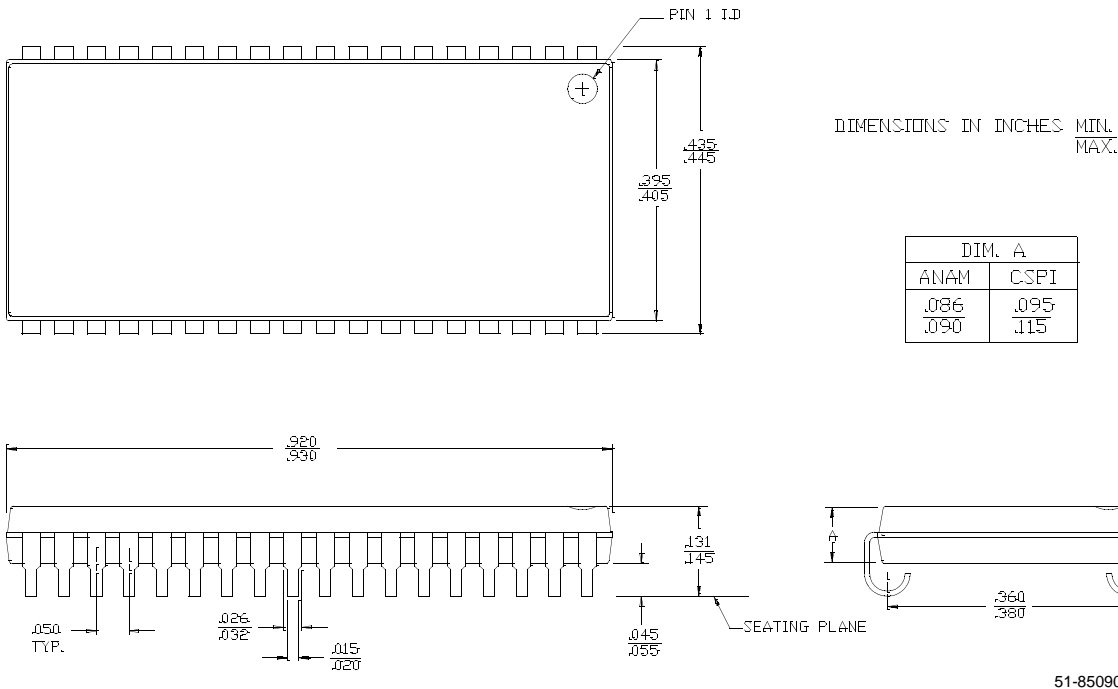
## Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1049DV33-10VXI	51-85090	36-lead (400-Mil) Molded SOJ (Pb-Free)	Industrial
	CY7C1049DV33-10ZSXI	51-85087	44-pin TSOP II (Pb-Free)	
12	CY7C1049DV33-12VXE	51-85090	36-lead (400-Mil) Molded SOJ (Pb-Free)	Automotive
	CY7C1049DV33-12ZSXE	51-85087	44-pin TSOP II (Pb-Free)	

Please contact your local Cypress sales representative for availability of these parts.

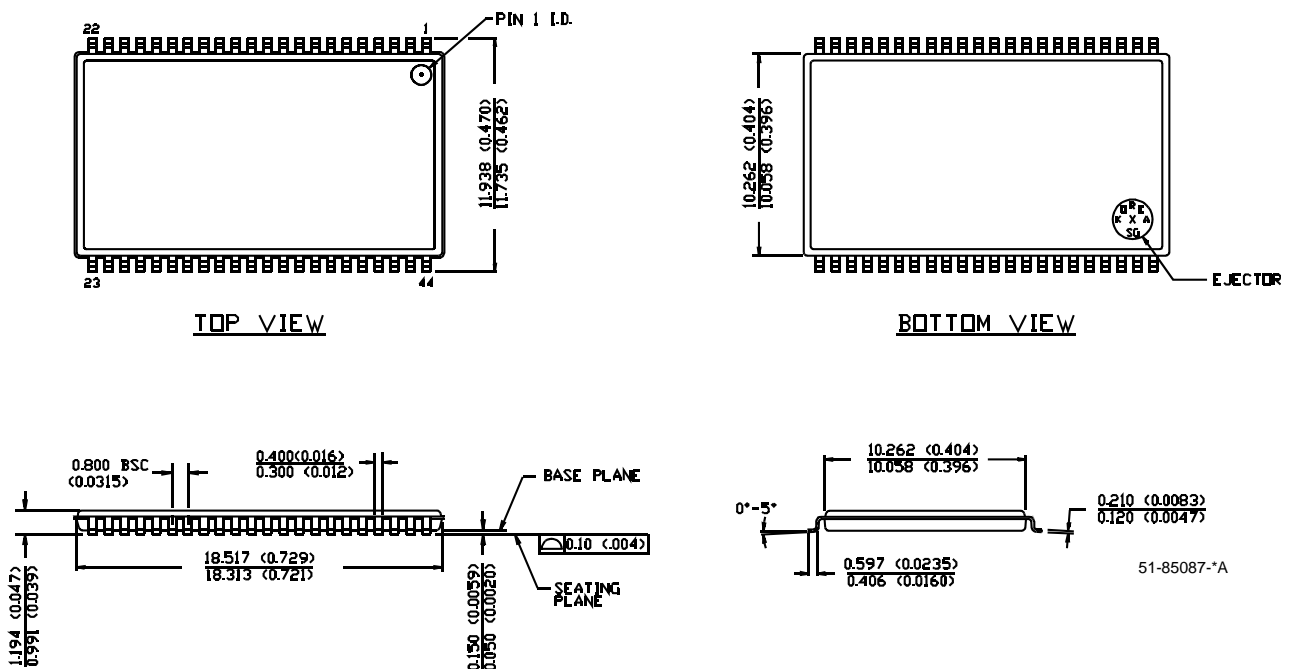
## Package Diagrams

### 36-lead (400-mil) Molded SOJ (51-85090)



### 44-pin TSOP II (51-85087)

DIMENSION IN MM (INCH)  
MAX.  
MIN.



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**Document History Page**

Document Title: CY7C1049DV33 4-Mbit (512K x 8) Static RAM Document Number: 38-05475				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance Data sheet for C9 IPP
*A	233729	See ECN	SYT	1.AC, DC parameters are modified as per EROS(Spec # 01-2165) 2.Pb-free offering in the 'ordering information'
*B	351096	See ECN	PCI	Changed from Advance to Preliminary Removed 20 ns Speed bin Corrected DC voltage (min) value in maximum ratings section from - 0.5 to - 0.3V Redefined I <sub>CC</sub> values for Com'I and Ind'I temperature ranges I <sub>CC</sub> (Com'I): Changed from 100, 80 and 67 mA to 90, 80 and 75 mA for 8, 10 and 12ns speed bins respectively I <sub>CC</sub> (Ind'I): Changed from 80 and 67 mA to 90 and 85 mA for 10 and 12ns speed bins respectively Added V <sub>IH(max)</sub> spec in Note# 2 Changed reference voltage level for measurement of Hi-Z parameters from ±500 mV to ±200 mV Added Data Retention Characteristics/Waveform and footnotes 11 and 12 Changed Package Diagram name from 44-pin TSOP II Z44 to 44-pin TSOP II ZS44 Changed part names from Z to ZS in the Ordering Information Table Added 8 ns parts in the Ordering Information Table Added Lead-Free Ordering Information Shaded Ordering Information Table
*C	446328	See ECN	NXR	Converted from Preliminary to Final Removed -8 speed bin Removed Commercial Operating Range product information Added Automotive Operating Range product information Updated Thermal Resistance table Updated footnote #8 on High-Z parameter measurement Replaced Package Name column with Package Diagram in the Ordering Information table