To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

PRELIMINARY
Notice : This is not a final specification.
some parametric limits are subject to change.

M62443SP/FP

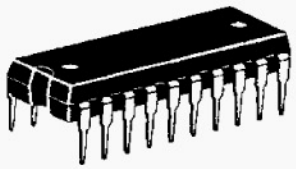
SOUND CONTROLLER

Tone and Volume Controller with 4 Input Selector

OUTLINE

M62443SP/FP is the tone and volume controller with 4 input selector.
This IC can apply the broad application because of low noise and distortion.

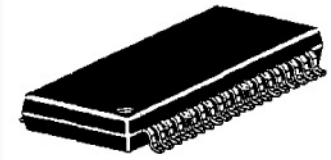
PACKAGE OUTLINE



28 P 4 B (SP)

(28pin Shrink DIP)

PITCH : 1.778mm
SIZE : 19.0mmX6.3mmX3.3mm



28 P 2 W-A(FP)

PITCH : 1.27mm
SIZE :8.4mmX17.5mmX2.0mm

FEATURE

- •TONE(Bass/Treble) control and 1dB step volume control are enabled .
- •Low noise and low distortion .
  V_{NO}= 4.5μVrms, THD=0.1% max
- •4 Input selector.
- •Controlling by 2 Line serial data .

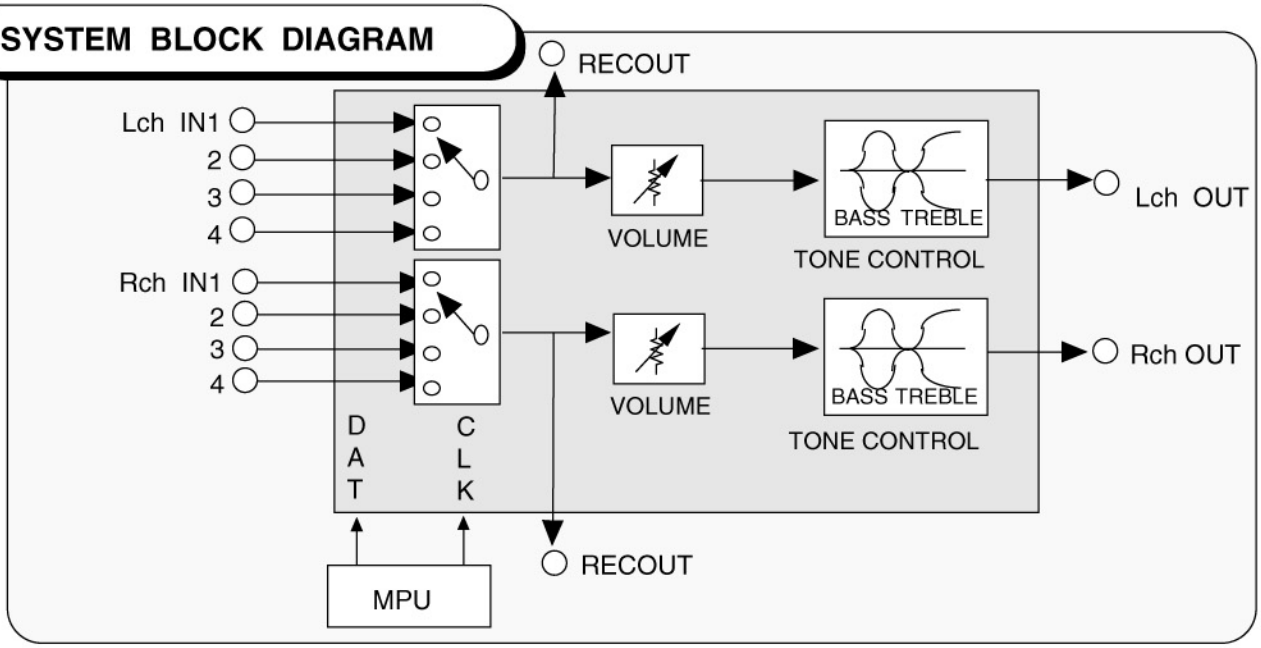
APPLICATION

- •Mini-Stereo , etc

RECOMMENDED OPERATING CONDITION

•Supply voltage range	5.5~9.5V	(analog)	4.5~5.5V	(digital)
•Rated supply voltage	9V	(analog)	5V	(digital)

SYSTEM BLOCK DIAGRAM



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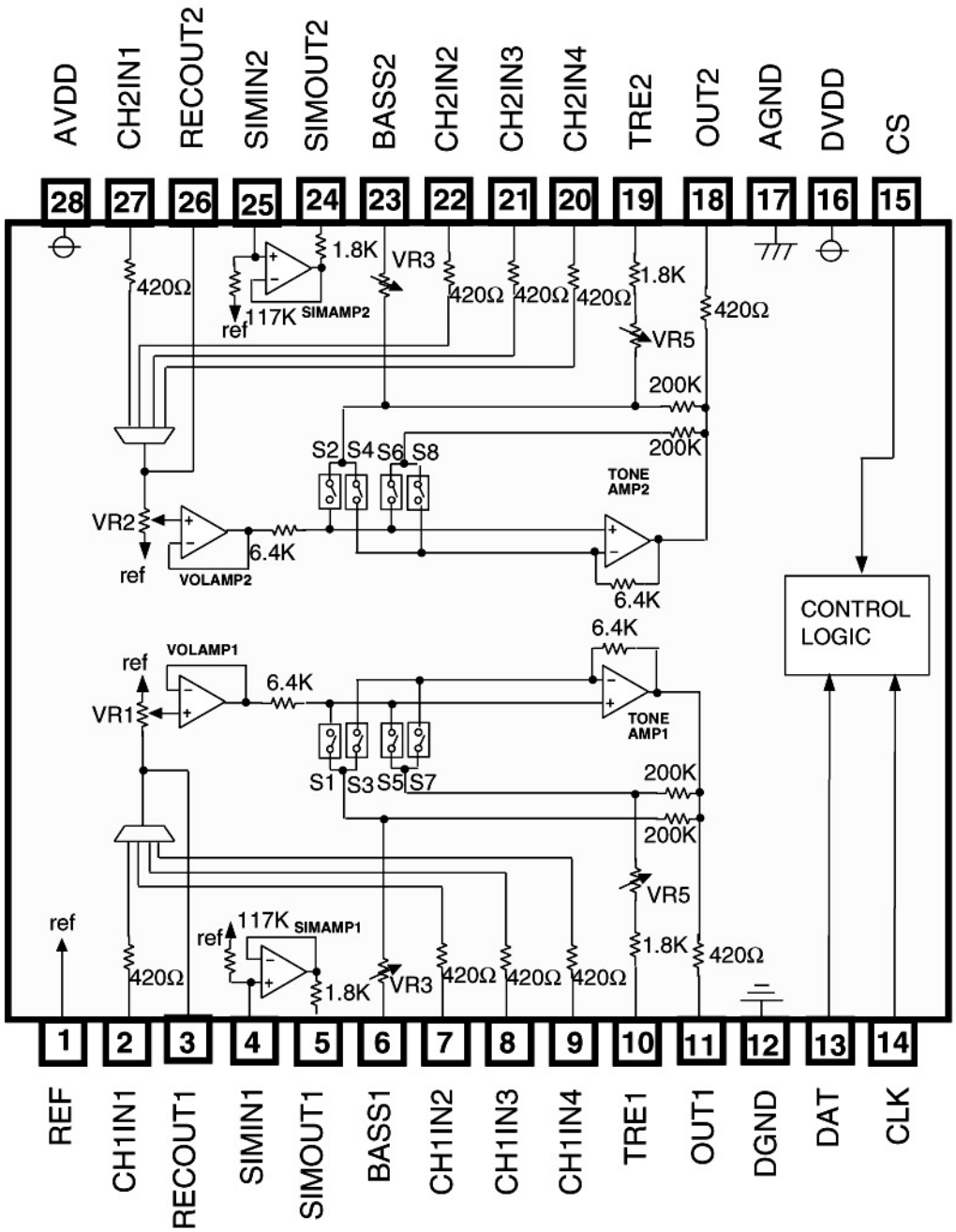
BLOCK DIAGRAM



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PIN DESCRIPTION

PIN No.	PIN NAME	I/O	DESCRIPTION
1	REF	I	Reference voltage terminal for analog
2	CH1 IN1	I	Input terminal (ch1,select 1)
3	RECOUT1	O	Through output terminal (ch1)
4	SIMIN 1	I	Pin for capacitor of simulated inductor 1
5	SIMOUT 1	O	Pin for capacitor of simulated inductor 1
6	BASS1	I	Pin for capacitor of ch1-side bass setting
7	TRE1	I	Pin for capacitor of ch1-side treble setting
8	CH1 IN2	I	Input terminal (ch1,select 2)
9	CH1 IN3	I	Input terminal (ch1,select 3)
10	CH1 IN4	I	Input terminal (ch1,select 4)
11	OUT1	O	Output terminal (ch1)
12	DGND	—	Digital GND
13	DAT	I	I/ O terminal of DATA 2 line bus format
14	CLK	I	Input terminal of CLOCK 2 line bus format
15	CS	I	Chip select terminal
16	DVDD	—	VDD for digital circuit
17	AGND	—	GND for analog circuit
18	OUT2	O	Output terminal (ch2)
19	TRE2	I	Pin for capacitor of ch2-side treble setting
20	CH2 IN4	I	Input terminal (ch2,select 4)
21	CH2 IN3	I	Input terminal (ch2,select 3)
22	CH2 IN2	I	Input terminal (ch2,select 2)
23	BASS2	I	Pin for capacitor of ch2-side bass setting
24	SIMOUT2	O	Pin for capacitor of simulated inductor 2
25	SIMIN 2	I	Pin for capacitor of simulated inductor 2
26	RECOUT2	O	Through output terminal (ch2)
27	CH2 IN1	I	Input terminal (ch2,select 1)
28	AVDD	—	VCC for analog circuit

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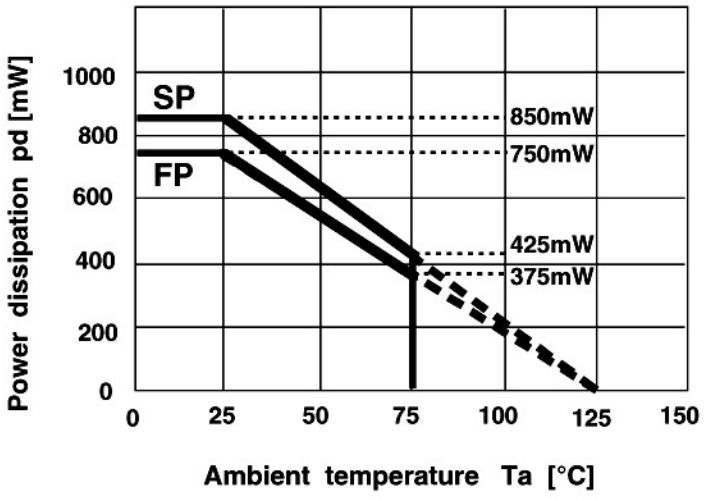
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	CONDITION	LIMITS	UNIT
AVdd	Analog supply voltage		10.0	V
DVdd	Digital supply voltage		7.0	V
Pd	Power dissipation	Ta ≦ 25°C	850(SP) 750(FP)	mW
Kθ	Thermal Derating ratio	Ta > 25°C	8.5(FP) 7.5(FP)	mW/°C
Topr	Operating temperature		-20~+75	°C
Tstg	Storage temperature		-40~+125	°C

Thermal Derating



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RECOMMENDED OPERATING CONDITION

(Ta=25°C unless otherwise noted)

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Analog supply voltage	AVDD		5.5	9.0	9.5	V
Digital supply voltage	DVDD		4.5	5.0	5.5	V
H level input voltage (logic circuit)	VIH		0.7 DVDD	—	VDD	V
L level input voltage (logic circuit)	VIL		0	—	0.3 DVDD	V

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ELECTRIC CHARACTERISTICS

(Ta=25°C, AVDD=9V,DVDD=5V and bass and treble=0dB
unless otherwise noted)

(1) SUPPLY VOLTAGE

ITEM	SYMBOL	CONDITION	LIMIT			UNIT
			Min	typ	Max	
Analog supply current	**Icc**	•AVdd=9.0V •measure terminal=28 pin •no signal input	—	10	20	mA
Digital supply current	**Idd**	•DVdd= 5V •measure terminal=16 pin •no signal input	—	0	2	µA

(2) I / O CHARACTERISTICS

ITEM	SYMBOL	CONDITION	LIMIT			UNIT
			Min	typ	Max	
Maximum input voltage	**VIM**	2,27pin input11,18pin output RL=10KΩ, THD=1%,f=1kHz ATT=-6dB	2.0	3.2	—	Vrms
Output voltage	**Vodc**	11pin,18pin, no signal	4.35	4.5	4.65	V
Gain	**Gv**	Vin=0dBm,FLAT,f=1kHz 2- 11PIN 27-18PIN gain	-2	0	2	dB
Output noise voltage	**Vono**	IHF-A filter no signal Rg=10KΩ 11,18pin	—	4.5	10	µ Vrms
Total harmonic distortion	**THD**	11pin,18pin f=1kHz Vo=0.5Vrms , RL=10KΩ LPF=30kHz	—	0.007	0.1	%
Channel separation	**CT**	RL=10KΩ S:Vin=1Vrms,f=1kHz M:Rg=10kΩ,IHF-A filter	—	-100	-70	dB

PRELIMINARY
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(3) TONE CHARACTERISTICS

ITEM	SYMBOL	CONDITION	LIMIT			UNIT
			Min	typ	Max	
Tone control gain (bass)	Gbassb	f=100Hz	9	12	15	dB
	Gbassc		-15	-12	-9	dB
Tone control gain (treble)	Gtrebb	f=10KHz	9	12	15	dB
	Gtrebc		-15	-12	-9	dB

(4) VOLUME CHARACTERISTICS

ITEM	SYMBOL	CONDITION	LIMIT			UNIT
			Min	typ	Max	
Maximum attenuation	ATTmax	f=1KHz, Vin=0dBm 2pin~11pin 27pin~18pin gain IHF-A-filter	-108	-100	-80	dB
Minimum attenuation	ATTmin		-1.5	0	1.5	dB

PRELIMINARY
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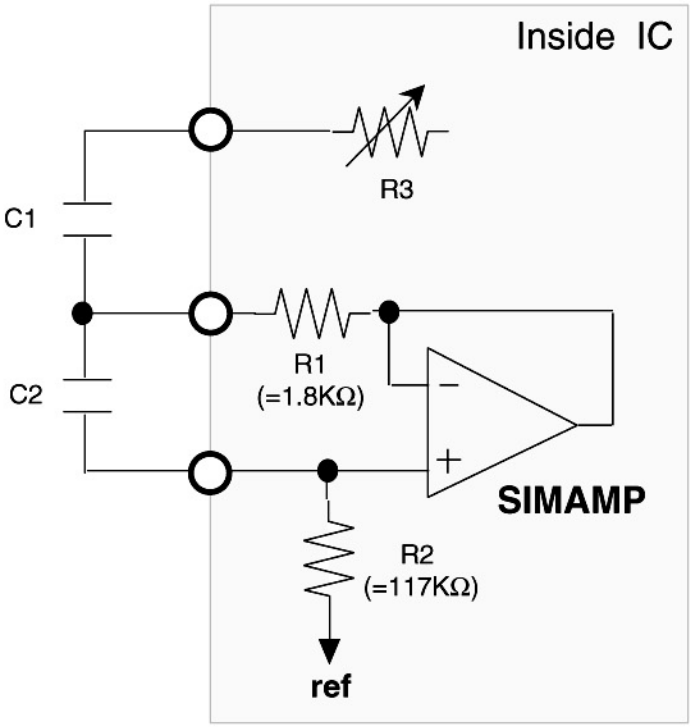
FUNCTION EXPLANATION

(1) EQUIVALENT CIRCUIT OF TONE CONTROL

The resonance circuit is able to construct by using built-in amplifier for simulated inductor. (Shows the constant as follow)



Center frequency

$f0 = 1 / 2\pi\sqrt{C1 \cdot C2 \cdot R1 \cdot R2}$ [Hz]

$Q = \sqrt{(C2 \cdot R2) / (C1 \cdot R1)}$

(EX) BASS band (f≒100Hz)
R1=1.8KΩ , R2=117KΩ
C1=0.47μ , C2=0.022μ

FIG1. The circuit used simulated inductor.

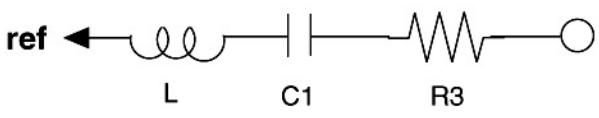


FIG2. The equivalent circuit used L.

FIG1 is equal to FIG2.
The following relation is concluded.

$L = C2 \cdot ER1 \cdot ER2$

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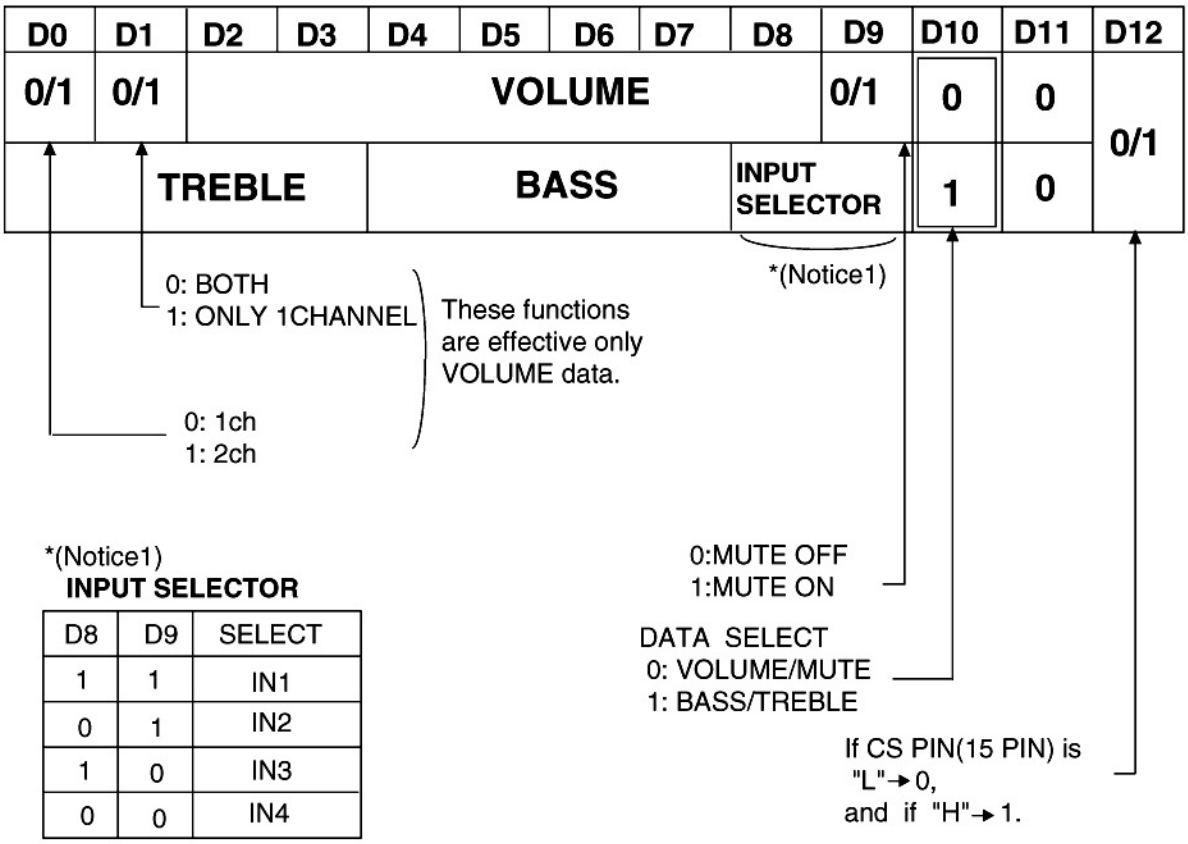
INPUT DATA FORMAT

Input direction



*(Notice1)
INPUT SELECTOR

D8	D9	SELECT
1	1	IN1
0	1	IN2
1	0	IN3
0	0	IN4

PRELIMINARY
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(3) -1: volume control

VOLUME CODE

ATT	D2	D3	D4	D5	D6
0dB	H	L	H	L	H
-4dB	L	L	H	L	H
-8dB	H	H	L	L	H
-12dB	L	H	L	L	H
-16dB	H	L	L	L	H
-20dB	L	L	L	L	H
-24dB	H	H	H	H	L
-28dB	L	H	H	H	L
-32dB	H	L	H	H	L
-36dB	L	L	H	H	L
-40dB	H	H	L	H	L
-44dB	L	H	L	H	L
-48dB	H	L	L	H	L
-52dB	L	L	L	H	L
-56dB	H	H	H	L	L
-60dB	L	H	H	L	L
-64dB	H	L	H	L	L
-68dB	L	L	H	L	L
-72dB	H	H	L	L	L
-76dB	L	H	L	L	L
-80dB	H	L	L	L	L
-∞dB	L	L	L	L	L

ATT	D7	D8
0dB	H	H
-1dB	L	H
-2dB	H	L
-3dB	L	L

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(4) -2 : tone level control

TONE CODE

	BASS				TREBLE			
	D7	D6	D5	D4	D3	D2	D1	D0
12dB	L	H	H	L	L	H	H	L
10dB	L	H	L	H	L	H	L	H
8dB	L	H	L	L	L	H	L	L
6dB	L	L	H	H	L	L	H	H
4dB	L	L	H	L	L	L	H	L
2dB	L	L	L	H	L	L	L	H
0dB	L	L	L	L	L	L	L	L
-2dB	H	L	L	H	H	L	L	H
-4dB	H	L	H	L	H	L	H	L
-6dB	H	L	H	H	H	L	H	H
-8dB	H	H	L	L	H	H	L	L
-10dB	H	H	L	H	H	H	L	H
-12dB	H	H	H	L	H	H	H	L

NOT USED HHHH
LHHH
HLLL

(4) -3 : MUTE CONTROL

On condition D9=1,MUTE can be set up.
In MUTE,VOLUME LEVEL is set up
VOL=-∞automatically.

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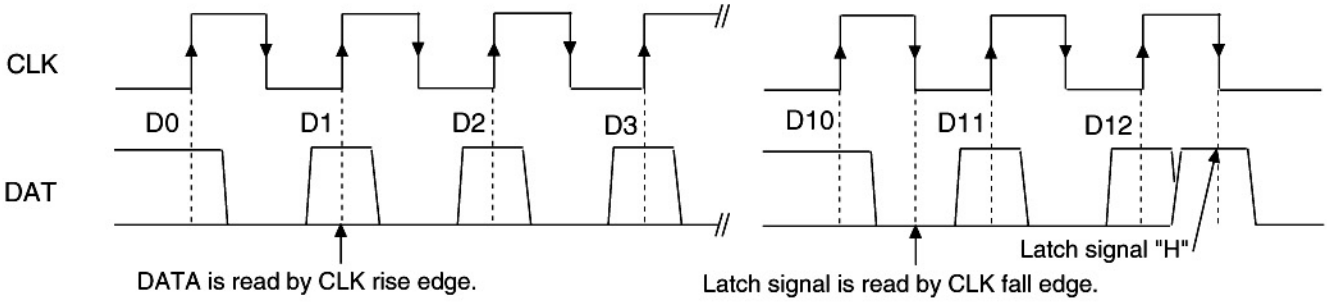
DATA and CLOCK



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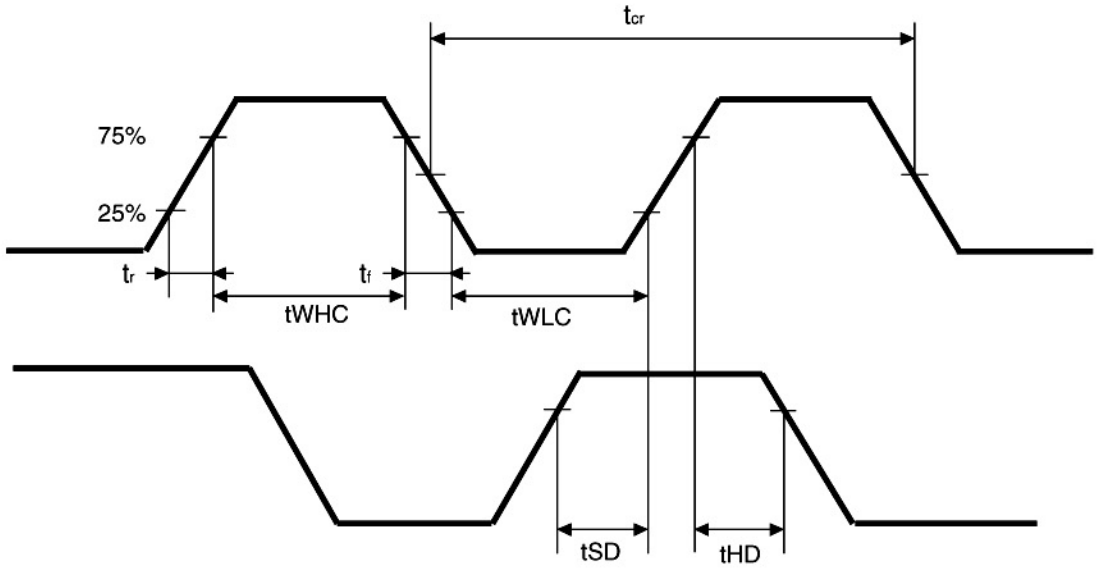
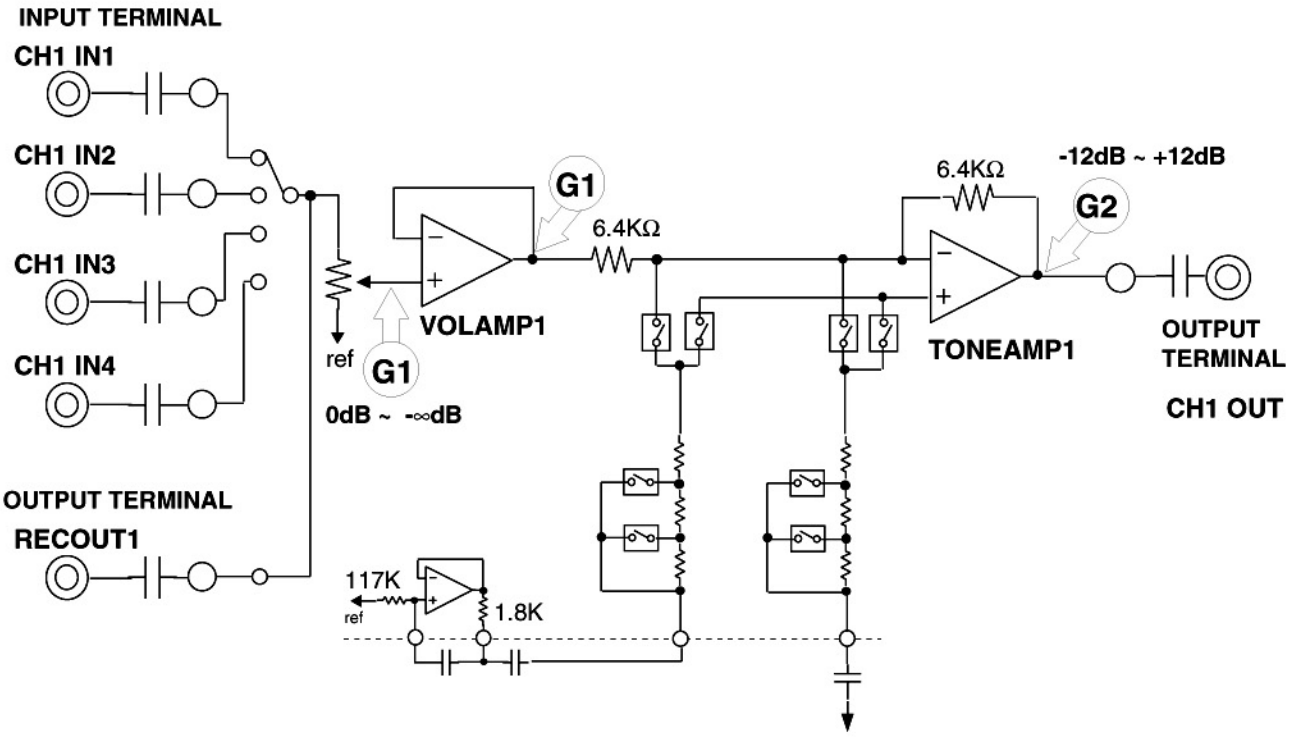
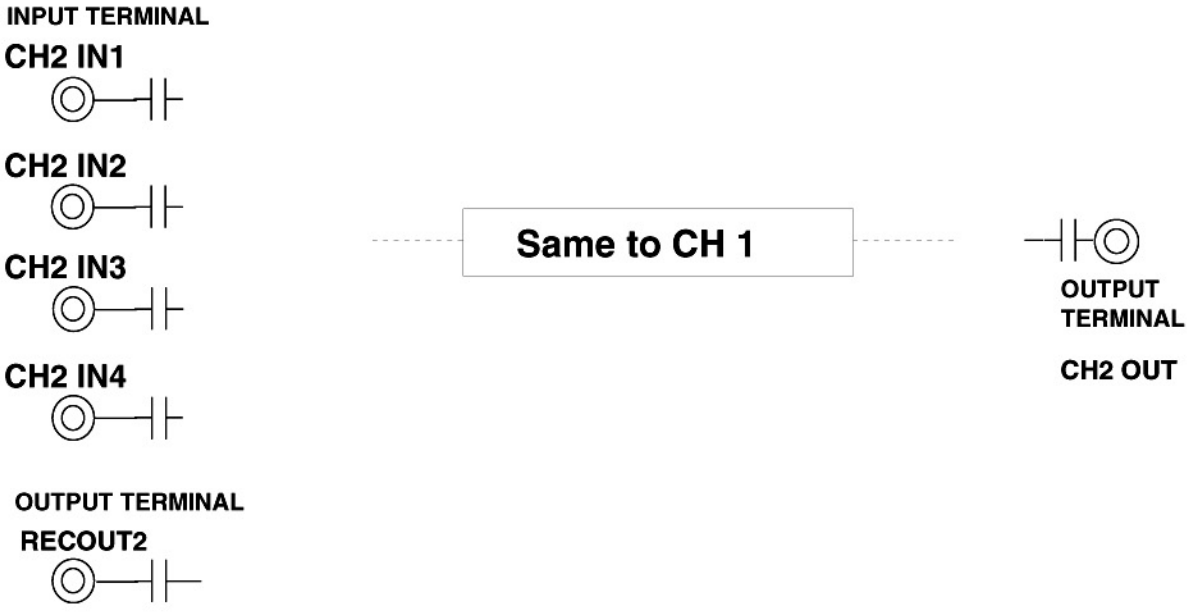
BUS LINE TIMING SPECIFICATION



Parameter	Symbol	MIN	MAX	Units
CLK clock frequency	t_{cr}	4	-	µs
The HIGH period of the clock	tWHC	1.6	-	µs
The LOW period of the clock	tWLC	1.6	-	µs
Rise time of CLK line	t_r	-	0.4	µs
Fall time of CLK line	t_f	-	0.4	µs
Set -up time DATA	tSD	0.8	-	µs
Hold time DATA	tHD	0.8	-	µs

LEVEL DIAGRAM





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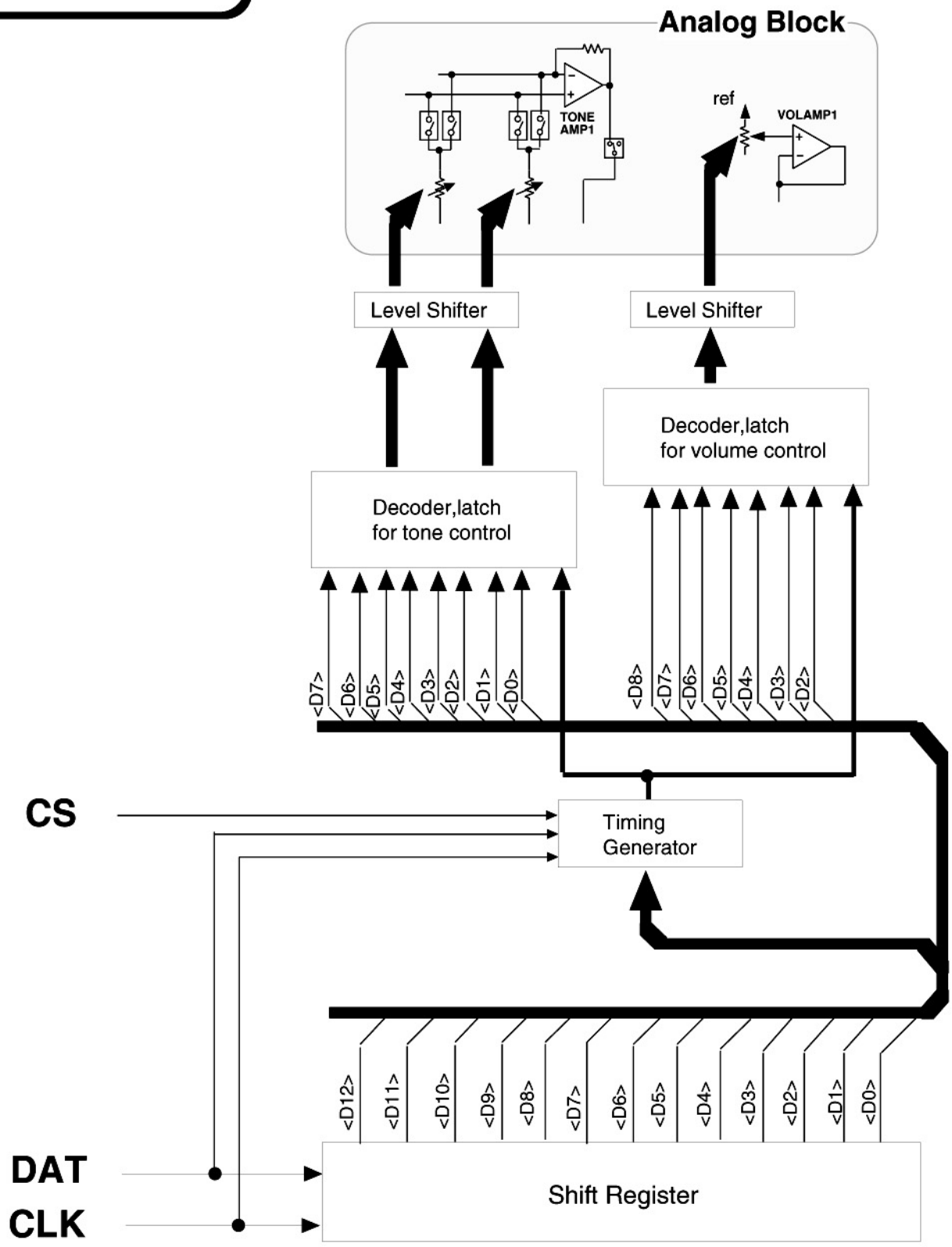
LOGIC CIRCUIT



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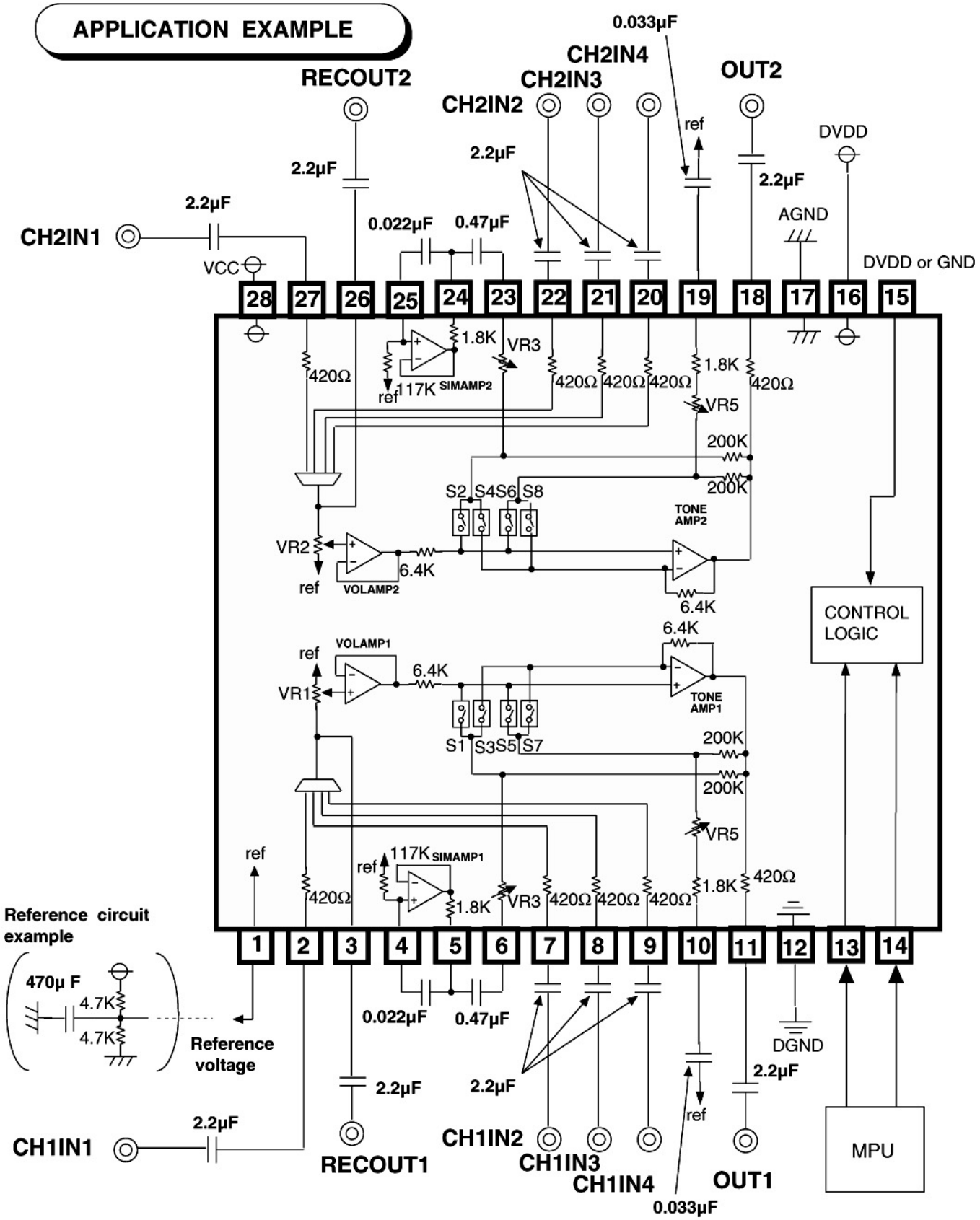
APPLICATION EXAMPLE