ADM6999/X

Single Chip Ethernet Switch Controller

ADM6999/X

Communications

Never stop thinking.

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ADM6999/X, Single Chip Ethernet Switch Controller

Revision History: 2005-11-25, Rev. 1.32

Previous Version:

Page/Date	Subjects (major changes since last revision)
2005-08	Rev. 0.1, First Infineon-ADMtek Co Ltd version
2002-09	Rev. 1.0, Remove Preliminary word
2002-12	Rev. 1.1, Modify error word. Modify Pin 98 as P8_Enable
2003-04	Rev. 1.2, Modify MII RXER as NC or GND pin, Modify MII RXCLK & TXCLK timing requirement, Remove LEDEN pin to NC, Modify ADM6999/X VLAN example error EEPROM Register 0x11h
2003-05	Rev. 1.3, Change RTX to 1K 1% at A2 version chip
2004-04	Rev. 1.31, Updated Infineon-ADMtek Co Ltd logo
2004-10	Rev. 1.32, Changed to the new Infineon format
2005-11	Minor change. Included Green package information

Trademarks

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1 Introduction

1.1 General Description

The ADM6999/X is a high performance, low cost, highly integration (Controller, PHY and Memory) eight-port 10/100 Mbps TX/FX plus one 10/100 MII/RMII/7wires port Ethernet switch controller with all ports supporting 10/100 Mbps Full/Half duplex. The ADM6999/X is intended for applications to stand alone bridged for low cost SOHO market such as 8port, 8+1FX. The ADM6999X is the environmentally friendly “green” package version.

ADM6999/X provides most advance function such as: **802.1p (Q.O.S.), 802.1q (VLAN), Port MAC Address Locking, Management, Port Status, TP Auto-MDIX, 25M Crystal & Extra ninth Port (RMII/MII/GPSI)** function to meet customer request on Switch demand.

The built-in 768K SRAM used for packet buffer and address learning table is divided into 512 bytes/block to achieve the optimized memory utilization through complicated link list on packets with various lengths.

ADM6999/X also supports priority features by Port-Base, VLAN and IP TOS field checking. It’s easy for users to set different priority mode in individual port, through a small low-cost micro controller to initialize or on-the-fly to configure. Each output port supports two queues in the way of fixed N: 1 fairness queuing to fit the bandwidth demand on various types of packet such as Voice, Video and data. 802.1Q, Tag/Untag, and up to 32 groups of VLAN are supported.

An intelligent address recognition algorithm makes ADM6999/X to recognize up to 2048 different MAC addresses and enables filtering and forwarding at full wire speed.

Port MAC address Locking function is also supported by ADM6999/X to use on Building Internet access to prevent multiple users share one port traffic.

1.2 Features

Main features:

- Supports eight 10M/100M auto-detect Half/Full duplex switch ports with TX/FX interfaces and one universal port. The ninth port can be configured to be a GPSI, MII, RMII interface
- Built-in 12Kx64 SRAM
- Supports 2048 MAC addresses table
- Supports two queues for QoS
- Supports priority features by Port-Based, 802.1p VLAN & IP TOS of packets
- Supports Store & Forward architecture and performs forwarding and filtering at non-blocking full wire speed
- Supports buffer allocation with 512 bytes per block
- Supports Aging function Enable/Disable
- Supports per port Single/Dual color mode & Serial LED mode with Power On auto diagnostic
- Supports 802.3x Flow Control pause packet for Full Duplex in case buffer is full
- Supports Back Pressure function for Half Duplex operation in case buffer is full
- Supports packet length up to 1522 bytes
- Broadcast Storming Filter function
- Supports 802.1Q VLAN. Up to 16/32 VLAN groups are implemented by the user defined four or five bits of VLAN ID
- Supports MAC-clone feature
- Supports TP interface **Auto MDIX** function for auto TX/RX swap by strapping-pin
- Easy Management 32bits smart counter for per port RX/TX byte/packet count, error count and collision count
- Supports PHY status output for management system
- 25M Crystal only for the whole system. Output 10M/25M/50M for different interfaces
- 128 QFP package with 0.18um technology. 1.8 V/3.3 V power supply

1.3 Applications

ADM6999/X in 128-pin PQFP:

- SOHO 8-port switch
- 8-port switch + Router with CPU interface.
- 16/24 Dual-speed hub application enabled by “Hubbing-switch©” mode by 100Mbps-backbone bandwidth.

2 Input and Output Signals

This chapter describes Pin Diagram and Pin Description.

2.1 Pin Diagram

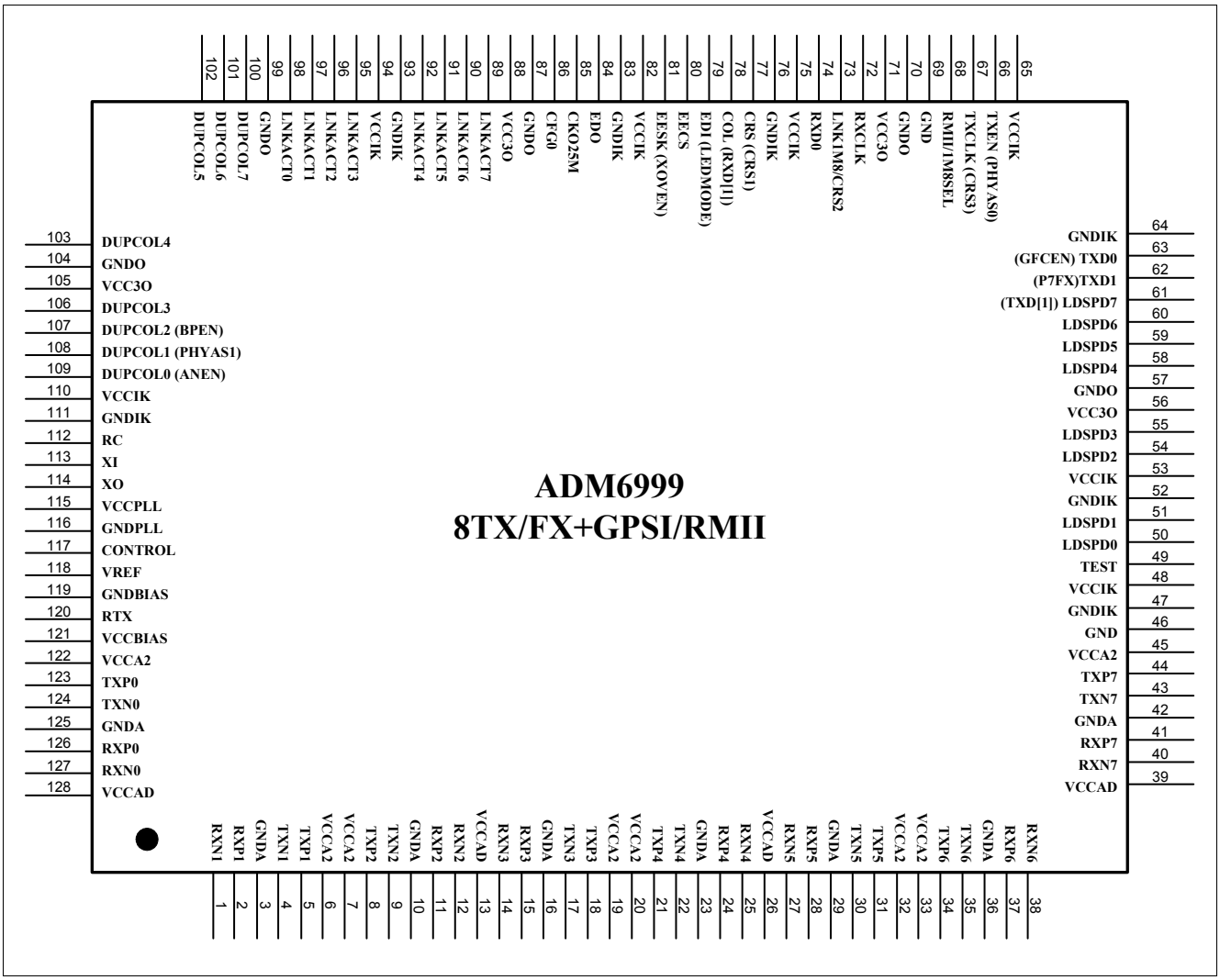


Figure 1 8 TP/FX PORT + 1 GPSI/RMII PORT 128 Pin Diagram

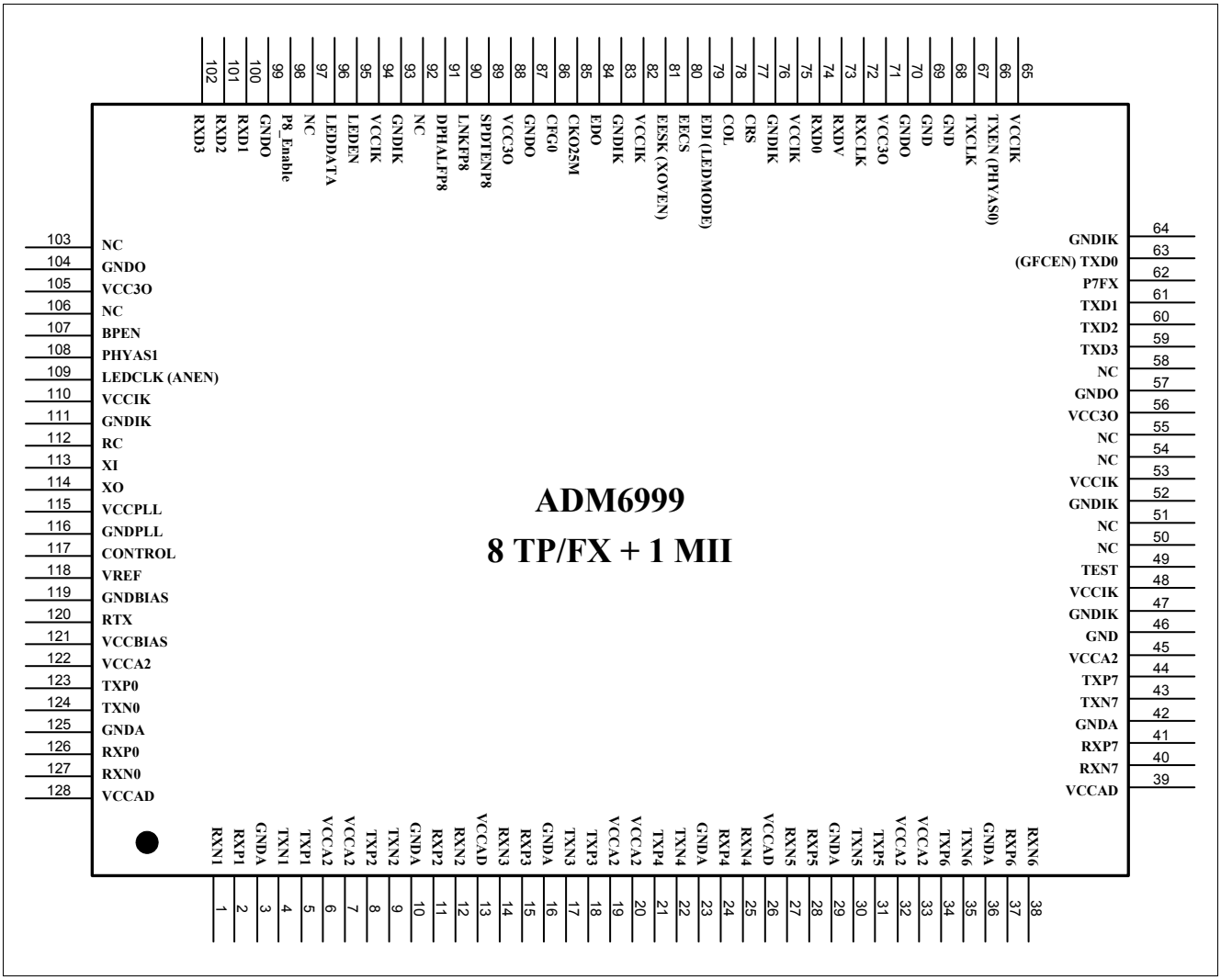


Figure 2 8 TP/FX PORT + 1 MII PORT 128 Pin Diagram

2.2 Pin Description

Table 1 ADM6999/X-128 PINS(8 TP + GPSI/RMII)[1)2)]

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Twisted Pair Interface				
126	RXP0	I/O	Analog	**Twisted Pair Receive Input Positive**
2	RXP1			
11	RXP2			
15	RXP3			
24	RXP4			
28	RXP5			
37	RXP6			
41	RXP7			
127	RXN0	I/O	Analog	**Twisted Pair Receive Input Negative**
1	RXN1			
12	RXN2			
14	RXN3			
25	RXN4			
27	RXN5			
38	RXN6			
40	RXN7			
123	TXP0	I/O	Analog	**Twisted Pair Transmit Output Positive**
5	TXP1			
8	TXP2			
18	TXP3			
21	TXP4			
31	TXP5			
34	TXP6			
44	TXP7			
124	TXN0	I/O	Analog	**Twisted Pair Transmit Output Negative**
4	TXN1			
9	TXN2			
17	TXN3			
22	TXN4			
30	TXN5			
35	TXN6			
43	TXN7			
Ninth Port (GPSI/RMII) Interfaces, 11 pins[3)]				

Table 1 ADM6999/X-128 PINS(8 TP + GPSI/RMII)[1)2)] (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
68	RMII/GPSISEL	I	PD	**Strapping pin to set 9th port for GPSI or RMII (half-duplex mode)** On power-on-reset, latched as setting for 9th port: 0_B , to set as GPSI (GPSI) mode 1_B , to set as RMII half-duplex mode.Internal pull down
63	TXD	I/O	8mA PU	**GPSI: GPSI Mode** GPSI Transmit data synchronous to the rising edge of TXCLK.
	TXD0	I/O	8mA PU	**RMII: RMII Mode** RMII transmit data 0 synchronous to the rising edge of 50M REFCLK.
	GFCEN	I/O	8mA PU	**Setting** Setting Internally Pull Up. At power-on-reset, latched as Flow control setting 0_B , to disable flow-control 1_B , to enable flow-control (default)
62	P7FX	I/O	8mA PD	**Setting Port7 FX/TX Mode select** Internal pull down. 0_B , Port7 as TX port 1_B , Port7 as FX port
	TXD1	I/O	8mA PD	**RMII: RMII Mode** Transmittes data 1. To be used at RMII half-duplex mode for 9th port only.
74	RXD	I		**GPSI: GPSI Mode** Receives data at GPSI mode.
	RXD0	I		**RMII: RXD0 Mode** Receives data 0 at RMII mode.
73	LNKGPSI	I	PD	**GPSI: GPSI Mode** Links status input at GPSI mode.
	CRS2	I	PD	**RMII: RMII Mode** Carrier Sense 2 input control for Hubbing Switch.
78	COL	I	PD	**GPSI: GPSI Mode** GPSI Port Collision input.
	RXD1	I	PD	**RMII: RMII Mode** RMII receives data1.
77	CRS	I	PD	**GPSI: GPSI Mode** GSPI Port Carrier Sense
	CRS1	I	PD	**RMII: RMII Mode** Carrier Sense 1 input control for Hubbing Switch.
72	RXCLK	I		**GPSI mode** GPSI Port Receive Clock Input.
67	TXCLK	I		**GPSI: GPSI mode** GPSI Port Transmit clock Input.
	CRS3	I		**RMII: RMII mode** Carrier Sense 3 input control for Hubbing Switch.

Table 1 ADM6999/X-128 PINS(8 TP + GPSI/RMII)[1)2)] (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
66	TXEN	I/O	8mA PD	**GPSI: GPSI Mode** Data transmit enable.
	TXEN	I/O	8mA PD	**RMII: RMII Mode** Data transmit enable.
	PHYAS0	I/O	8mA PD	**Setting** PHYAS1 (108), PHYAS0 (66). Power on reset value PHYAS0 combines with PHYAS1(DUPCOL1). Internal pull down. PHYAS1/S0 E2PRM 00 Master 01 Slave0 1x Slave1 Master: ADM6999/X will read 93C66/46 EEPROM first Bank (00h ~ 27h). Slave 0: ADM6999/X will read 93C66 EEPROM second Bank (40h ~ 67h). Slave 1: ADM6999/X will read 93C66 EEPROM third Bank (80h ~ a7h).
LED Interface				
89	LNKACT7	O	8mA	**LINK/Activity LED[7:0]** Active low. 0_B , indicates link okay on cable, but no activity and signals on idle stage. "blinking" indicates link activity on cable. 1_B , indicates no link activity on cable
90	LNKACT6			
91	LNKACT5			
92	LNKACT4			
95	LNKACT3			
96	LNKACT2			
97	LNKACT1			
98	LNKACT0			
100	DUPCOL7	O	8mA	**Duplex/Collision LED[7:3]** Active low. 0_B , for full-duplex indication 1_B , for half-duplex and "blinking" for collision indication
101	DUPCOL6			
102	DUPCOL5			
103	DUPCOL4			
106	DUPCOL3			
107	DUPCOL2	I/O	8mA PU	**PORT2 Duplex Collision LED** Port2 Duplex/Collision LED. Active low.
	BPEN	I/O	8mA PU	**Setting** BPEN: Back Pressure power on setting pin. Internal pull up. 0_B , Disables all port half-duplex backpressure 1_B , Enables all port half-duplex backpressure

Table 1 ADM6999/X-128 PINS(8 TP + GPSI/RMII)[1)2)] (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
108	DUPCOL1	I/O	8mA PD	**Port1 Duplex Collision LED** If pulled low, then acted as active high to drive 0_B , for half-duplex and "blinking" for collision indication 1_B , for full-duplex indication
	DUPCOL1	I/O	8mA PD	**Port1 Duplex Collision LED** If pulled high, then acted as active low to drive 0_B , for full-duplex indication 1_B , for half-duplex and "blinking" for collision indication
	PHYAS1	I/O	8mA PD	**Setting** PHYAS1: Combines with **PHYAS0** (pin 66) to set chip physical address.
109	DUPCOL0	I/O	8mA PU	**Duplex/Collision LED 0** Port0 Duplex/Collision LED. Active high or low depends on setting.
	ANEN	I/O	8mA PU	**Setting** ANEN: On power-on-reset, latched as Auto Negotiation capability for all ports. 0_B , to disable Auto Negotiation 1_B , to enable Auto Negotiation (defaulted by pulled up internally)
61	LDSPD7	O	8mA	**Speed LED[7:0]** Used to indicate corresponding port's speed status. 0_B , for 100Mbit/s 1_B , for 10Mbit/s
60	LDSPD6			
59	LDSPD5			
58	LDSPD4			
55	LDSPD3			
54	LDSPD2			
51	LDSPD1			
50	LDSPD0			
EEPROM/Management Interface				
84	EEDO	I	TTL PU	**EEPROM Data Output** Serial data input from EEPROM. This pin is internally pull-up.
80	EECS	O	4mA PD	**EEPROM Chip Select** This pin is an active high chip enable for EEPROM. When RC is low, it will be Tristate. This pin is internally pull-down.
81	EECK	I/O	4mA PD	**Serial Clock** This pin is clock source for EEPROM.
	XOVEN	I/O	4mA PD	**Setting** XOVEN: This pin is internally pull-down. On power-on-reset, latched as P7~0 Auto MDIX enable or not. Suggests externally pull up to enable Auto MDIX for all ports. 0_B , to disable MDIX (defaulted) 1_B , to enable MDIX

Table 1 ADM6999/X-128 PINS(8 TP + GPSI/RMII)[1)2)] (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
79	EEDI	O	4mA PD	**EEPROM Serial Data Input** This pin is the output for serial data transfer.
	LEDMODE	O	4mAPD	**Setting** LEDMODE: On power-on-reset, latched as Dual Color mode or not. This pin is internal pull-down. 0_B , to set Single color mode for LED 1_B , to set Dual Color mode for LED
Misc.				
85	CKO25M	O	8mA	10M Clock Output For GPSI port configuration (RMII/GPSISEL/CFG0 = 0/1), 50M output for RMII (RMII/GPSISEL/CFG0 = 1/1).
117	Control	O		**FET Control Signal** The pin is used to control FET for 3.3 V to 1.8 V regulator. Add 0.01 µf capacitor to GND.
120	RTX	Analog		**TX Resistor** Add 1.1K %1(A1), 1K %1 (A2) resister to GND.
118	VREF	Analog		**Analog Reference Voltage**
112	RC	I	SCHE	**RC Input for Power On reset** Reset input pin
113	XI	I	Analog	**25M Crystal Input** 25M Crystal Input. Variation is limited to +/- 50ppm.
114	XO	O	Analog	**25M Crystal Output** When connected to oscillator, this pin should be unconnected.
49	TEST	I	TTL	**TEST Value** At normal application connects to GND.
Chip Configuration, 2 pins				
86	CFG0	I	TTL PU	**Configuration of Pin-out. Internally Pull high.** RMII/GPSISEL: CFG0, Description 0: 1, 8 port and 1 GPSI (GPSI) interface 1: 1, 8 port and 1 RMII for Hubbing Switch
Power/Ground				
3, 10, 16, 23, 29, 36, 42, 125	GNDA	I		**Ground Used by AD Block**
6, 7, 19, 20, 32, 33, 45, 122	VCCA2	I		**1.8 V, Power Used by TX Line Driver**
13, 26, 39, 128	VCCAD	I		**3.3 V, Power Used by AD Block**
119	GNDBIAS	I		**Ground Used by Bias Block**
121	VCCBIAS	I		**3.3 V, Power Used by Bias Block**

Table 1 ADM6999/X-128 PINS(8 TP + GPSI/RMII)[1)2)] (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
116	GNDPLL	I		**Ground used by PLL**
115	VCCPLL	I		**1.8 V, Power used by PLL**
47, 52, 64, 76, 83, 93, 111	GNDIK	I		**Ground Used by Digital Core**
48, 53, 65, 75, 82, 94, 110	VCCIK	I		**1.8 V, Power Used by Digital Core**
46, 57, 70, 87, 99, 104	GNDO	I		**Ground Used by Digital Pad**
56, 71, 88, 105	VCC3O	I		**3.3 V, Power Used by Digital Pad**
69	GND	I	TTL	**Scan Enable** This pin will be used as the scan enable input for testing. Connects to GND at normal application.

1) Do not swap TP port +- signal. It may cause link fail when link partner does not support Auto Polarity function.

2) I: Input, O: Output, I/O: Bi-directional, OD: Open drain, SCHE: Schmitt-Trigger, PD: internal pull-down, PU: internal pull-up

3) RMII only runs at Half-duplex mode.

Table 2 ADM6999/X-128 PINS (8 TP + 1 MII)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Twisted Pair Interface				
126	RXP0	I/O	Analog	**Twisted Pair Receive Input Positive**
2	RXP1			
11	RXP2			
15	RXP3			
24	RXP4			
28	RXP5			
37	RXP6			
41	RXP7			
127	RXN0	I/O	Analog	**Twisted Pair Receive Input Negative**
1	RXN1			
12	RXN2			
14	RXN3			
25	RXN4			
27	RXN5			
38	RXN6			
40	RXN7			
123	TXP0	I/O	Analog	**Twisted Pair Transmit Output Positive**
5	TXP1			
8	TXP2			
18	TXP3			
21	TXP4			
31	TXP5			
34	TXP6			
44	TXP7			
124	TXN0	I/O	Analog	**Twisted Pair Transmit Output Negative**
4	TXN1			
9	TXN2			
17	TXN3			
22	TXN4			
30	TXN5			
35	TXN6			
43	TXN7			
8th Port (MII) Interfaces, 20 pins				

Table 2 ADM6999/X-128 PINS (8 TP + 1 MII) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
63	TXD[0]	I/O	8mA PU	**MII transmit data 0** Acts as MII transmit data TXD0 Synchronous to the rising edge of TXCLK
	GFCEN	I/O	8mA PU	**Setting** GFCEN: Global Flow Control Enable. At power-on-reset, latched as Full Duplex Flow control setting. 0_B , to disable flow-control. internally Pull-up. 1_B , to enable flow-control (default)
59	TXD3	O	8mA	**MII Transmit Data bit 3~1** Synchronous to the rising edge of TXCLK. These pins act as MII TXD[3:1].
60	TXD2			
61	TXD1			
62	P7FX	I/O	8mA PD	**Setting Port7 FX/TX mode select** Internal pull down. 0_B , Port7 as TX port 1_B , Port7 as FX port
66	TXEN	I/O	8mA PD	**MII Transmit Enable**
	PHYAS0	I/O	8mA PD	**Setting** PHYAS0: Chip physical address on loading EEPROM data. Internal pull down. Power on reset value PHYAS0 combines with PHYAS1. PHYAS1 PHYAS0 0 0 Master(93C46) If there is no EEPROM then user must use 93C66 timing to write chip's registers. If user puts 93C46 with correct Signature then user writes chip register by 93C46 timing. If user puts 93C66 then data put in Bank0. User can write chip register by 93C66 timing. User must assert one SK cycle when CS at idle stage and chip's internal register is being writing.
108	PHYAS1	I/O	8mA PD	**Chip physical address1** Check pin 66.
102	RXD3	I	PD	**MII port receive data 3~0** These pins act as MII RXD[3:0]. Synchronous to the rising edge of RXCLK. Internal pull down.
101	RXD2			
100	RXD1			
74	RXD0			
73	RXDV	I	PD	**MII receive data valid** Internal pull down.
68	GND	I	PD	**GND or NC**
78	COL	I	PD	**MII Port Collision input** Internal pull down.
77	CRS	I	PD	**MII Port Carrier Sense** Internal pull down.
72	RXCLK	I		**MII Port Receive Clock Input**

Table 2 ADM6999/X-128 PINS (8 TP + 1 MII) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
67	TXCLK	I		**MII Port Transmit Clock Input**
98	P8_Enable	I		**MII Port Enable. Should add pull high 1K resister to 3.3 V.**
91	DHALFP8	I	PD	**MII Port Hardware Duplex input pin.** Low: Full Duplex High: Half Duplex Internal pull down.
90	LNKFP8	I	PD	**MII Port Hardware Link input pin** Low: Link OK High: Link Off Internal pull down.
89	SPDTNP8	I	PD	**MII Port Hardware Speed input pin** Low: 100M High: 10M Internal pull down.
LED Interface				
95	NC	O	8mA	**Keep NC**
96	LEDDATA	I/O	8mA PD	**Serial LED Data**
109	LEDCLK	I/O	8mA PU	**Serial LED Clock**
	ANEN	I/O	8mA PU	**Setting** ANEN: On power-on-reset, latched as Auto Negotiation capability for all ports. 0_B , to disable Auto Negotiation 1_B , to enable Auto Negotiation (defaulted by pulled up internally)
EEPROM/Management Interface				
84	EEDO	I	TTL PU	**EEPROM Data Output** Serial data input from EEPROM. This pin is internally pull-up.
80	EECS	O	4mA PD	**EEPROM Chip Select** This pin is active high chip enable for EEPROM. When RC is low, it will be Tristate. This pin is internally pull-down.
81	EECK	I/O	4mA PD	**Serial Clock** This pin is clock source for EEPROM.
	XOVEN	I/O	4mA PD	**Setting** XOVEN: This pin is internally pull-down. On power-on-reset, latched as P7~0 Auto MDIX enable or not. Suggests externally pull up to enable MDIX for all ports. 0_B , to disable MDIX (defaulted) 1_B , to enable MDIX

Table 2 ADM6999/X-128 PINS (8 TP + 1 MII) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
79	EEDI	O	4mA PD	**EEPROM Serial Data Input** This pin is output for serial data transfer. When RC is low, it will be tristate.
	LEDMODE	O	4mA PD	**Setting** LEDMODE: This pin is internal pull-down. On power-on-reset, latched as Dual Color mode or not. 0_B , to set Single color mode for LED 1_B , to set Dual Color mode for LED.
Misc., 8 pins				
85	CKO25M	O	8mA	**25M Clock Output For MII port**
117	Control	O		**FET Control Signal** The pin is used to control FET for 3.3 V to 1.8 V regulator.
120	RTX	Analog		**TX Resistor** Add 1.1K %1 resister to GND
118	VREF	Analog		**Analog Reference Voltage**
112	RC	I	SCHE	**RC Input for Power On reset** Reset input pin.
113	XI	I	Analog	**25M Crystal Input** 25M Crystal Input. Variation is limited to +/- 50ppm.
114	XO	O	Analog	**25M Crystal Output** When connected to oscillator, this pin should be left unconnected.
49	TEST	I	TTL	**TEST Value** At normal application connects to GND.
Switch function				
107	BPEN	I/O	8mA	At power-on-reset, latched as Back Pressure setting 0_B , to disable Back Pressure 1_B , to enable Back-Pressure (defaulted)
Chip configuration				
86	CFG0	I	TTL PU	Must Connected to GND.
Power/Ground				
3, 10, 16, 23, 29, 36, 42, 125	GNDA	I		**Ground Used by AD Block**
6, 7, 19, 20, 32, 33, 45, 122	VCCA2	I		**1.8 V, Power Used by TX Line Driver**
13, 26, 39, 128	VCCAD	I		**3.3 V, Power Used by AD Block**
119	GNDBIAS	I		**Ground Used by Bias Block**

Table 2 ADM6999/X-128 PINS (8 TP + 1 MII) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
121	VCCBIAS	I		**3.3 V, Power Used by Bias Block**
116	GNDPLL	I		**Ground used by PLL**
115	VCCPLL	I		**1.8 V, Power used by PLL**
47, 52, 64, 76, 83, 93, 111	GNDIK	I		**Ground Used by Digital Core**
48, 53, 65, 75, 82, 94, 110	VCCIK	I		**1.8 V, Power Used by Digital Core**
46, 57, 70, 87, 99, 104	GNDO	I		**Ground Used by Digital Pad**
56, 71, 88, 105	VCC3O	I		**3.3 V, Power Used by Digital Pad**
69	GND	I	TTL	**Scan Enable** This pin will be used as the scan enable input for testing. Connects to GND at normal application.
NC Pin				
50, 51, 54, 55, 58, 92, 97, 103, 106	NC			**Not Connected**

3 Descriptions

This chapter provides Functional Description, 10/100M PHY Block Description, Memory Block Description, Switch Functional Description, EEPROM Content and EEPROM Access Description.

3.1 Functional Description

The ADM6999/X integrates eight 100Base-X physical sub-layer (PHY), 100Base-TX physical medium dependent (PMD) transceivers, eight complete 10Base-T modules, 8 port 100/10 switch controller and one 10/100 MAC and memory into a single chip for both 10Mbits/s and 100Mbits/s Ethernet switch operation. It also supports 100Base-FX operation through external fiber-optic transceivers. The device is capable of operating in either Full Duplex mode or Half-Duplex mode in 10Mbits/s and 100Mbits/s. Operational modes can be selected by hardware configuration pins, software settings of management registers, or determined by the on-chip auto negotiation logic.

The ADM6999/X consists of three major blocks:

- 10/100M PHY Block
- Switch Controller Block
- Built-in 12Kx64 SSRAM

3.2 10/100M PHY Block Description

The 100Base-X section of the device implements the following functional blocks:

- 100Base-X physical coding sub-layer (PCS)
- 100Base-X physical medium attachment (PMA)
- Twisted-pair transceiver (PMD)

The 100Base-X and 10Base-T sections share the following functional blocks:

- Clock synthesizer module
- MII Registers
- IEEE 802.3u auto negotiation

3.2.1 100Base-X Module

The ADM6999/X implements 100Base-X compliant PCS and PMA and 100Base-TX compliant TP-PMD as illustrated in Figure 2. Bypass options for each of the major functional blocks within the 100Base-X PCS provides flexibility for various applications. 100Mbits/s PHY loop back is included for diagnostic purpose.

3.2.2 100Base-X Receiver

The 100Base-X receiver consists of functional blocks required to recover and condition the 125Mbits/s receive data stream. The ADM6999/X implements the 100Base-X receiving state machine diagram as given in ANSI/IEEE Standard 802.3u, Clause 24. The 125Mbits/s receive data stream may originate from the on-chip twisted-pair transceiver in a 100Base-TX application. Alternatively, the receive data stream may be generated by an external optical receiver as in a 100Base-FX application.

The receiver block consists of the following functional sub-blocks:

- A/D Converter
- Adaptive Equalizer and timing recovery module
- NRZI/NRZ and serial/parallel decoder
- De-scrambler
- Symbol alignment block
- Symbol Decoder
- Collision Detect Block
- Carrier sense Block
- Stream decoder block

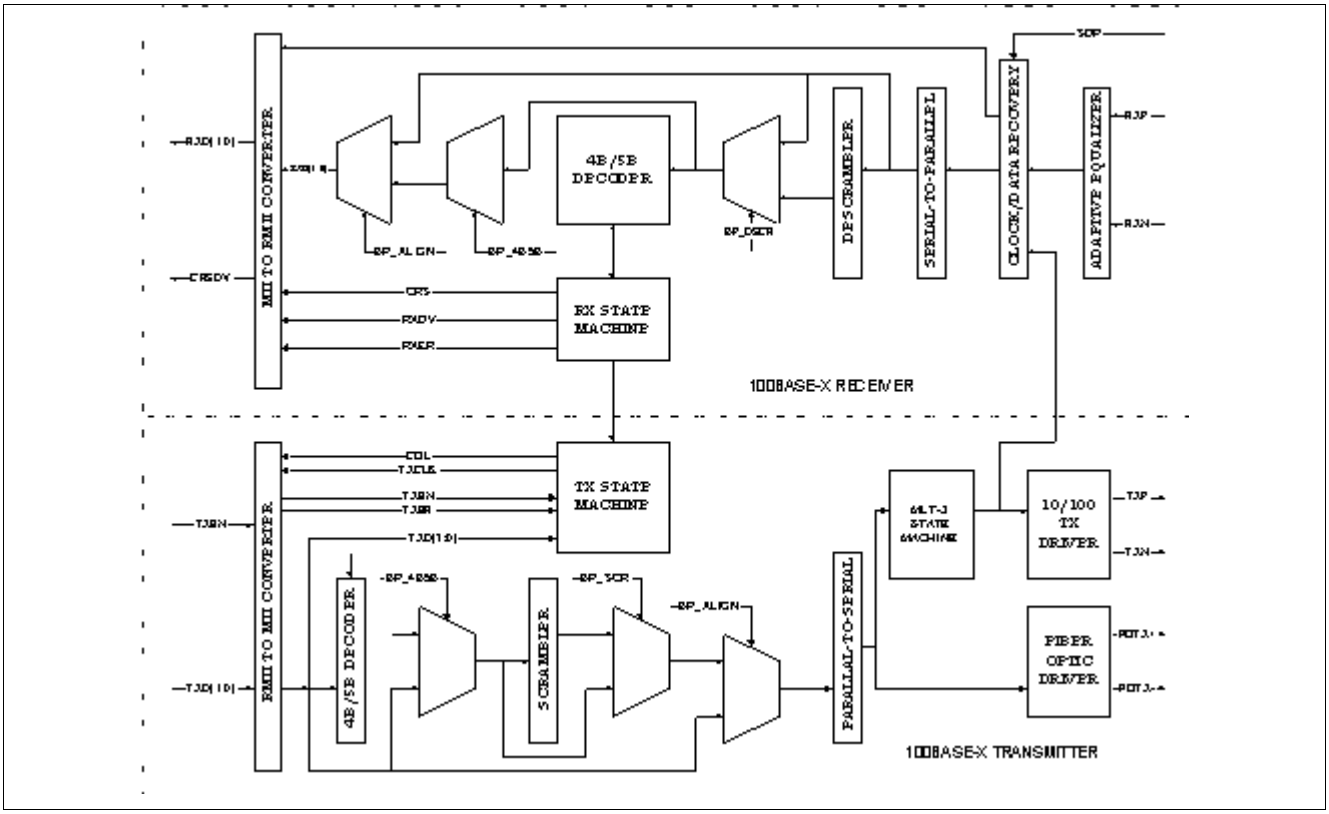


Figure 3 100Base-X Transmitter

3.2.2.1 A/D Converter

High performance A/D converter with 125 MHz sampling rate converts signals received on RXP/RXN pins to 6 bits data streams; besides it possess auto-gain-control capability that will further improve receive performance especially under long cable or harsh detrimental signal integrity. Due to high pass characteristic on transformer, built in base-line-wander correcting circuit will cancel it out and restore its DC level.

3.2.2.2 Adaptive Equalizer and Timing Recovery Module

All digital design is especial immune from noise environments and achieves better correlation between production and system testing. Baud rate Adaptive Equalizer/Timing Recovery compensates line loss induced from twisted pair and tracks far end clock at 125M samples per second. Adaptive Equalizer implemented with Feed forward and Decision Feedback techniques meet the requirement of BER less than 10-12 for transmission on CAT5 twisted pair cable ranging from 0 to 120 meters.

3.2.2.3 NRZI/NRZ and Serial/Parallel Decoder

The recovered data is converted from NRZI to NRZ. The data is not necessarily aligned to 4B/5B code group's boundary.

3.2.2.4 Data De-scrambling

The de-scrambler acquires synchronization with the data stream by recognizing idle bursts of 40 or more bits and locking its deciphering Linear Feedback Shift Register (LFSR) to the state of the scrambling LFSR. Upon achieving synchronization, the incoming data is XORed by the deciphering LFSR and de-scrambled.

In order to maintain synchronization, the de-scrambler continuously monitors the validity of the unscrambled data that it generates. To ensure this, a link state monitor and a hold timer are used to constantly monitor the

synchronization status. Upon synchronization of the de-scrambler the hold timer starts a 722 us countdown. Upon detection of sufficient idle symbols within the 722 us period, the hold timer will reset and begin a new countdown. This monitoring operation will continue indefinitely given a properly operating network connection with good signal integrity. If the link state monitor does not recognize sufficient unscrambled idle symbols within 722 us period, the de-scrambler will be forced out of the current state of synchronization and reset in order to re-acquire synchronization.

3.2.2.5 Symbol Alignment

The symbol alignment circuit in the ADM6999/X determines code word alignment by recognizing the /J/K delimiter pair. This circuit operates on unaligned data from the de-scrambler. Once the /J/K symbol pair (11000 10001) is detected, subsequent data is aligned on a fixed boundary.

3.2.2.6 Symbol Decoding

The symbol decoder functions as a look-up table that translates incoming 5B symbols into 4B nibbles as shown in Table 1. The symbol decoder first detects the /J/K symbol pair preceded by idle symbols and replaces the symbol with MAC preamble. All subsequent 5B symbols are converted to the corresponding 4B nibbles for the duration of the entire packet. This conversion ceases upon the detection of the /T/R symbol pair denoting the end of stream delimiter (ESD). The translated data is presented on the internal RXD[3:0] signal lines with RXD[0] represents the least significant bit of the translated nibble.

3.2.2.7 Valid Data Signal

The valid data signal (RXDV) indicates that recovered and decoded nibbles are being presented on the internal RXD[3:0] synchronous to receive clock, RXCLK. RXDV is asserted when the first nibble of translated /J/K is ready for transfer over the internal MII. It remains active until either the /T/R delimiter is recognized, link test indicates failure, or no signal is detected. On any of these conditions, RXDV is de-asserted.

3.2.2.8 Receive Errors

The RXER signal is used to communicate receiver error conditions. While the receiver is in a state of holding RXDV asserted, the RXER will be asserted for each code word that does not map to a valid code-group.

3.2.2.9 100Base-X Link Monitor

The 100Base-X link monitor function allows the receiver to ensure that reliable data is being received. Without reliable data reception, the link monitor will halt both transmit and receive operations until such time that a valid link is detected.

The ADM6999/X performs the link integrity test as outlined in IEEE 100Base-X (Clause 24) link monitor state diagram. The link status is multiplexed with 10Mbits/s link status to form the reportable link status bit in serial management register 1h, and driven to the LNKACT pin.

When persistent signal energy is detected on the network, the logic moves into a Link-Ready state after approximately 500 us, and waits for an enable signal from the auto negotiation module. When received, the link-up state is entered, and the transmission and reception logic blocks become active. Should the auto negotiation be disabled, the link integrity logic moves immediately to the link-up state after entering the link-ready state.

3.2.2.10 Carrier Sense

Carrier sense (CRS) for 100Mbits/s operation is asserted upon the detection of two noncontiguous zeros occurring within any 10-bit boundary of the received data stream.

The carrier sense function is independent of symbol alignment. In switch mode, CRS is asserted during either packet transmission or reception. For repeater mode, CRS is asserted only during packet reception. When the idle

symbol pair is detected in the received data stream, CRS is de-asserted. In repeater mode, CRS is only asserted due to receive activity. CRS is intended to encapsulate RXDV.

3.2.2.11 Bad SSD Detection

A bad start of stream delimiter (Bad SSD) is an error condition that occurs in the 100Base-X receiver if carrier is detected (CRS asserted) and a valid /J/K set of code-group (SSD) is not received.

If this condition is detected, then the ADM6999/X will assert RXER and present RXD[3:0] = 1110 to the internal MII for the cycles hat correspond to received 5B code-groups until at least two idle code-groups are detected. Once at least two idle code groups are detected, RXER and CRS become de-asserted.

3.2.2.12 Far-End Fault

Auto negotiation provides a mechanism for transferring information from the Local Station to the link Partner that a remote fault has occurred for 100Base-TX. As auto negotiation is not currently specified for operation over fiber, the far end fault indication function (FEFI) provides this capability for 100Base-FX applications.

A remote fault is an error in the link that one station can detect while the other cannot. An example of this is a disconnected wire at a station's transmitter. This station will be receiving valid data and detect that the link is good via the link integrity monitor, but will not be able to detect that its transmission is not propagating to the other station.

A 100Base-FX station that detects such a remote fault may modify its transmitted idle stream from all ones to a group of 84 ones followed by a single 0. This is referred to as the FEFI idle pattern.

3.2.3

3.2.3 100Base-TX Transceiver

ADM6999/X implements a TP-PMD compliant transceiver for 100Base-TX operation. The differential transmit driver is shared by the 10Base-T and 100Base-TX subsystems. This arrangement results in one device that uses the same external magnetic for both the 10Base-T and the 100Base-TX transmission with simple RC component connections. The individually wave-shaped 10Base-T and 100Base-TX transmit signals are multiplexed in the transmission output driver selection.

3.2.3.1 Transmit Drivers

The ADM6999/X 100Base-TX transmission driver implements MLT-3 translation and wave-shaping functions. The rise/fall time of the output signal is closely controlled to conform to the target range specified in the ANSI TP-PMD standard.

3.2.3.2 Twisted-Pair Receiver

For 100Base-TX operation, the incoming signal is detected by the on-chip twisted-pair receiver that consists of a differential line receiver, an adaptive equalizer and a base-line wander compensation circuit.

The ADM6999/X uses an adaptive equalizer that changes filter frequency response in according to cable length. The cable length is estimated based on the incoming signal strength. The equalizer tunes itself automatically for any cable length to compensate for the amplitude and phase distortions incurred from the cable.

3.2.4 10Base-T Module

The 10Base-T Transceiver Module is IEEE 802.3 compliant. It includes the receiver, transmitter, collision, heartbeat, loop back, jabber, wave shaper, and link integrity functions, as defined in the standard. Figure 3 provides an overview for the 10Base-T module.

The ADM6999/X 10Base-T module is comprised of the following functional blocks:

- Manchester encoder and decoder
- Collision detector
- Link test function
- Transmit driver and receiver
- Serial and parallel interface
- Jabber and SQE test functions
- Polarity detection and correction

3.2.4.1 Operation Modes

The ADM6999/X 10Base-T module is capable of operating in either half-duplex mode or full-duplex mode. In half-duplex mode, the ADM6999/X functions as an IEEE 802.3 compliant transceiver with fully integrated filtering. The COL signal is asserted during collisions or jabber events, and the CRS signal is asserted during transmit and receive. In full duplex mode the ADM6999/X can simultaneously transmit and receive data.

3.2.4.2 Manchester Encoder/Decoder

Data encoding and transmission begins when the transmission enable input (TXEN) goes high and continues as long as the transceiver is in good link state. Transmission ends when the transmission enable input goes low. The last transition occurs at the center of the bit cell if the last bit is a 1, or at the boundary of the bit cell if the last bit is 0.

Decoding is accomplished by a differential input receiver circuit and a phase-locked loop that separates the Manchester-encoded data stream into clock signals and NRZ data. The decoder detects the end of a frame when no more mid bit transitions are detected. Within one and half bit times after the last bit, carrier sense is de-asserted.

3.2.4.3 Transmit Driver and Receiver

The ADM6999/X integrates all the required signal conditioning functions in its 10Base-T block such that external filters are not required. Only one isolation transformer and impedance matching resistors are needed for the 10Base-T transmit and receive interface. The internal transmit filtering ensures that all the harmonics in the transmission signal are attenuated properly.

3.2.4.4 Smart Squelch

The smart squelch circuit is responsible for determining when valid data is present on the differential receive. The ADM6999/X implements an intelligent receive squelch on the RXP/RXN differential inputs to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10Base-T standard) to determine the validity of data on the twisted-pair inputs.

The signal at the start of the packet is checked by the analog squelch circuit and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly, the opposite squelch level must then be exceeded within 150ns. Finally, the signal must exceed the original squelch level within an additional 150ns to ensure that the input waveform will not be rejected.

Only after all these conditions have been satisfied a control signal will be generated to indicate to the remainder of the circuitry that valid data is present.

Valid data is considered to be present until the squelch level has not been generated for a time longer than 200 ns, indicating end of packet. Once good data has been detected, the squelch levels are reduced to minimize the effect of noise, causing premature end-of-packet detection. The receive squelch threshold level can be lowered for use in longer cable applications. This is achieved by setting bit 10 of register address 11h.

3.2.5 Carrier Sense

Carrier Sense (CRS) is asserted due to receive activity once valid data is detected via the smart squelch function. For 10 Mbits/s half duplex operation, CRS is asserted during either packet transmission or reception. For 10 Mbits/s full duplex and repeater mode operations, the CRS is asserted only due to receive activity.

3.2.6 Jabber Function

The jabber function monitors the ADM6999/X output and disables the transmitter if it attempts to transmit a longer sized packet than legal. If TXEN is high for greater than 24ms, the 10Base-T transmitter will be disabled. Once disabled by the jabber function, the transmitter stays disabled for the entire time that the TXEN signal is asserted. This signal has to be de-asserted for approximately 256 ms (The un-jab time) before the jabber function re-enables the transmit outputs. The jabber function can be disabled by programming bit 4 of register address 10h to high.

3.2.7 Link Test Function

A link pulse is used to check the integrity of the connection with the remote end. If valid link pulses are not received, the link detector disables the 10Base-T twisted-pair transmitter, receiver, and collision detection functions.

The link pulse generator produces pulses as defined in IEEE 802.3 10Base-T standard. Each link pulse is nominally 100ns in duration and is transmitted every 16 ms, in the absence of transmit data.

3.2.8 Automatic Link Polarity Detection

ADM6999/X's 10Base-T transceiver module incorporates an "automatic link polarity detection circuit". The inverted polarity is determined when seven consecutive link pulses of inverted polarity or three consecutive packets are received with inverted end-of-packet pulses. If the input polarity is reversed, the error condition will be automatically corrected and reported in bit 5 of register 10h.

3.2.9 Clock Synthesizer

The ADM6999/X implements a clock synthesizer that generates all the reference clocks needed from a single external frequency source. The clock source must be a TTL level signal at 25 MHz +/- 50ppm

3.2.10 Auto Negotiation

The Auto Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices. Fast Link Pulse (FLP) Bursts provide the signaling used to communicate auto negotiation abilities between two devices at each end of a link segment. For further details regarding auto negotiation, refer to Clause 28 of the IEEE 802.3u specification. The ADM6999/X supports four different Ethernet protocols, so the inclusion of auto negotiation ensures that the highest performance protocol will be selected based on the ability of the link partner.

Highest priority relative to the following list.

1. 100Base-TX full duplex (highest priority)
2. 100Base-TX half duplex
3. 10Base-T full duplex
4. 10Base-T half duplex (lowest priority)

3.3 Memory Block Description

ADM6999/X build in 768K bits memory inside. Memory buffer is divided in two blocks. One is MAC addressing table and another one is data buffer.

MAC address Learning Table size is 2048 entry with each entry occupies eight bytes length. These eight bytes data include 6 bytes source address, VLAN information, Port information and Aging counter.

Data buffer is divided to 512 bytes/block. ADM6999/X buffer management is per port fixed block number and all port share one global buffer. This architecture can get better memory utilization and network balance on different speed and duplex test condition.

Received packets will be separated in several 512 bytes/block and chain together. If the packet size is more than 512 bytes then ADM6999/X will chain two or more blocks to store receiving packet.

3.4 Switch Functional Description

The ADM6999/X uses a “store & forward” switching approach for the following reasons:

Store & forward switches allow switching between different speed media (e.g. 10BaseX and 100BaseX). Such switches require the large elastic buffer especially bridging between a server on a 100Mbps network and clients on a 10Mbps segment.

Store & forward switches improve overall network performance by acting as a “network cache”

Store & forward switches prevent the forwarding of corrupted packets by the frame check sequence (FCS) before forwarding to the destination port.

3.4.1 Basic Operation

The ADM6999/X receives incoming packets from one of its ports, searches in the Address Table for the Destination MAC Address and then forwards the packet to the other port within same VLAN group, if appropriate. If the destination address is not found in the address table, the ADM6999/X treats the packet as a broadcast packet and forwards the packet to the other ports which are in the same VLAN group.

The ADM6999/X automatically learns the port number of attached network devices by examining the Source MAC Address of all incoming packets at wire speed. If the Source Address is not found in the Address Table, the device adds it to the table.

3.4.1.1 Address Learning

The ADM6999/X uses a hash algorithm to learn the MAC address and can learn up to 2K MAC addresses. An Address is stored in the Address Table. The ADM6999/X searches for the Source Address (SA) of an incoming packet in the Address Table and acts as below:

If the SA was not found in the Address Table (a new address), the ADM6999/X waits until the end of the packet (non-error packet) and updates the Address Table. If the SA was found in the Address Table, then aging value of each corresponding entry will be reset to 0.

When the DA is PAUSE command, then the learning process will be disabled automatically by ADM6999/X.

3.4.1.2 Address Recognition and Packet Forwarding

The ADM6999/X forwards the incoming packets between bridged ports according to the Destination Address (DA) as below. All the packet forwarding will check VLAN first. Forwarding port must be the same VLAN with source port.

1. If the DA is an UNICAST address and the address was found in the Address Table, the ADM6999/X will check the port number and acts as follows:
   a) If the port number is equal to the port on which the packet was received, the packet is discarded.
   b) If the port number is different, the packet is forwarded across the bridge.
2. If the DA is an UNICAST address and the address was not found, the ADM6999/X treats it as a multicast packet and forwards across the bridge.
3. If the DA is a Multicast address, the packet is forwarded across the bridge.
4. If the DA is PAUSE Command (01-80-C2-00-00-01), then this packet will be dropped by ADM6999/X. ADM6999/X can issue and learn PAUSE command.

5. ADM6999/X will forward the packet with DA of (01-80-C2-00-00-00), filter out the packet with DA of (01-80-C2-00-00-01), and forward the packet with DA of (01-80-C2-00-00-02 ~ 01-80-C2-00-00-0F)

3.4.1.3 Address Aging

Address aging is supported for topology changes such as an address moving from one port to the other. When this happens, the ADM6999/X internally has a 300 seconds timer and will age out (remove) the address from the address table. Aging function can be enabled/disabled by user. Normally, disabling aging function is for security purpose.

3.4.1.4 Back off Algorithm

The ADM6999/X implements the truncated exponential back off algorithm compliant to the IEEE802.3 CSMA/CD standard. ADM6999/X will restart the back off algorithm by choosing 0-9 collision counts. The ADM6999/X resets the collision counter after 16 consecutive retransmit trials.

3.4.1.5 Inter-Packet Gap (IPG)

IPG is the idle time between any two successive packets from the same port. The typical number is 96 bits time. The value is 9.6us for 10Mbps ETHERNET, 960ns for 100Mbps fast ETHERNET. ADM6999/X provides option of 92 bit gap in EEPROM to prevent packet lost when turn off Flow Control and clock P.P.M. value difference.

3.4.1.6 Illegal Frames

The ADM6999/X will discard all illegal frames such as small packets (less than 64 bytes), oversized packets (greater than 1518 or 1522 bytes) and bad CRC. Dribbling packet with good CRC value will be accepted by ADM6999/X. In case of bypass mode being enabled, ADM6999/X will support tagged and untagged packets with size up to 1522 bytes. In case of non-bypass mode, ADM6999/X will support tagged packets up to 1526bytes, untagged packets up to 1522bytes.

3.4.1.7 Half Duplex Flow Control

Back Pressure function is supported for half-duplex operation. When the ADM6999/X cannot allocate a receive buffer for an incoming packet (buffer full), the device will transmit a jam pattern on the port, thus forcing a collision. Back Pressure is enabled by the BPEN set during RESET asserting. An Infineon-ADMtek Co Ltd proprietary algorithm is implemented inside the ADM6999/X to prevent back pressure function cause HUB partitioned under heavy traffic environment and reduce the packet lost rate to increase the whole system performance.

3.4.1.8 Full Duplex Flow Control

When full duplex port run out of its receive buffer, a PAUSE packet command will be issued by ADM6999/X to notice the packet sender and to pause transmission. This frame based flow control is totally compliant to IEEE 802.3x. ADM6999/X can issue or receive pause packet.

3.4.1.9 Broadcast Storm Filter

If Broadcast Storming filter is enable, the broadcast packets over the rising threshold within 50 ms will be discarded by the threshold setting. See EEPROM Reg.10h.

Broadcast storm mode after initial:

Time interval: 50 ms

The max. packet number = 7490 in 100Base, 749 in 10Base

Per Port Rising Threshold				
	00	01	10	11
All 100TX	Disable	10%	20%	40%
Not All 100TX	Disable	1%	2%	4%

Per Port Falling Threshold				
	00	01	10	11
All 100TX	Disable	5%	10%	20%
Not All 100TX	Disable	0.5%	1%	2%

3.4.2 Auto TP MDIX Function

In normal application which Switch connects to NIC card is by using one by one TP cable. If Switch connects other devices such as another Switch must be by two ways. The first way is to use the Cross Over TP cable. The second way it is to use extra RJ45 with internal TX+- and RX+- signal crossover. By second way customer can use one by one cable to connect two Switch devices. All these efforts need extra costs and are not a good solution. ADM6999/X provides Auto MDIX function which can adjust TX+- and RX+- at correct pin. Users can use one by one cable between ADM6999/X and other device. This function can be Enabled/Disabled by hardware pin and EEPROM configuration register 0x01h~0x09h bit 15. If hardware pin sets all ports at Auto MDIX mode then EEPROM setting is useless. If hardware pin sets all ports at non Auto MDIX mode then EEPROM can set each port's Auto MDIX function to be enabled or disabled.

3.4.3 Port Locking

Port locking function will provide customer a simple way to limit per port user number to one. If this function is turned on then ADM6999/X will lock first MAC address in learning table. This locked MAC address will never be aged out unless Reset signal. Other MAC address that is not same as locked one will be dropped. ADM6999/X provides one MAC address per port. This function is per port setting. When turn on Port Locking function, recommend customer turn off aging function. See EEPROM register 0x12h bit 0~8.

3.4.4 VLAN Setting & Tag/Untag & Port-base VLAN

ADM6999/X supports bypass mode and untagged port as default setting while the chip is power-on. Thus, every packet with or without tag will be forwarding to the destination port without any modification by ADM6999/X. Meanwhile port-base VLAN could be enabled according to the PVID value (user define 4bits to map 16 groups written at register 13 to register 22) of the configuration content of each port.

ADM6999/X also supports 16 802.1Q VLAN groups. In VLAN four bytes tag include twelve VLAN ID. ADM6999/X learns user to define four bits of VID. If user need to use this function, two EEPROM registers are needed to be programmed first:

- Port VID number at EEPROM register 0x01h~0x09h bit 13~10, register 0x28h~0x2bh and register 0x2ch bit 7~0: ADM6999/X will check coming packet. If coming packet is a non VLAN packet then ADM6999/X will use PVID as VLAN group reference. ADM6999/X will use packet's VLAN value when receive tagged packet.
- VLAN Group Mapping Register. EEPROM register 013h~022h define VLAN grouping value. User use these register to define VLAN group.

User can define each port as Tagged port or Untagged port by Configuration register Bit 4. The operation of packet between Tagged port and Untagged port can be explained by following example:

Example1: Port receives Untagged packet and send to Untagged port

ADM6999/X will check the port's user defined four bits of VLAN ID first then check VLAN group register. If the destination port is the same VLAN as the receiving port then this packet will forward to destination port without any change. If destination port is not the same VLAN as the receiving port then this packet will be dropped.

Example2: Port receives Untagged packet and send to Tagged port

ADM6999/X will check the port's user defined fours bits of VLAN ID first then check VLAN group register. If the destination port is the same VLAN as the receiving port than this packet will forward to destination port with four byte VLAN Tag and new CRC. If destination port is not the same VLAN as the receiving port then this packet will be dropped.

Example3: Port receives Tag packet and send to Untag port

ADM6999/X will check the packet VLAN ID first then check VLAN group resister. If the destination port is the same VLAN as the receiving port than this packet will forward to destination port after removing four bytes with new CRC error. If the destination port is not the same VLAN as the receiving port then this packet will be dropped.

Example4: Port receives Tag packet and send to Tag port

ADM6999/X will check the user define packet VLAN ID first then check VLAN group resister. If the destination port is the same VLAN as the receiving port than this packet will forward to destination port without any change. If the destination port is not the same VLAN as the receiving port then this packet will be dropped.

3.4.5 Priority Setting

It is a trend that data, voice and video will be put on networking, Switch not only deals data packets but also provides services of multimedia data. ADM6999/X provides two priority queues on each port with N:1 rate. See EEPROM Reg. 0x10h.

This priority function can set three ways as below:

- By Port Base: Set specific port at specific queue. ADM6999/X only checks the port priority and does not check the packet's content VLAN and TOS at bypass mode.
- By VLAN first: ADM6999/X checks VLAN three priority bit first then IP TOS priority bits. Chip must be set at Tagged mode.
- By IP TOS first: ADM6999/X checks IP TOS three priority bit first then VLAN three priority bits. Chip must be set at Tagged mode.

If port is set at VLAN/TOS priority but receiving packet without VLAN or TOS information then port base priority will be used.

3.4.6 LED Display

3.4.6.1 LED Display Mode

Three LEDs per port are provided by ADM6999/X. Link/Act, Duplex/Col & Speed are three LED displays of ADM6999/X. Dual color LED mode is also supported by ADM6999/X. For an easy production purpose ADM6999/X will send a test signal to each LED at power on reset stage. EEPROM register 0x12h defines LED configuration table.

ADM6999/X LED is an active Low signal. Dupcol0 & Dupcol1 will check external signal at Reset time. If external signal adds pull high then LED will active Low. If external signal adds pull down register then LED will drive high.

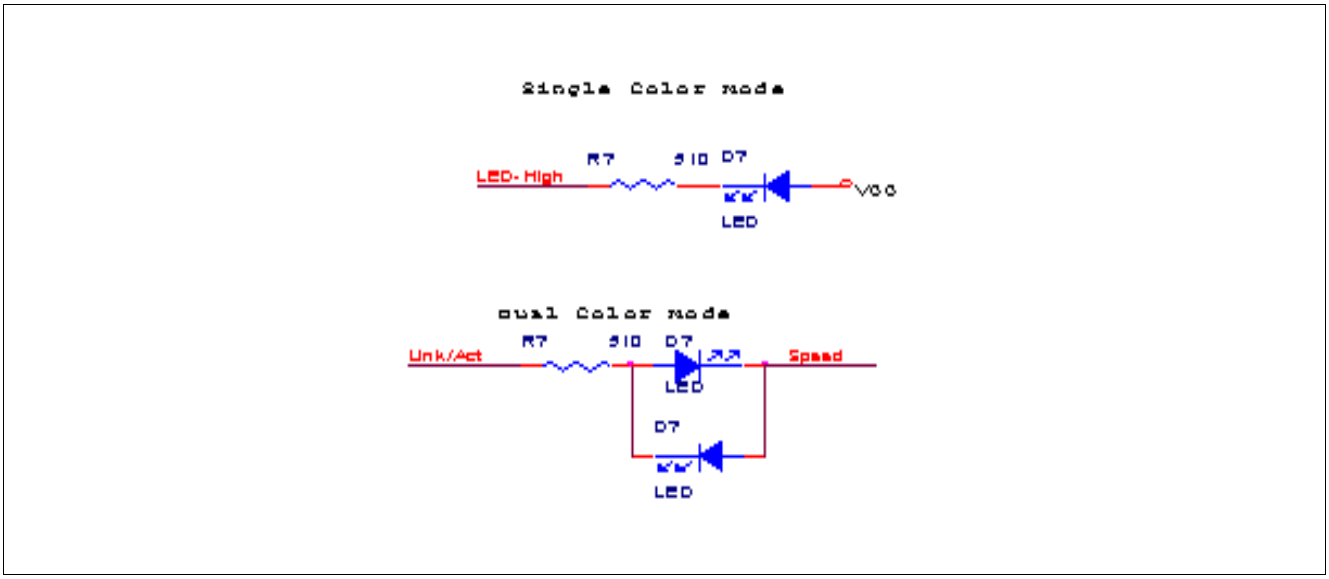


Figure 4 LED Display Mode

3.4.6.2 LED Display Interface

The ADM6999/X provides three different interfaces to drive the status to the LEDs. Each interface supports visibility of per port's speed, combined transmit and receive activity and duplex collision status. Different interfaces and color modes are applied according to LEDMODE pin and the configuration of the ADM6999/X latched during the power on reset. Refer to Table 1.3 for an illustration.

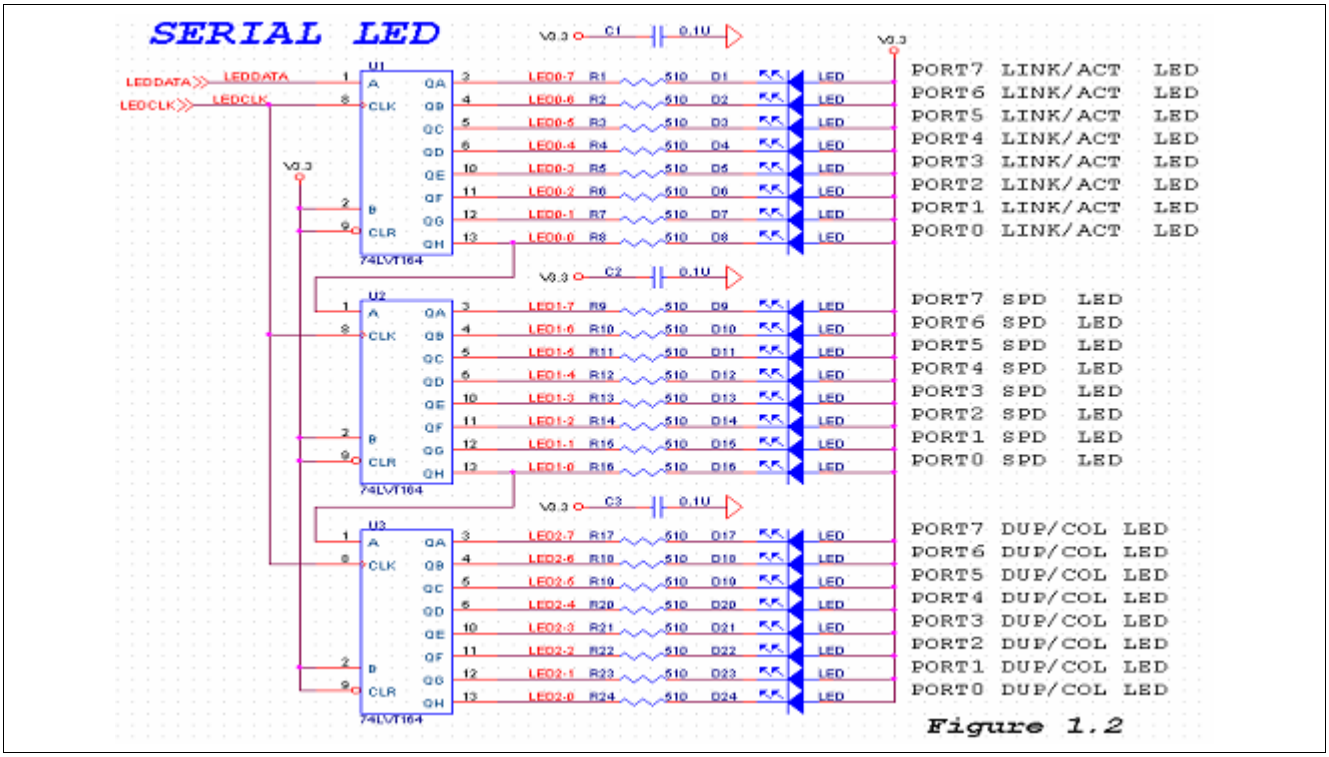


Figure 5 LED Display Interface

Table 3 LED Corresponding Interface

Configuration		LEDMODE	Interface utilized
ADM6999/X	8+1MII	1: dual color 0: single color	Serial Interface. Totally two pins, LEDCLK, and LEDDATA are used to output the LED status.
ADM6999/X	8+1 GPSI 8+1 RMII	1: dual color 0: single color	Parallel Interface. Three pins per port are used to output the LED status types.

3.4.6.2.1 Parallel LED Interface

Three pins per port are used to drive LEDs: l Link/Act, Duplex/Col & Speed. The color mode is controlled by the LEDMODE pin.

3.4.6.2.2 Serial LED Interface

A two pins interface, LEDDATA and LEDCLK, provides external shift register to capture the LED status indicated by the ADM6999/X. The status is encapsulated within the shift sequence, which is a consecutive stream of 8-bit status words. The first word is the DUPCOL status, the second is the speed status, and the last is the LNKACT status. Each word contains 8 bits and each bit corresponds to each port of the designated LED status. The designated LED status is sent first followed by port 1 then port 2, etc. The shift sequence is repeated every 40 ms and each bit last 640ns. Figure 1.2 shows the external circuit.

3.4.7 MII Connection with CPU

ADM6999/X supports MAC Mode MII. MAC mode MII can directly be connected with PHY. If user wants to connect ADM6999/X with CPU, user must reserve signal as below and set chip at 100M Full Duplex. ADM6999/X will drive 25M clock for MII interface. There is no extra logic at 100M Full Duplex connection.

Below connection is set CPU & Switch MII port at 100M Full Duplex. If user wants to set port at half duplex then COL signal needs to take care as:

COL = TXEN & RXDV. Select one chip TXEN and RXDV to create COL signal.

Some CPU supports reverse MII. It means CPU's MII can be set at MAC mode or PHY mode. User must check this point before connect ADM6999/X to CPU MAC port.

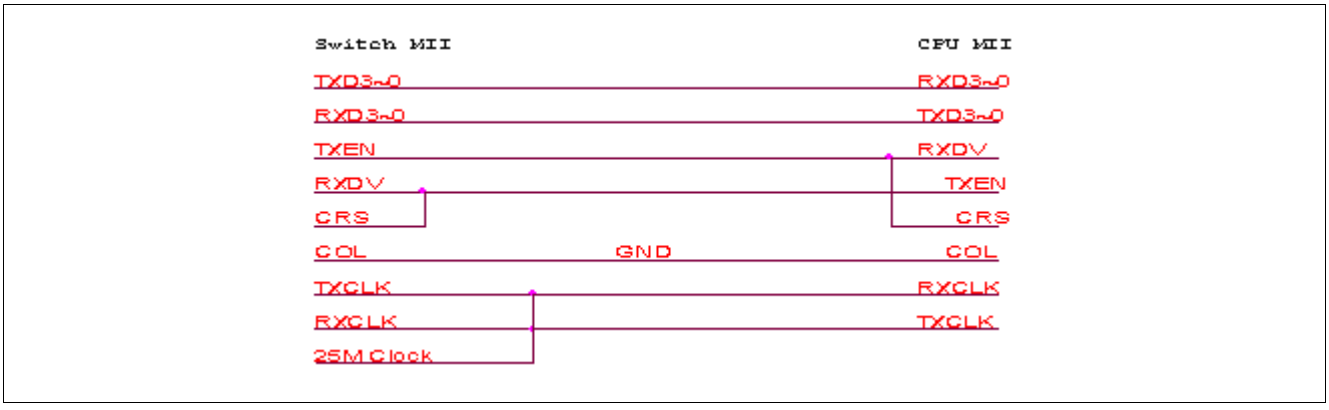


Figure 6 The MII Connection with CPU

3.5 EEPROM Content

EEPROM provides ADM6999/X many options setting such as:

- Port Configuration: Speed, Duplex, Flow Control Capability and Tag/Untag
- VLAN & TOS Priority Mapping
- Broadcast Storming rate and Trunk
- Fiber Select, Auto MDIX select
- VLAN Mapping
- Per Port Buffer number

3.5.1 EEPROM Registers

Table 4 Registers Address SpaceRegisters Address Space

Module	Base Address	End Address	Note
EEPROM	00_H	$2C_H$	

Table 5 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
SR	Signature Register	00_H	38
PCR_0	Port Configuration Register 0	01_H	39
PCR_1	Port 1 Configuration Register	02_H	40
PCR_2	Port 2 Configuration Register	03_H	40
PCR_3	Port 3 Configuration Register	04_H	40
PCR_4	Port 4 Configuration Register	05_H	40
PCR_5	Port 5 Configuration Register	06_H	40
PCR_6	Port 6 Configuration Register	07_H	40
PCR_7	Port 7 Configuration Register	08_H	40
PCR_8	Port 8 Configuration Register	09_H	40
VID01_OR	VID 0, 1 Option Register	$0A_H$	41
CR	Configuration Register	$0B_H$	42
VLAN_PMR	VLAN Priority Map Register	$0E_H$	43
TOS_PMR	TOS Priority Map Register	$0F_H$	44
MCR_0	Miscellaneous Configuration Register 0	10_H	46
VLAN_MSR	VLAN Mode Select Register	11_H	48
MCR_2	Miscellaneous Configuration Register 2	12_H	51
VLAN_MTR_0	VLAN Mapping Table Register 0	13_H	52
VLAN_MTR	VLAN Mapping Table Registers	13_H	52
PBTCR_P01	Port Buffer Threshold Control Reg. P0, P1	23_H	54
PBTCR_P23	Port Buffer Threshold Control Reg. P2, P3	24_H	54
PBTCR_P45	Port Buffer Threshold Control Reg. P4, P5	25_H	55
PBTCR_P67	Port Buffer Threshold Control Reg. P6, P7	26_H	55
TBTCR	Total Buffer Threshold Control Register	27_H	56
PVID11_4_CR_P01	Port0, 1 PVID bit11~4 Configuration Register	28_H	57
PVID11_4_CR_P23	Port2, 3 PVID bit11~4 Configuration Register	29_H	58
PVID11_4_CR_P45	Port4, 5 PVID bit 11~4 Configuration Register	$2A_H$	59
PVID11_4_CR_P67	Port6, 7 PVID bit 11~4 Configuration Register	$2B_H$	60
PVID11_4_VLAN_CR	P8 PVID bit 11~4/VLAN Group Shift Bits Conf.	$2C_H$	60

The register is addressed wordwise.

Table 6 Register Access Types

Mode	Symbol	Description HW	Description SW
read/write	rw	Register is used as input for the HW	Register is readable and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latches high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latches high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latches high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latches high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiates the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiates the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiates the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiates the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is readable and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is readable and writable by SW.

Table 7 Registers Clock DomainsRegisters Clock Domains

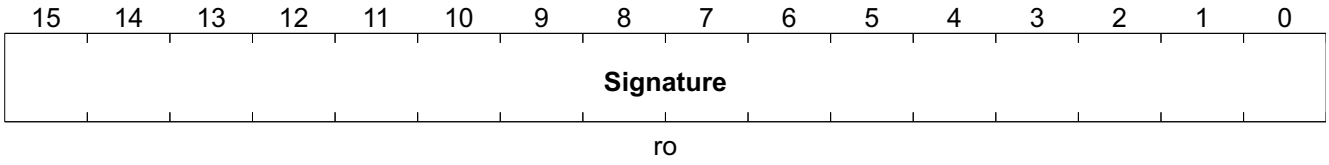
Clock Short Name	Description

3.5.1.1 EEPROM Registers Description

Signature Register

ADM6999/X will check register 0 value before read all EEPROM content. If this value does not match with 0x4154h then other values in EEPROM will be useless. ADM6999/X will use internal default value. User can not write Signature register when programming ADM6999/X internal register.

SR	Offset	Reset Value
Signature Register	**00_H**	**4154_H**



Field	Bits	Type	Description
Signature	15:0	ro	**Signature** 4154_H, must be the value of 4154_H

Configuration Registers

Register 0x09h bit5 is not effective on disable port. User can disable port by VLAN.

PCR_0 **Offset** **Reset Value**

Port Configuration Register 0 **01_H** **$040F_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANE	**SI**	**ID**				**PBPN**		**EN**	**TOS**	**PD**	**TP**	**DC**	**SC**	**AN**	**FC**
rw	rw	rw				rw		rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ANE	15	rw	**Auto MDIX Enable** Hardware Reset latch value EECK can set global Auto MDIX function. If hardware pin set all port at Auto MDIX then this bit is useless. If hardware pin set chip at non Auto MDIX then this bit can set each port at Auto MDIX. 0_B **D**, disable, default 1_B **E**, enable
SI	14	rw	**Select FX Interface** Port7 TX/FX can be set by hardware Reset latch value P7FX. If hardware pin set Port7 as FX then this bit is useless. If hardware pin set Port7 as TX then this pin can set Port7 as FX or TX. 0_B **TP**, TP mode, default 1_B **FX**, FX mode
ID	13:10	rw	**Port VLAN ID** Check Register 0x28h~0x2ch for other PVID[11:4]. Default 1.
PBPN	9:8	rw	**Port Base Priority Number** From 1~0 mapping to Q1~Q0. Default 0.
EN	7	rw	**Enable Port Based Priority** If this bit turns on then ADM6999/X will not check TOS or VLAN as priority reference. ADM6999/X will check port base priority only. ADM6999/X default is bypass mode which checks port base priority only. If user wants to check VLAN tag priority then he must set chip at Tag mode. See 0x11h. 0_B , Disable, default 1_B , Enable
TOS	6	rw	**TOS Over VLAN Priority** Define ADM6999/X priority source when VLAN & TOS existed in the packet. 0_B , VLAN priority level higher than TOS, default 1_B , TOS priority level higher than VLAN
PD	5	rw	**Port Disable** Does not include the Ninth port. The Ninth port disable can be done by VLAN separation. 0_B , enable port, default 1_B , disable port

Field	Bits	Type	Description
TP	4	rw	**VLAN Tag Port** 0_B , Untagged port, default 1_B , Tagged port
DC	3	rw	**Duplex Capability** 0_B , Half Duplex 1_B , Full Duplex, default
SC	2	rw	**Speed Capability** 0_B , 10M 1_B , 100M, default
AN	1	rw	**Auto Negotiation Capability Enable** 0_B , disable 1_B , enable, default
FC	0	rw	**802.3X Flow Control Capability** 0_B , disable 1_B , enable, default

All configuration registers have the same structure and characteristics, see **PCR_0**.
The offset addresses of the other configuration registers are listed in **Table 8**.

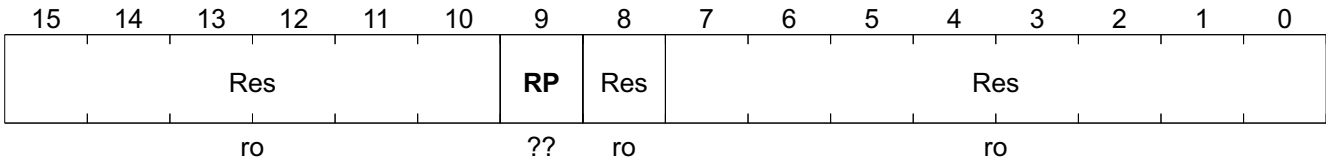
Table 8 Configuration Registers

Register Short Name	Register Long Name	Offset Address	Page Number
PCR_1	Port 1 Configuration Register	02_H	
PCR_2	Port 2 Configuration Register	03_H	
PCR_3	Port 3 Configuration Register	04_H	
PCR_4	Port 4 Configuration Register	05_H	
PCR_5	Port 5 Configuration Register	06_H	
PCR_6	Port 6 Configuration Register	07_H	
PCR_7	Port 7 Configuration Register	08_H	
PCR_8	Port 8 Configuration Register	09_H	

VID 0, 1 Option Register

Bit 9: Replaced VID 0, 1. 1/ADM6999/X will replace packet VID by PVID when coming packet's VID = 0 or 1, 0/ADM6999/X will not replace packet's VID 0 & 1.

VID01_OR	Offset	Reset Value
VID 0, 1 Option Register	**$0A_H$**	**5920_H**



Field	Bits	Type	Description
Res	15:10	ro	**Reserved** 010110_B , default
RP	9	rw	**Replaced Packet VID 0, 1 by PVID** 0_B , disable, default 1_B , enable
Res	8	ro	**Reserved** 1_B , default
Res	7:0	ro	**Reserved** 20_H , default

Configuration Register

CR	Offset	Reset Value
Configuration Register	$0B_H$	8000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE	Res	Res	Res					**ET**	**EL**	Res	Res				
??	ro	ro	ro					??	??	ro	ro				

Field	Bits	Type	Description
FE	15	rw	**Disable Far_End_Fault Detection** ADM6999/X will not recognize Far_End_Fault when turn on this bit. 0_B , enable 1_B , disable, default
Res	14	ro	**Reserved** 0_B , default
Res	13	ro	**Reserved** 0_B , default
Res	12:8	ro	**Reserved** 00000_B , default
ET	7	rw	**Enable Trunk** 0_B , Disable, default 1_B , enable Port6, 7 as Trunk port
EL	6	rw	**Enable IPG Leveling** 1/92 bit. 0/96 bit. When this bit is enable ADM6999/X will transmit packet out at 96 bit or 92 bit to clean buffer. If user disables this function then ADM6999/X will transmit packet at 96 bit. 0_B , Disable, default 1_B , Enable
Res	5	ro	**Reserved** 0_B , default
Res	4:0	ro	**Reserved** 00000_B , default

VLAN Priority Map Register

VLAN_PMR	Offset	Reset Value
VLAN Priority Map Register	$0E_H$	5500_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
V7		V6		V5		V4		V3		V2		V1		V0	
??		??		??		??		??		??		??		??	

Field	Bits	Type	Description
V7	15:14	rw	**Mapped Priority of Tag Value (VLAN) 7** 01_B , default
V6	13:12	rw	**Mapped Priority of Tag Value (VLAN) 6** 01_B , default
V5	11:10	rw	**Mapped Priority of Tag Value (VLAN) 5** 01_B , default
V4	9:8	rw	**Mapped Priority of Tag Value (VLAN) 4** 01_B , default
V3	7:6	rw	**Mapped Priority of Tag Value (VLAN) 3** 00_B , default
V2	5:4	rw	**Mapped Priority of Tag Value (VLAN) 2** 00_B , default
V1	3:2	rw	**Mapped Priority of Tag Value (VLAN) 1** 00_B , default
V0	1:0	rw	**Mapped Priority of Tag Value (VLAN) 0** 00_B , default

00: low priority queue. Q0

01: high priority queue. Q1

The weight ratio is 1:N. Queue ratio (defined in 0x10h bit[13:12])

Reg. 0x10 Bit[13:12]	Weight Ratio
00	1:1
01	1:2
10	1:3
11	1:4

The default is port-base priority for un-tagged packet and none IP frame.

TOS Priority Map Register

TOS_PMR	Offset	Reset Value
TOS Priority Map Register	$0F_H$	5500_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
V7		V6		V5		V4		V3		V2		V1		V0	
??		??		??		??		??		??		??		??	

Field	Bits	Type	Description
V7	15:14	rw	**Mapped Priority of Tag Value (TOS) 7** 01_B , default
V6	13:12	rw	**Mapped Priority of Tag Value (TOS) 6** 01_B , default
V5	11:10	rw	**Mapped Priority of Tag Value (TOS) 5** 01_B , default
V4	9:8	rw	**Mapped Priority of Tag Value (TOS) 4** 01_B , default
V3	7:6	rw	**Mapped Priority of Tag Value (TOS) 3** 00_B , default
V2	5:4	rw	**Mapped Priority of Tag Value (TOS) 2** 00_B , default
V1	3:2	rw	**Mapped Priority of Tag Value (TOS) 1** 00_B , default
V0	1:0	rw	**Mapped Priority of Tag Value (TOS) 0** 00_B , default

00: low priority queue. Q0

01: high priority queue. Q1

The weight ratio is 1:N. Queue ratio (defined in 0x10h/bit[13:12])

Reg. 0x10 Bit[13:12]	Weight Ratio
00	1:1
01	1:2
10	1:3
11	1:4

The default is port-base priority for un-tagged packet and none IP frame.

Packet with Priority

- Normal Packet Content

Ethernet Packet from Layer 2

Preamble/SFD	Destination (6 bytes)	Source (6 bytes)	Packet length (2 bytes)	Data (46-1500 bytes)	CRC (4 bytes)
–	Byte 0~5	Byte 6~11	Byte 12~13	Byte 14	–

- VLAN Packet

ADM6999/X will check packet byte 12 &13. If byte[12:13] = 8100h then this packet is a VLAN packet.

Tag Protocol TD 8100	Tag Control Information TCI	LEN Length	Routing Information
Byte 12~13	Byte14~15	Byte 16~17	Byte 18

- Byte 14~15: Tag Control Information TCI
- Bit[15:13]: User Priority 7~0
- Bit 12: Canonical Format Indicator (CFI)
- Bit[11~0]: VLAN ID. The ADM6999/X will use bit[3:0] as VLAN group.

- TOS IP Packet

ADM6999/X checks byte 12 &13 if this value is 0800h then ADM6999/X knows this is a TOS priority packet.

Type 0800	IP Header
Byte 12~13	Byte 14~15

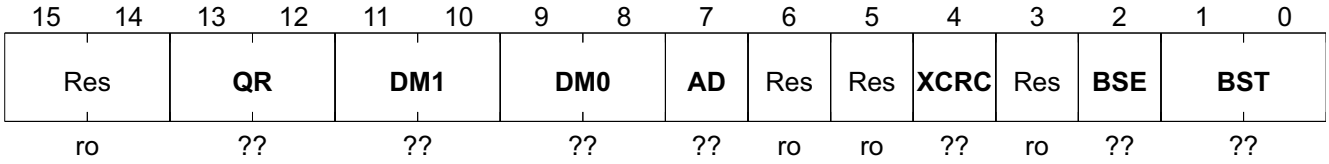
IP header define

Byte 14

- Bit[7:0]: IP protocol version number & header length
- Byte 15: Service type
- Bit[7~5]: IP Priority (Precedence) from 7~0
- Bit 4: No Delay (D)
- Bit 3: High Throughput
- Bit 2: High Reliability (R)
- Bit[1:0]: Reserved

Miscellaneous Configuration Register 0

MCR_0	Offset	Reset Value
Miscellaneous Configuration Register 0	**10_H**	**0040_H**



Field	Bits	Type	Description
Res	15:14	ro	**Reserved**
QR	13:12	rw	**Queue Ratio** 00_B , 1:1 01_B , 1:2 10_B , 1:3 11_B , 1:4
DM1	11:10	rw	**Discard Mode (drop scheme for Q1)**
DM0	9:8	rw	**Discard Mode (drop scheme for Q0)**
AD	7	rw	**Aging Disable** 0_B , enable aging, default 1_B , disable aging
Res	6	ro	**Reserved** 0_B , default
Res	5	ro	**Reserved** 0_B , default
XCRC	4	rw	**XCRC** 0_B , enable CRC Check, default 1_B , disable CRC check
Res	3	ro	**Reserved** 0_B , default
BSE	2	rw	**Broadcast Storming Enable** 0_B , disable, default 1_B , enable
BST	1:0	rw	**Broadcast Storming Threshold** See below table. 00_B , default

Bit[1:0]: Broadcast Storming threshold

Broadcast storm mode after initial:

Time interval: 50 ms

The max. packet number = 7490 in 100Base, 749 in 10Base

Table 9 Per Port Rising Threshold

	00	01	10	11
All 100TX	Disable	10%	20%	40%
Not All 100TX	Disable	1%	2%	4%

Table 10 Per Port Falling Threshold

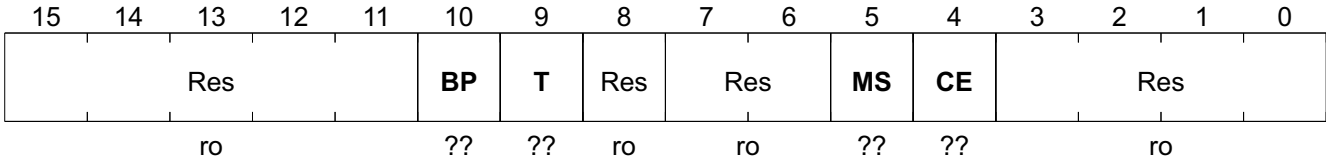
	00	01	10	11
All 100TX	Disable	5%	10%	20%
Not All 100TX	Disable	0.5%	1%	2%

Table 11 Drop Scheme for each Queue

Discard Mode/ Utilization	00	01	10	11
TBD	0%	0%	25%	50%

VLAN Mode Select Register

VLAN_MSR	Offset	Reset Value
VLAN Mode Select Register	11_H	$FF00_H$



Field	Bits	Type	Description
Res	15:11	ro	**Reserved** 11111_B , default
BP	10	rw	**Back-pressure Enable** This is a global pin for all ports. 0_B , disable 1_B , enable, default
T	9	rw	**RMII TXEN Timing** If user connects several ADM6999/X to be Hubbing Switch then this bit turns on. If user connects RMII to RMII PHY then this bit must turn off. RMII mode supports half duplex only. 0_B , RMII PHY 1_B , Hubbing Switch, default
Res	8	ro	**Reserved** 1_B , default
Res	7:6	ro	**Reserved** 00_B , default
MS	5	rw	**VLAN Mode Select** 0_B , by-pass mode with port-base VLAN, default 1_B , 802.1Q base VLAN
CE	4	rw	**MAC Clone Enable** 0_B , Normal mode. Learning with SA only. ADM6999/X files/searches MAC table by SA or DA only. Default. 1_B , MAC Clone mode. Learning with SA, VID0. ADM6999/X files/searches MAC table by SA or DA with VID0. This bit makes the chip learn two same addresses with different VID0.
Res	3:0	ro	**Reserved** 0000_B , default

Below is Bit4, 5 VLAN Tag and MAC application example based on Infineon-ADMtek Co Ltd ADM6999/X.

Table 12 ADM6996 Port Mapping with ADM6999/X

ADM6996	ADM6999/X
Port0	Port0
–	Port1
Port1	Port2
–	Port3
Port2	Port4
–	Port5
Port3	Port6
Port4	Port7
Port5 MII	Port8 MII

Below is Router old architecture. The disadvantages of this are:

1. WAN port only support 10M Half-Duplex and non-MDIX function.
2. Need extra 10M NIC costs.
3. ISA bus will become bottleneck of whole system.

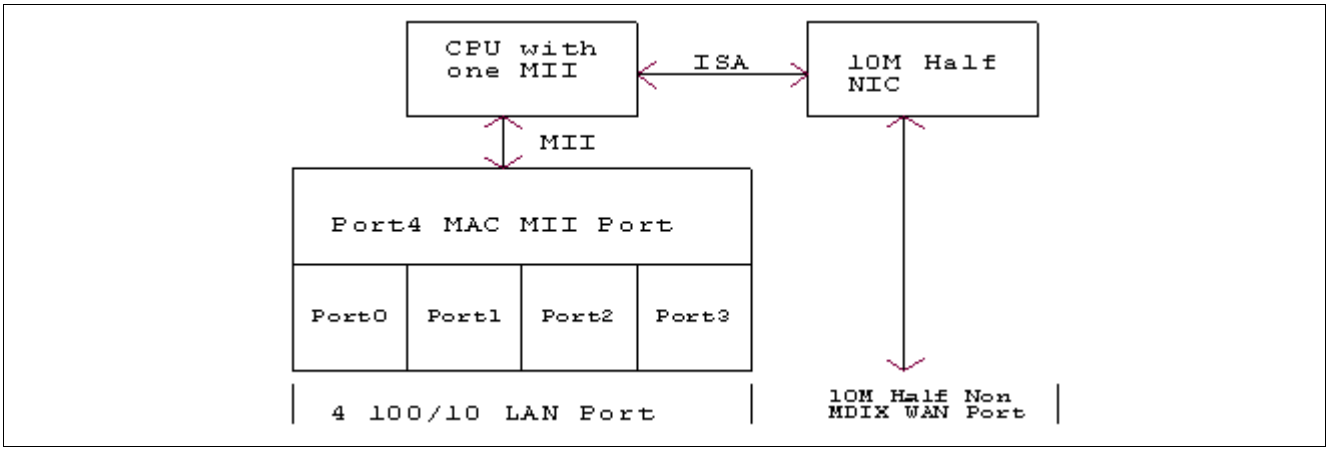


Figure 7 Router Old Architecture

Below is new architecture by using ADM6999/X serial chip VLAN function. The advantages of below are:

1. WAN Port can upgrade to 100/10 Full/Half, Auto MDIX.
2. WAN/LAN Port is programmable and put on the same Switch.
3. No need of extra NIC and saves lot of costs.
4. High bandwidth of MII port up to 200M speed.

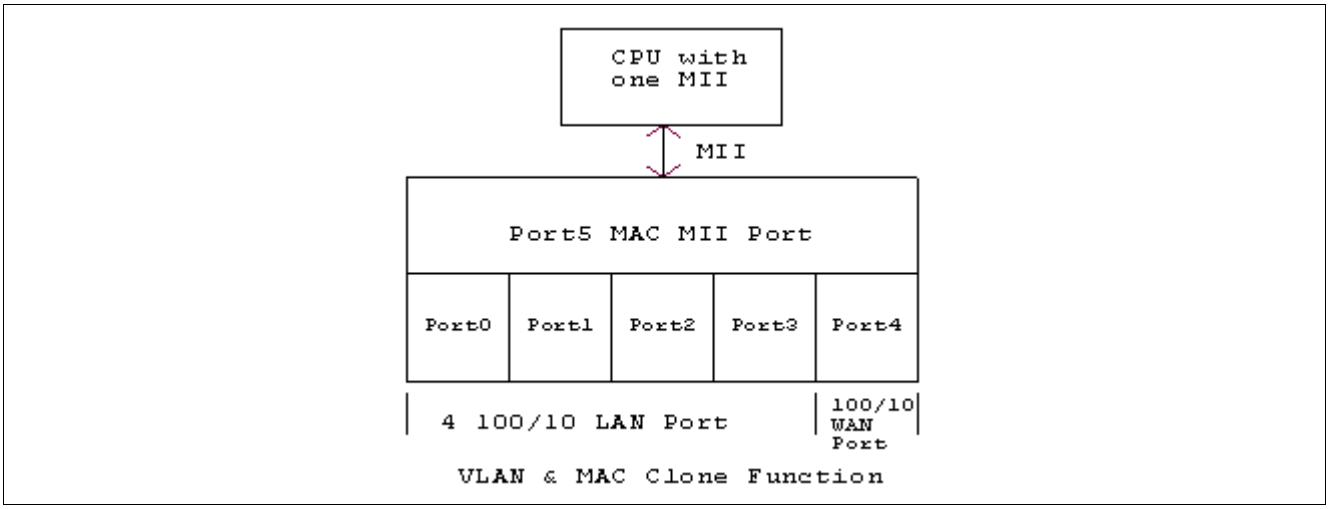


Figure 8 The New Architecture by Using ADM6999/X

New Router application works well on normal application. If user's ISP vendor (cable modem) lock Registration Card's ID then Router CPU must send this Lock Registration Card's ID to WAN Port. One condition that could happen is that there exist two same MAC ID on this Switch. One is the original Card and another one is CPU. This will make Switch learning table trouble.

ADM6999/X provides MAC Clone function that allows two same MAC addresses with different VLAN ID0 on learning table. This will solve Lock registration Card's ID issue. ADM6999/X serial chip will put these two same MAC addresses with different VLAN ID0 at different learning table entry.

How to Set ADM6999/X on Router:

- Port0~3: LAN Port
- Port4: WAN Port
- Port5: MII Port as CPU Port

Step1: Set Register 11_H bit4 and bit5 to 1.

{Coding: Write Register 11_H as $FF30_H$}

Step2: Set Port0~3 as Untag Port and set PVID = 1.

{Coding: Write Register 01_H, 03_H, 05_H, 07_H as $840F_H$. Port0~3 as Untag, PVID = 1, Enable MDIX}

Step3: Set Port4 as Untag Port and set PVID = 2.

{Coding: Write Register 08_H as $880F_H$. Port4 as Untag, PVID = 2, Enable MDIX.}

Step4: Set Port5 MII Port as Tag Port and set PVID = 2.

{Coding: Write Register 09_H as $881F_H$. Port5 MII port as Tag, PVID = 2.}

Step5: Group Port0, 1, 2, 3, 5 as VLAN 1.

{Coding: Write Register 14_H as 0155_H. VLAN1 cover Port0, 1, 2, 3, 5.}

Step6: Group Port4, 5 as VLAN 2.

{Coding: Write Register 15_H as 0180_H. VLAN2 cover Port4, 5.}

How MAC Clone Operation:

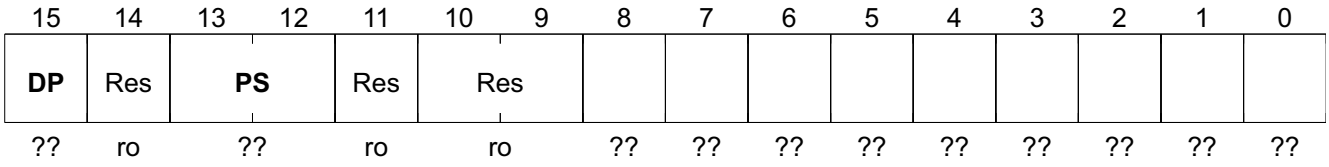
1. LAN to LAN/CPU Traffic. ADM6999/X LAN traffic to LAN/CPU only. Traffic to another LAN port will be untag packet. Traffic to CPU is Tag packet with VID = 1. CPU can check VID to distinguish LAN traffic or WAN traffic.
2. WAN to CPU Traffic. ADM6999/X WAN traffic to CPU only. Traffic to CPU is Tagged packet with VID = 2. CPU can check VID to distinguish LAN traffic or WAN traffic.
3. CPU to LAN Packet. ADM6999/X CPU Packet to LAN port must add VID = 1 in VLAN field. ADM6999/X checks VID to distinguish LAN traffic or WAN traffic. LAN output packet is Untagged.

4. CPU to WAN Packet. ADM6999/X CPU Packet to WAN port must add VID = 2 in VLAN filed. ADM6999/X check VID to distinguish LAN traffic or WAN traffic. WAN output packet is Untagged.
5. ADM6999/X learning sequence. ADM6999/X will check VLAN mapping setting first then check learning table. User does not worry about LAN/WAN traffic mix up.

Note: Bit 10: Half Duplex Back Pressure enable. 1/enable, 0/disable.

Miscellaneous Configuration Register 2

MCR_2	Offset	Reset Value
Miscellaneous Configuration Register 2	**12_H**	**3600_H**



Field	Bits	Type	Description
DP	15	rw	**Drop Packet when Excessive Collision Happen Enable** 0_B , Disable, default 1_B , enable
Res	14	ro	**Reserved**
PS	13:12	rw	**Power Saving Select**
Res	11:9	ro	**Reserved**
ML8	8	rw	**Port8 MAC Lock** 0_B , Disable, default 1_B , Locks first MAC source address
ML7	7	rw	**Port7 MAC Lock** 0_B , Disable, default 1_B , Locks first MAC source address
ML6	6	rw	**Port6 MAC Lock** 0_B , Disable, default 1_B , Locks first MAC source address
ML5	5	rw	**Port5 MAC Lock** 0_B , Disable, default 1_B , Locks first MAC source address
ML4	4	rw	**Port4 MAC Lock** 0_B , Disable, default 1_B , Locks first MAC source address
ML3	3	rw	**Port3 MAC Lock** 0_B , Disable, default 1_B , Locks first MAC source address
ML2	2	rw	**Port2 MAC Lock** 0_B , Disable, default 1_B , Locks first MAC source address

Field	Bits	Type	Description
ML1	1	rw	**Port1 MAC Lock** 0_B , Disable, default 1_B , Locks first MAC source address
ML0	0	rw	**Port0 MAC Lock** 0_B , Disable, default 1_B , Locks first MAC source address

Notes

1. *Bit [8:0]: Port Locking enable. Learn one MAC ID when enable. 1/enable. 0/disable.*
2. *Bit[15]: Half Duplex excessive collision (16) drop packet enable. 1/drop. 0/no drop.*

VLAN Mapping Table Register 0

16 VLAN Group: See Register 0x2ch bit 11 = 0

VLAN_MTR_0	Offset	Reset Value
VLAN Mapping Table Register 0	**13_H**	**H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res							**P8**	**P7**	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**
							??	??	??	??	??	??	??	??	??

Field	Bits	Type	Description
P8	8	rw	**VLAN Mapping Table** Port assignment
P7	7	rw	
P6	6	rw	
P5	5	rw	
P4	4	rw	
P3	3	rw	
P2	2	rw	
P1	1	rw	
P0	0	rw	

Select the VLAN group ports is to set the corresponding bits to 1.

VLAN Mapping Table Registers

32 VLAN Group: See Register $2C_H$ bit 11 = 1

VLAN_MTR	Offset	Reset Value
VLAN Mapping Table Registers	**13_H**	**H**

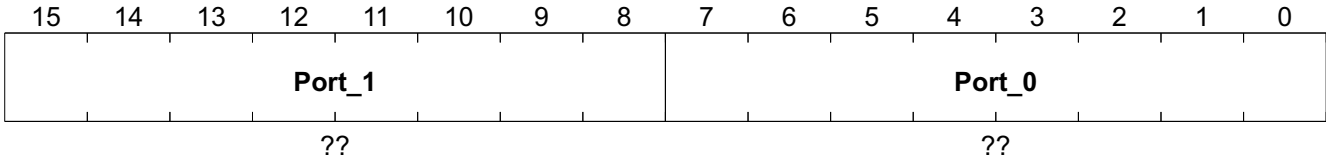
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P7	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**	**P7**	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**
??	??	??	??	??	??	??	??	??	??	??	??	??	??	??	??

Field	Bits	Type	Description
P7	15	rw	**Port 7, Odd VLAN Mapping Table**
P6	14	rw	**Port 6, Even VLAN Mapping Table**
P5	13	rw	**Port 5, Odd VLAN Mapping Table**
P4	12	rw	**Port 4, Even VLAN Mapping Table**
P3	11	rw	**Port 3, Odd VLAN Mapping Table**
P2	10	rw	**Port 2, Even VLAN Mapping Table**
P1	9	rw	**Port 1, Odd VLAN Mapping Table**
P0	8	rw	**Port 0, Even VLAN Mapping Table**
P7	7	rw	**Port 7, Odd VLAN Mapping Table**
P6	6	rw	**Port 6, Even VLAN Mapping Table**
P5	5	rw	**Port 5, Odd VLAN Mapping Table**
P4	4	rw	**Port 4, Even VLAN Mapping Table**
P3	3	rw	**Port 3, Odd VLAN Mapping Table**
P2	2	rw	**Port 2, Even VLAN Mapping Table**
P1	1	rw	**Port 1, Odd VLAN Mapping Table**
P0	0	rw	**Port 0, Even VLAN Mapping Table**

All VLAN groups will cover Port8 at 32 group mode. This feature is good for multiple ADM6999/X systems.

Port Buffer Threshold Control Registers P0, P1

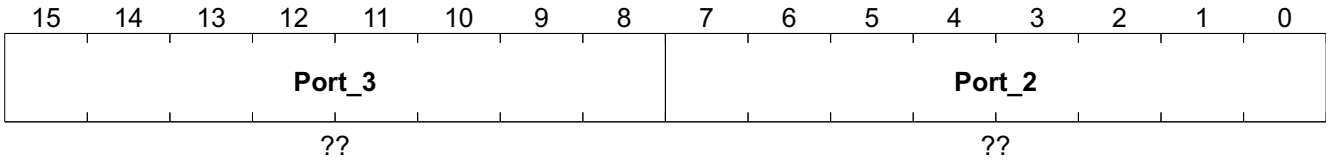
PBTCR_P01	Offset	Reset Value
Port Buffer Threshold Control Reg. P0, P1	23_H	0000_H



Field	Bits	Type	Description
Port_1	15:8	rw	**Port1 Buffer threshold control**
Port_0	7:0	rw	**Port0 Buffer threshold control**

Port Buffer Threshold Control Register P2, P3

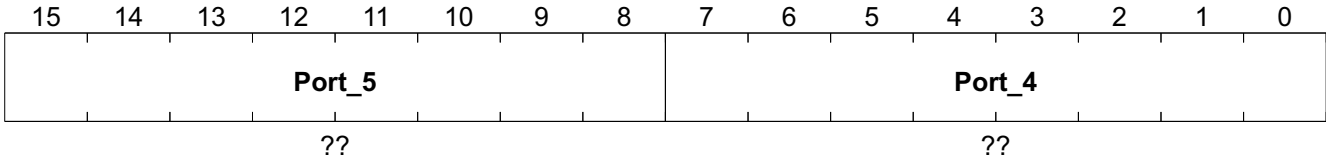
PBTCR_P23	Offset	Reset Value
Port Buffer Threshold Control Reg. P2, P3	24_H	0000_H



Field	Bits	Type	Description
Port_3	15:8	rw	**Port3 Buffer threshold control**
Port_2	7:0	rw	**Port2 Buffer threshold control**

Port Buffer Threshold Control Register P4, P5

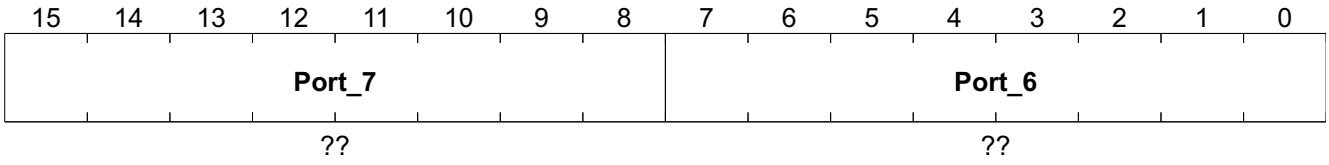
PBTCR_P45	Offset	Reset Value
Port Buffer Threshold Control Reg. P4, P5	25_H	0000_H



Field	Bits	Type	Description
Port_5	15:8	rw	**Port5 Buffer threshold control**
Port_4	7:0	rw	**Port4 Buffer threshold control**

Port Buffer Threshold Control Register P6, P7

PBTCR_P67	Offset	Reset Value
Port Buffer Threshold Control Reg. P6, P7	26_H	0000_H



Field	Bits	Type	Description
Port_7	15:8	rw	**Port7 Buffer threshold control**
Port_6	7:0	rw	**Port6 Buffer threshold control**

ADM6999/X supports buffer management scheme with dynamic thresholds to ensure the fair share of memory among different port queues. If users need each port to have a fixed threshold, they can configure the Bit14 in the 27_H to 1.

Dynamic threshold management:

Bit[7]: The add bit. Bit[6:0]: The offset bits.

When Bit[7] = 1, the switch will use the value (buffers really used + 2 * bit[6:0]) as the buffer count that the port has used.

When Bit[7] = 0, the switch will use the value (buffers really used - 2 * bit[6:0]) as the buffer count that the port has used.

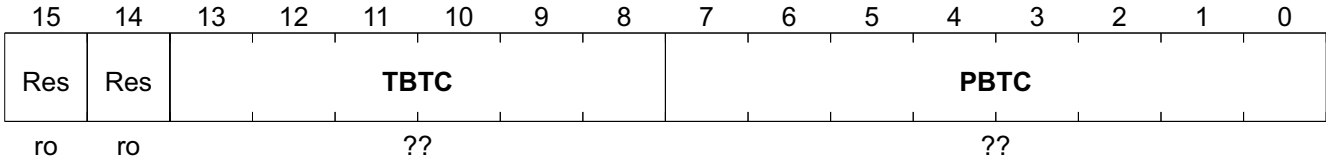
Fixed threshold management:

Bit[3:0]: The buffer threshold bits.

When the total buffer was not reached, the buffer amount allocated to each port will be equal to bit[3:0] * 4.

Total Buffer Threshold Control Register

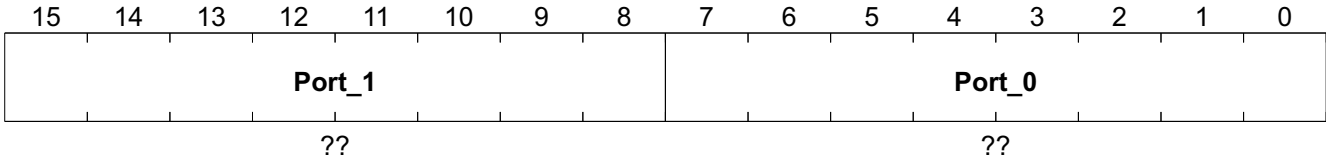
TBTCR	Offset	Reset Value
Total Buffer Threshold Control Register	27_H	0000_H



Field	Bits	Type	Description
Res	15	ro	**Reserved** 0_B , default
Res	14	ro	**Reserved** 0_B , default
TBTC	13:8	rw	**Total Buffer Threshold Control**
PBTC	7:0	rw	**Port8 Buffer Threshold Control** The configuration is the same as the other ports.

Port0, 1 PVID bit11~4 Configuration Register

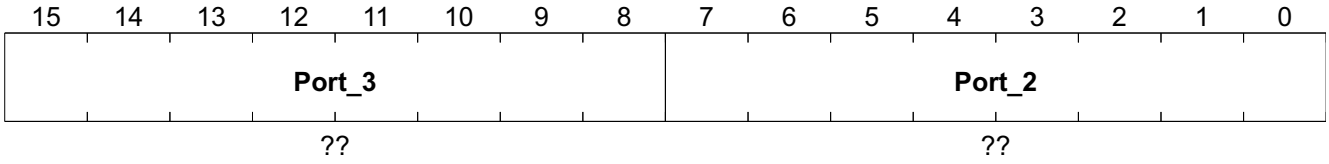
PVID11_4_CR_P01	Offset	Reset Value
Port0, 1 PVID bit11~4 Configuration Register	28_H	0000_H



Field	Bits	Type	Description
Port_1	15:8	rw	**Port1 PVID bit 11~4** These 8 bits combine with register 0x02h Bit[13~10] as full 12 bit VID. 00_H , default
Port_0	7:0	rw	**Port0 PVID bit 11~4** These 8 bits combine with register 0x01h Bit[13~10] as full 12 bit VID. 00_H , default

Port2, 3 PVID bit11~4 Configuration Register

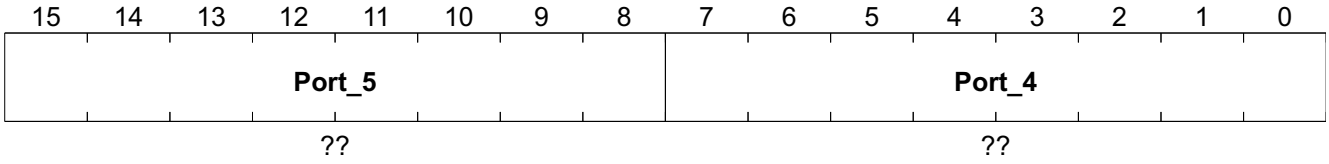
PVID11_4_CR_P23	Offset	Reset Value
Port2, 3 PVID bit11~4 Configuration Register	29_H	0000_H



Field	Bits	Type	Description
Port_3	15:8	rw	**Port3 PVID bit 11~4** These 8 bits combine with register 0x04h Bit[13~10] as full 12 bit VID. 00_H , default
Port_2	7:0	rw	**Port2 PVID bit 11~4** These 8 bits combine with register 0x03h Bit[13~10] as full 12 bit VID. 00_H , default

Port4, 5 PVID bit 11~4 Configuration Register

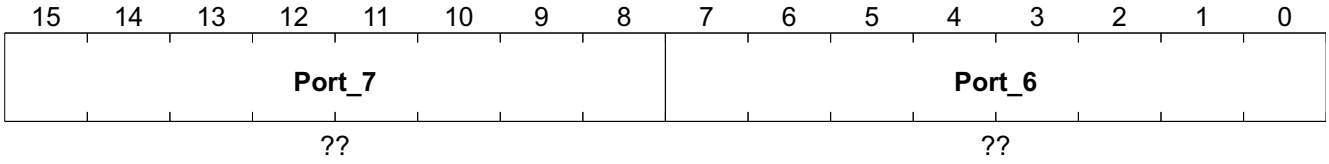
PVID11_4_CR_P45	Offset	Reset Value
Port4, 5 PVID bit 11~4 Configuration Register	$2A_H$	0000_H



Field	Bits	Type	Description
Port_5	15:8	rw	**Port5 PVID bit 11~4** These 8 bits combine with register 0x06h Bit[13~10] as full 12 bit VID. 00_H , default
Port_4	7:0	rw	**Port4 PVID bit 11~4** These 8 bits combine with register 0x05h Bit[13~10] as full 12 bit VID. 00_H , default

Port6, 7 PVID bit 11~4 Configuration Register

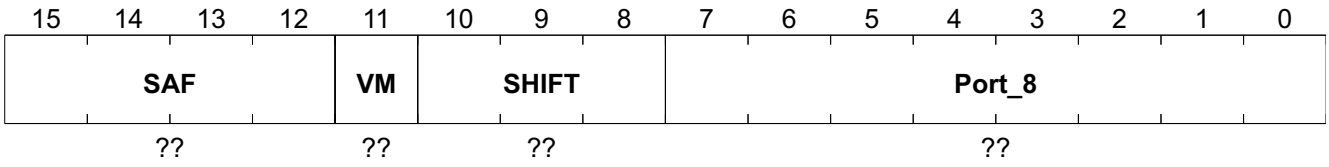
PVID11_4_CR_P67	Offset	Reset Value
Port6, 7 PVID bit 11~4 Configuration Register	$2B_H$	0000_H



Field	Bits	Type	Description
Port_7	15:8	rw	**Port7 PVID bit 11~4** These 8 bits combine with register 0x08h Bit[13~10] as full 12 bit VID. 00_H , default
Port_6	7:0	rw	**Port6 PVID bit 11~4** These 8 bits combine with register 0x07h Bit[13~10] as full 12 bit VID. 00_H , default

Port8 PVID bit 11~4 and VLAN Group Shift Bits Configuration Register

PVID11_4_VLAN_CR	Offset	Reset Value
P8 PVID bit 11~4/VLAN Group Shift Bits Conf.	$2C_H$	$D000_H$



Field	Bits	Type	Description
SAF	15:12	rw	**Special Address Forwarding** IEEE 802.3 reserved DA forward or drop police 1101_H , default **Bit[15]** Control reserved MAC (0180C2000010-0180C20000FF) 0_B , Discard 1_B , Forward, default **Bit[14]** Control reserved MAC (0180C2000002- 0180C200000F) 0_B , Discard 1_B , Forward, default **Bit[13]** Control reserved MAC (0180C2000001) 0_B , Discard, default 1_B , Forward **Bit[12]** Control reserved MAC (0180C2000000) 0_B , Discard 1_B , Forward, default
VM	11	rw	**VLAN Mode** 1/32 VLAN group, 0/16 VLAN group 0_B , default
SHIFT	10:8	rw	**Tag Shift for VLAN Grouping** VLAN Tagshift register. ADM6999/X will select 4/5 bit from total 12 bit VID as VLAN group reference. Select 4 or 5 bit from VID depends on bit 11 setting. For example Bit[10:8] = 001, Bit11 = 0,then ADM6999/X will select packet VID4~VID1 as VLAN group mapping. It is very flexible for user on VLAN grouping. $00C_H$, default **16 VLAN Mode** 0_D , VID[3:0] 1_D , VID[4:1] 2_D , VID[5:2] 3_D , VID[6:3] 4_D , VID[7:4] 5_D , VID[8:5] 6_D , VID[9:6] 7_D , VID[10:7] **32 VLAN Mode** 0_D , VID[4:0] 1_D , VID[5:1] 2_D , VID[6:2] 3_D , VID[7:3] 4_D , VID[8:4] 5_D , VID[9:5] 6_D , VID[10:6] 7_D , VID[11:7]

Field	Bits	Type	Description
Port_8	7:0	rw	**Port8 PVID bit 11~4** These 8 bits combine with register 09_H Bit[13~10] as full 12 bit VID. 00_H , default

3.6 EEPROM Access Description

Customer can select if ADM6999/X reads EEPROM contents as chip setting or not. ADM6999/X will check the signature of EEPROM to decide if reading content of EEPROM or not.

Table 13 RC & EEPROM Content Relationship

RC	CS	SK	DI	DO
0	High Impedance	High Impedance	High Impedance	High Impedance
Rising edge 01 (30ms)	Output	Output	Output	Input
1 (after 30 ms)	Input	Input	I/O	Input

Keep at least 30 ms after RC from 0 to 1. ADM6999/X will read data from EEPROM. After RC from 0 to 1, if CPU update EEPROM then ADM6999/X will update configuration registers too.

When CPU programming EEPROM & ADM6999/X, ADM6999/X recognizes the EEPROM WRITE instruction only. If there is any Protection instruction before or after the EEPROM WRITE instruction, CPU needs to generate separated CS signal cycle for each Protection & WRITE instruction.

CPU can directly program ADM6999/X after 30ms of Reset signal rising edge with or without EEPROM.

ADM6999/X serial chips will latch hardware-reset value as recommend value. It includes EEPROM interface:

- EECS: Internal Pull down 40K resister.
- EESK: TP port Auto-MDIX select. Internal pull down 40K resister as non Auto-MDIX mode.
- EDI: Dual Color Select. Internal pull down 40K resister as Single Color Mode.
- EDO: EEPROM enable. Internal pull up 40K resister as EEPROM enable.

Below Figure is ADM6999/X serial chips EEPROM pins' operation at different stages. Reset signal is controlled by CPU with at least 100ms low. Point1 is Reset rising edge. CPU must prepare proper value on ECS(0), EESK, EDI, EDO(1) before this rising edge. ADM6999/X will read this value into chip at Point2. CPU must keep these values over point2. Point2 is 200ns after Reset rising edge.

ADM6999/X serial chips will read EEPROM content at Point4 which 800ns far away from the rising edge of Reset. CPU must turn EEPROM pins EECS, EESK, EDI and EDO to High-Z or pull high before Point4.

If user wants to change state to High-Z or pull high on EEPROM pins, the order is CS-> DI -> DO -> SK is better.

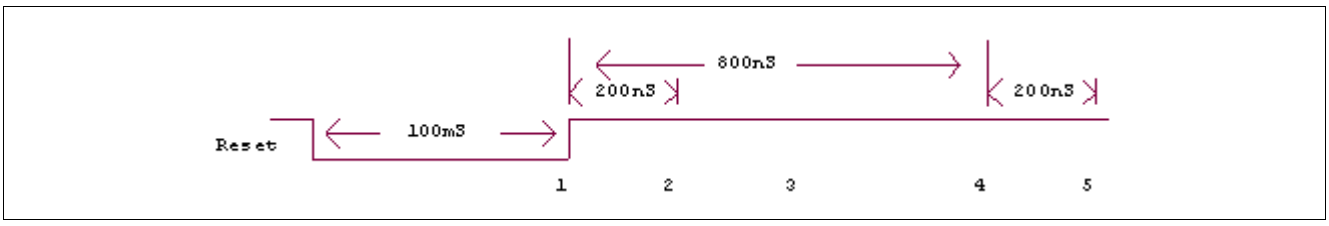


Figure 9 The ADM6999/X Serial Chips EEPROM Operation

It is a little bit different with the timing on writing EEPROM. See below graph. It must be carefully when CS goes down after writing a command, SK must issue at least one clock. This is a difference between ADM6999/X and EEPROM write timing. If the system is without EEPROM then user must write ADM6999/X internal register by 93C66 timing. If user uses EEPROM then the write timing depends on EEPROM type.

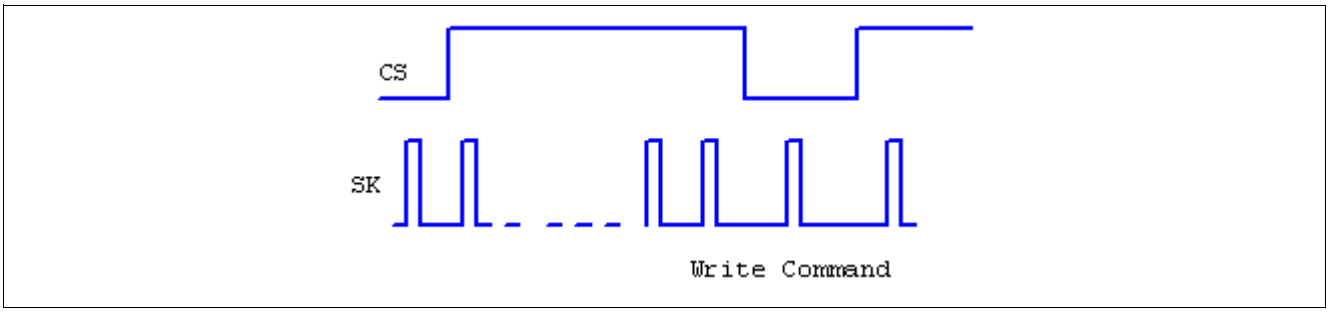


Figure 10 The difference on writing EEPROM

4 Serial Management

This chapter provides the Serial Management Registers overview and descriptions, and the Serial Interface Timing.

4.1 Serial Management Registers

Table 14 Registers Address SpaceRegisters Address Space

Module	Base Address	End Address	Note
EEPROM	00_H	$3C_H$	

Table 15 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
Chip_ID	Chip Identifier Register	00_H	67
PSR_0	Port Status 0 Register	01_H	68
PSR_1	Port Status 1 Register	02_H	71
CBSR	Cable Broken Status Register	03_H	72
RPC_0	Port 0 Receive Packet Count	04_H	72
RPC_1	Port 1 Receive Packet Count	05_H	73
RPBC_2	Port 2 Receive Packet Byte Count	05_H	73
RPC_2	Port 2 Receive Packet Count	06_H	73
RPC_3	Port 3 Receive Packet Count	07_H	73
RPC_4	Port 4 Receive Packet Count	08_H	73
RPC_5	Port 5 Receive Packet Count	09_H	73
RPC_6	Port 6 Receive Packet Count	$0A_H$	73
RPC_7	Port 7 Receive Packet Count	$0B_H$	73
RPC_8	Port 8 Receive Packet Count	$0C_H$	73
RPBC_0	Port 0 Receive Packet Byte Count	$0E_H$	73
RPBC_1	Port 1 Receive Packet Byte Count	$0F_H$	73
RPBC_3	Port 3 Receive Packet Byte Count	10_H	73
RPBC_4	Port 4 Receive Packet Byte Count	11_H	73
RPBC_5	Port 5 Receive Packet Byte Count	12_H	73
RPBC_6	Port 6 Receive Packet Byte Count	13_H	73
RPBC_7	Port 7 Receive Packet Byte Count	14_H	73
RPBC_8	Port 8 Receive Packet Byte Count	15_H	73
TPC_0	Port 0 Transmit Packet Count	16_H	73
TPC_1	Port 1 Transmit Packet Count	17_H	73
TPC_2	Port 2 Transmit Packet Count	18_H	73
TPC_3	Port 3 Transmit Packet Count	19_H	73
TPC_4	Port 4 Transmit Packet Count	$1A_H$	73
TPC_5	Port 5 Transmit Packet Count	$1B_H$	73
TPC_6	Port 6 Transmit Packet Count	$1C_H$	73
TPC_7	Port 7 Transmit Packet Count	$1D_H$	73

Table 15 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
TPC_8	Port 8 Transmit Packet Count	$1E_H$	73
TPBC_0	Port 0 Transmit Packet Byte Count	$1F_H$	73
TPBC_1	Port 1 Transmit Packet Byte Count	20_H	73
TPBC_2	Port 2 Transmit Packet Byte Count	21_H	73
TPBC_3	Port 3 Transmit Packet Byte Count	22_H	73
TPBC_4	Port 4 Transmit Packet Byte Count	23_H	73
TPBC_5	Port 5 Transmit Packet Byte Count	24_H	73
TPBC_6	Port 6 Transmit Packet Byte Count	25_H	73
TPBC_7	Port 7 Transmit Packet Byte Count	26_H	73
TPBC_8	Port 8 Transmit Packet Byte Count	27_H	74
CC_0	Port 0 Collision Count	28_H	74
CC_1	Port 1 Collision Count	29_H	74
CC_2	Port 2 Collision Count	$2A_H$	74
CC_3	Port 3 Collision Count	$2B_H$	74
CC_4	Port 4 Collision Count	$2C_H$	74
CC_5	Port 5 Collision Count	$2D_H$	74
CC_6	Port 6 Collision Count	$2E_H$	74
CC_7	Port 7 Collision Count	$2F_H$	74
CC_8	Port 8 Collision Count	30_H	74
EC_0	Port 0 Error Count	31_H	74
EC_1	Port 1 Error Count	32_H	74
EC_2	Port 2 Error Count	33_H	74
EC_3	Port 3 Error Count	34_H	74
EC_4	Port 4 Error Count	35_H	74
EC_5	Port 5 Error Count	36_H	74
EC_6	Port 6 Error Count	37_H	74
EC_7	Port 7 Error Count	38_H	74
EC_8	Port 8 Error Count	39_H	74
OFFR_0	Over Flow Flag 0 Register	$3A_H$	75
OFFR_1	Over Flow Flag 1 Register	$3B_H$	76
OFFR_2	Over Flow Flag 2 Register	$3C_H$	77

The register is addressed wordwise.

Table 16 Register Access Types

Mode	Symbol	Description HW	Description SW
read/write	rw	Register is used as input for the HW	Register is readable and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)

Table 16 Register Access Types (cont'd)

Mode	Symbol	Description HW	Description SW
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latches high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latches high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latches high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latches high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiates the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiates the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiates the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiate sthe input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is readable and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is readable and writable by SW.

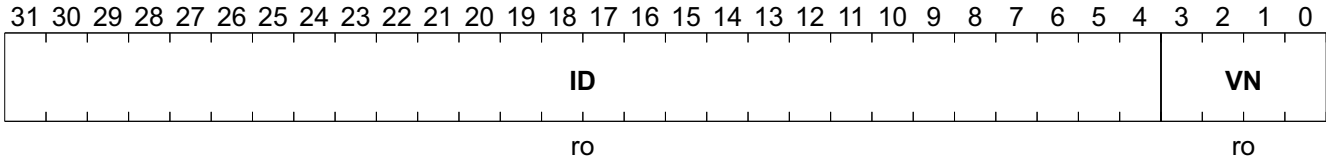
Table 17 Registers Clock DomainsRegisters Clock Domains

Clock Short Name	Description

4.1.1 Serial Management Registers Description

Chip Identifier Register

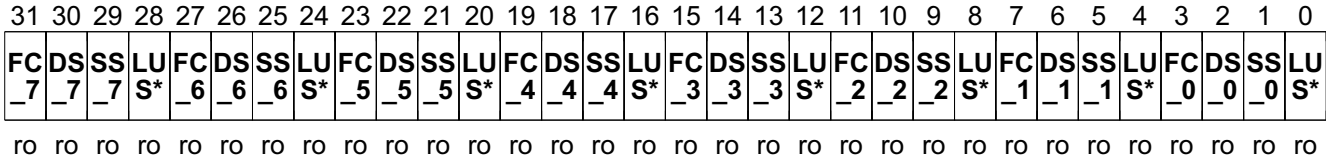
Chip_ID	Offset	Reset Value
Chip Identifier Register	00_H	$0002\ 1120_H$



Field	Bits	Type	Description
ID	31:4	ro	**ID** 0002112_H **ID**,
VN	3:0		**Version number** 0000_B **VN**,

Port Status 0 Register

PSR_0	Offset	Reset Value
Port Status 0 Register	**01_H**	**0000 0000_H**



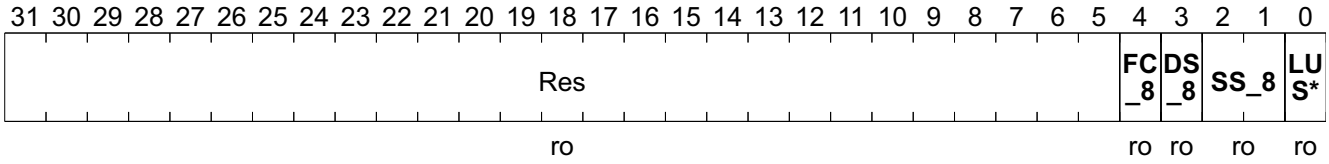
Field	Bits	Type	Description
FC_7	31	ro	**Port 7 Flow Control Enable** 0_B , Flow Control Disable 1_B , 802.3X on for full duplex or back pressure on for half duplex
DS_7	30	ro	**Port 7 Duplex Status** 0_B , Half Duplex 1_B , Full Duplex
SS_7	29	ro	**Port 7 Speed Status** 0_B , 10 Mbit/s 1_B , 100 Mbit/s
LUS_7	28	ro	**Port 7 Linkup Status** 0_B , Link is not established 1_B , Link is established
FC_6	27	ro	**Port 6 Flow Control Enable** 0_B , Flow Control Disable 1_B , 802.3X on for full duplex or back pressure on for half duplex
DS_6	26	ro	**Port 6 Duplex Status** 0_B , Half Duplex 1_B , Full Duplex
SS_6	25	ro	**Port 6 Speed Status** 0_B , 10 Mbit/s 1_B , 100 Mbit/s

Field	Bits	Type	Description
LUS_6	24	ro	**Port 6 Linkup Status** 0_B , Link is not established 1_B , Link is established
FC_5	23	ro	**Port 5 Flow Control Enable** 0_B , Flow Control Disable 1_B , 802.3X on for full duplex or back pressure on for half duplex
DS_5	22	ro	**Port 5 Duplex Status** 0_B , Half Duplex 1_B , Full Duplex
SS_5	21	ro	**Port 5 Speed Status** 0_B , 10 Mbit/s 1_B , 100 Mbit/s
LUS_5	20	ro	**Port 5 Linkup Status** 0_B , Link is not established 1_B , Link is established
FC_4	19	ro	**Port 4 Flow Control Enable** 0_B , Flow Control Disable 1_B , 802.3X on for full duplex or back pressure on for half duplex
DS_4	18	ro	**Port 4 Duplex Status** 0_B , Half Duplex 1_B , Full Duplex
SS_4	17	ro	**Port 4 Speed Status** 0_B , 10 Mbit/s 1_B , 100 Mbit/s
LUS_4	16	ro	**Port 4 Linkup Status** 0_B , Link is not established 1_B , Link is established
FC_3	15	ro	**Port 3 Flow Control Enable** 0_B , Flow Control Disable 1_B , 802.3X on for full duplex or back pressure on for half duplex
DS_3	14	ro	**Port 3 Duplex Status** 0_B , Half Duplex 1_B , Full Duplex
SS_3	13	ro	**Port 3 Speed Status** 0_B , 10 Mbit/s 1_B , 100 Mbit/s
LUS_3	12	ro	**Port 3 Linkup Status** 0_B , Link is not established 1_B , Link is established
FC_2	11	ro	**Port 2 Flow Control Enable** 0_B , Flow Control Disable 1_B , 802.3X on for full duplex or back pressure on for half duplex
DS_2	10	ro	**Port 2 Duplex Status** 0_B , Half Duplex 1_B , Full Duplex

Field	Bits	Type	Description
SS_2	9	ro	**Port 2 Speed Status** 0_B , 10 Mbit/s 1_B , 100 Mbit/s
LUS_2	8	ro	**Port 2 Linkup Status** 0_B , Link is not established 1_B , Link is established
FC_1	7	ro	**Port 1 Flow Control Enable** 0_B , Flow Control Disable 1_B , 802.3X on for full duplex or back pressure on for half duplex
DS_1	6	ro	**Port 1 Duplex Status** 0_B , Half Duplex 1_B , Full Duplex
SS_1	5	ro	**Port 1 Speed Status** 0_B , 10 Mbit/s 1_B , 100 Mbit/s
LUS_1	4	ro	**Port 1 Linkup Status** 0_B , Link is not established 1_B , Link is established
FC_0	3	ro	**Port 0 Flow Control Enable** 0_B , Flow Control Disable 1_B , 802.3X on for full duplex or back pressure on for half duplex
DS_0	2	ro	**Port 0 Duplex Status** 0_B , Half Duplex 1_B , Full Duplex
SS_0	1	ro	**Port 0 Speed Status** 0_B , 10 Mbit/s 1_B , 100 Mbit/s
LUS_0	0	ro	**Port 0 Linkup Status** 0_B , Link is not established 1_B , Link is established

Port Status 1 Register

PSR_1	Offset	Reset Value
Port Status 1 Register	02_H	$0000\ 0000_H$



Field	Bits	Type	Description
Res	31:5	ro	**Reserved** 0_H , default
FC_8	4		**Port 8 Flow Control Enable** 0_B , Flow Control Disable 1_B , 802.3X on for full duplex or back pressure on for half duplex
DS_8	3		**Port 8 Duplex Status** 0_B , Half Duplex 1_B , Full Duplex
SS_8	2:1		**Port 8 Speed Status** Two bits indicate the operating speed 00_B , 10 Mbit/s 01_B , 100 Mbit/s $1x_B$, 1000 Mbit/s
LUS_8	0		**Port 8 Linkup Status** 0_B , Link is not established 1_B , Link is established

Cable Broken Status Register

CBSR	Offset	Reset Value
Cable Broken Status Register	03_H	$0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res								CB_7	CBL_7		CB_6	CBL_6		CB_5	CBL_5		CB_4	CBL_4		CB_3	CBL_3		CB_2	CBL_2		CB_1	CBL_1		CB_0	CBL_0	
ro								ro	ro		ro	ro		ro	ro		ro	ro		ro	ro		ro	ro		ro	ro		ro	ro	

Field	Bits	Type	Description
Res	31:24	ro	**Reserved** 0_H , default
CB_7	23		**Port 7 Cable Broken**
CBL_7	22:21		**Port 7 Cable Broken Length**
CB_6	20		**Port 6 Cable Broken**
CBL_6	19:18		**Port 6 Cable Broken Length**
CB_5	17		**Port 5 Cable Broken**
CBL_5	16:15		**Port 5 Cable Broken Length**
CB_4	14		**Port 4 Cable Broken**
CBL_4	13:12		**Port 4 Cable Broken Length**
CB_3	11		**Port 3 Cable Broken**
CBL_3	10:9		**Port 3 Cable Broken Length**
CB_2	8		**Port 2 Cable Broken**
CBL_2	7:6		**Port 2 Cable Broken Length**
CB_1	5		**Port 1 Cable Broken**
CBL_1	4:3		**Port 1 Cable Broken Length**
CB_0	2		**Port 0 Cable Broken**
CBL_0	1:0		**Port 0 Cable Broken Length**

Port 0 Receive Packet Count

RPC_0	Offset	Reset Value
Port 0 Receive Packet Count	04_H	$0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Count_0																															
ro																															

Field	Bits	Type	Description
Count_0	31:0	ro	**Port 0 Receive Packet Count**

Other Port Registers have a similar structure as **RPC_0**; see **Table 18**.

Table 18 Port Registers

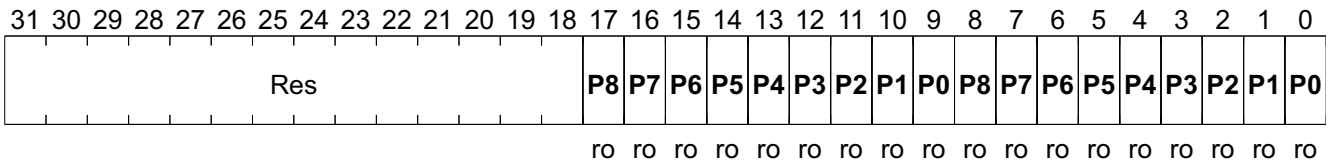
Register Short Name	Register Long Name	Offset Address	Page Number
RPC_1	Port 1 Receive Packet Count	05_H	
RPC_2	Port 2 Receive Packet Count	06_H	
RPC_3	Port 3 Receive Packet Count	07_H	
RPC_4	Port 4 Receive Packet Count	08_H	
RPC_5	Port 5 Receive Packet Count	09_H	
RPC_6	Port 6 Receive Packet Count	$0A_H$	
RPC_7	Port 7 Receive Packet Count	$0B_H$	
RPC_8	Port 8 Receive Packet Count	$0C_H$	
RPBC_0	Port 0 Receive Packet Byte Count	$0E_H$	
RPBC_1	Port 1 Receive Packet Byte Count	$0F_H$	
RPBC_2	Port 2 Receive Packet Byte Count	05_H	
RPBC_3	Port 3 Receive Packet Byte Count	10_H	
RPBC_4	Port 4 Receive Packet Byte Count	11_H	
RPBC_5	Port 5 Receive Packet Byte Count	12_H	
RPBC_6	Port 6 Receive Packet Byte Count	13_H	
RPBC_7	Port 7 Receive Packet Byte Count	14_H	
RPBC_8	Port 8 Receive Packet Byte Count	15_H	
TPC_0	Port 0 Transmit Packet Count	16_H	
TPC_1	Port 1 Transmit Packet Count	17_H	
TPC_2	Port 2 Transmit Packet Count	18_H	
TPC_3	Port 3 Transmit Packet Count	19_H	
TPC_4	Port 4 Transmit Packet Count	$1A_H$	
TPC_5	Port 5 Transmit Packet Count	$1B_H$	
TPC_6	Port 6 Transmit Packet Count	$1C_H$	
TPC_7	Port 7 Transmit Packet Count	$1D_H$	
TPC_8	Port 8 Transmit Packet Count	$1E_H$	
TPBC_0	Port 0 Transmit Packet Byte Count	$1F_H$	
TPBC_1	Port 1 Transmit Packet Byte Count	20_H	
TPBC_2	Port 2 Transmit Packet Byte Count	21_H	
TPBC_3	Port 3 Transmit Packet Byte Count	22_H	
TPBC_4	Port 4 Transmit Packet Byte Count	23_H	
TPBC_5	Port 5 Transmit Packet Byte Count	24_H	
TPBC_6	Port 6 Transmit Packet Byte Count	25_H	
TPBC_7	Port 7 Transmit Packet Byte Count	26_H	

Table 18 Port Registers (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
TPBC_8	Port 8 Transmit Packet Byte Count	27_H	
CC_0	Port 0 Collision Count	28_H	
CC_1	Port 1 Collision Count	29_H	
CC_2	Port 2 Collision Count	$2A_H$	
CC_3	Port 3 Collision Count	$2B_H$	
CC_4	Port 4 Collision Count	$2C_H$	
CC_5	Port 5 Collision Count	$2D_H$	
CC_6	Port 6 Collision Count	$2E_H$	
CC_7	Port 7 Collision Count	$2F_H$	
CC_8	Port 8 Collision Count	30_H	
EC_0	Port 0 Error Count	31_H	
EC_1	Port 1 Error Count	32_H	
EC_2	Port 2 Error Count	33_H	
EC_3	Port 3 Error Count	34_H	
EC_4	Port 4 Error Count	35_H	
EC_5	Port 5 Error Count	36_H	
EC_6	Port 6 Error Count	37_H	
EC_7	Port 7 Error Count	38_H	
EC_8	Port 8 Error Count	39_H	

Over Flow Flag 0 Register

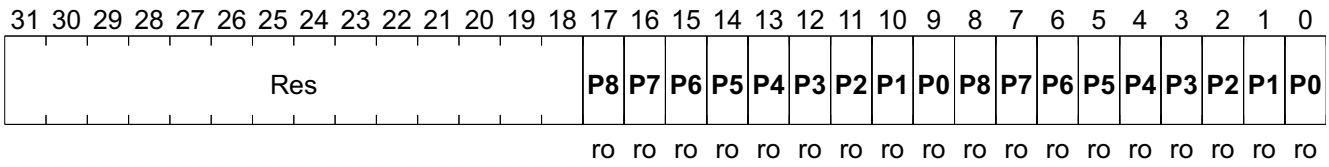
OFFR_0	Offset	Reset Value
Over Flow Flag 0 Register	$3A_H$	$0000\ 0000_H$



Field	Bits	Type	Description
P8	17	ro	**Overflow of Port Receive Packet Byte Count**
P7	16	ro	
P6	15	ro	
P5	14	ro	
P4	13	ro	
P3	12	ro	
P2	11	ro	
P1	10	ro	
P0	9	ro	
P8	8	ro	**Overflow of Port Receive Packet Count**
P7	7	ro	
P6	6	ro	
P5	5	ro	
P4	4	ro	
P3	3	ro	
P2	2	ro	
P1	1	ro	
P0	0	ro	

Over Flow Flag 1 Register

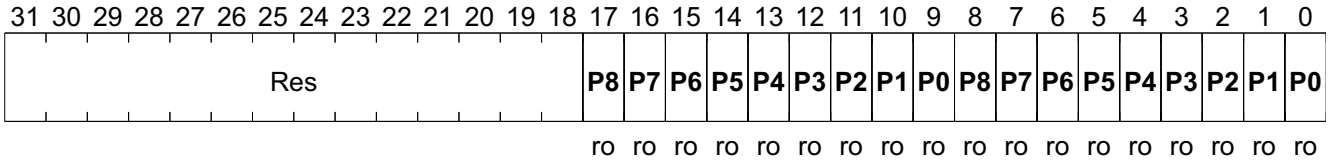
OFFR_1	Offset	Reset Value
Over Flow Flag 1 Register	$3B_H$	$0000\ 0000_H$



Field	Bits	Type	Description
P8	17	ro	**Overflow of Port Transmit Packet Byte Count**
P7	16	ro	
P6	15	ro	
P5	14	ro	
P4	13	ro	
P3	12	ro	
P2	11	ro	
P1	10	ro	
P0	9	ro	
P8	8	ro	**Overflow of Port Transmit Packet Count**
P7	7	ro	
P6	6	ro	
P5	5	ro	
P4	4	ro	
P3	3	ro	
P2	2	ro	
P1	1	ro	
P0	0	ro	

Over Flow Flag 2 Register

OFFR_2	Offset	Reset Value
Over Flow Flag 2 Register	$3C_H$	$0000\ 0000_H$



Field	Bits	Type	Description
P8	17	ro	**Overflow of Port Error Count**
P7	16	ro	
P6	15	ro	
P5	14	ro	
P4	13	ro	
P3	12	ro	
P2	11	ro	
P1	10	ro	
P0	9	ro	
P8	8	ro	**Overflow of Port Collision Count**
P7	7	ro	
P6	6	ro	
P5	5	ro	
P4	4	ro	
P3	3	ro	
P2	2	ro	
P1	1	ro	
P0	0	ro	

4.2 Serial Interface Timing

ADM6999/X serial chip internal counter or EEPROM access timing.

- EESK: Similar as MDC signal
- EDI: Similar as MDIO
- ECS: Must keep low

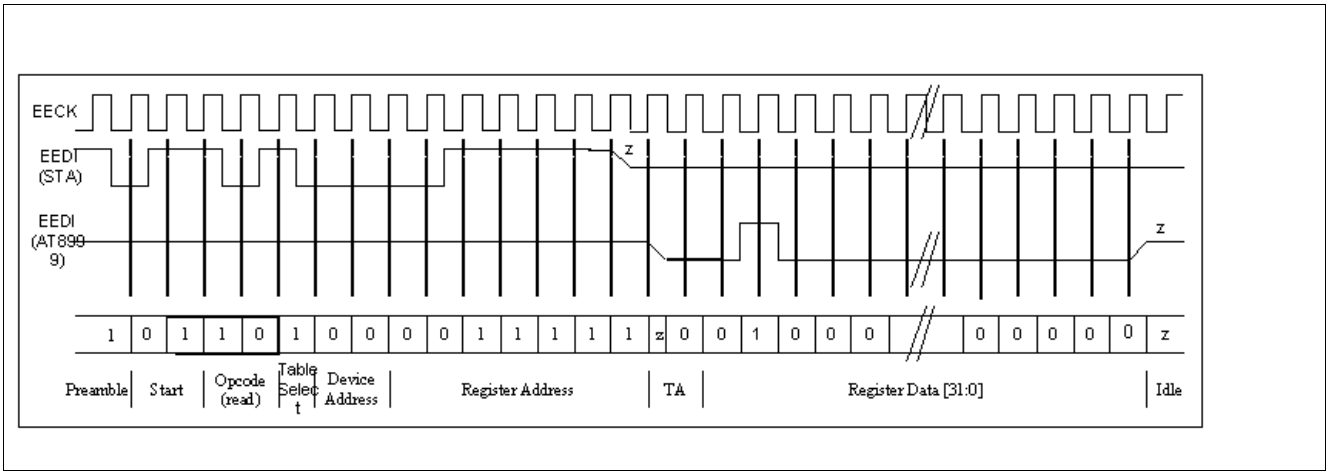


Figure 11 Serial Interface Timing X

- Preamble: At least 32 continuous 1
- Start: 01 (2 bits)
- Opcode: 10 (2 bits, Only supports read command)
- Table select: 1/Counter, 0/ EEPROM (1 bit)
- Register Address: Read Target register address (7 bits)
- TA: Turn Around
- Register Data: 32 bit data
- Counter output bit sequence is bit 31 to bit 0

If user read EEPROM then 32 bits data will be separated in two EEPROM registers. The sequence is:

- Register + 1, Register (Register is even number)
- Register, Register - 1(Register is Odd number)
- Example: Read Register 00h then ADM6999/X will drive 01_H & 00_H
- Read Register 03h then ADM6999/X will drive 03_H & 02_H
- Idle: EESK must send at least one clock at idle time

ADM6999/X issue Reset internal counter command

- EESK: Similar as MDC signal
- EDI: Similar as MDIO
- ECS: Must keep low

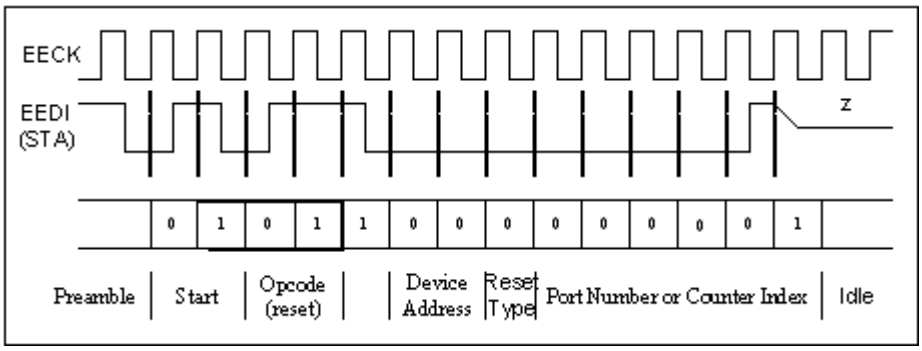


Figure 12 Serial Interface Timing Y

- Preamble: At least 32 continuous “1”
- Start: 01 (2 bits)
- Opcode: 01 (2 bits, Reset command)
- Device Address: Chip physical address as PHYAS[1:0]
- Reset_type: Reset counter by port number or by counter index
  - 1: Clear dedicate port’s all counters
  - 0: Clear dedicate counter
- Port_number or counter index: User defines clear port or counter
- Idle: EECK must send at least one clock at idle time

5 TX/FX Interface

5.1 TP Interface

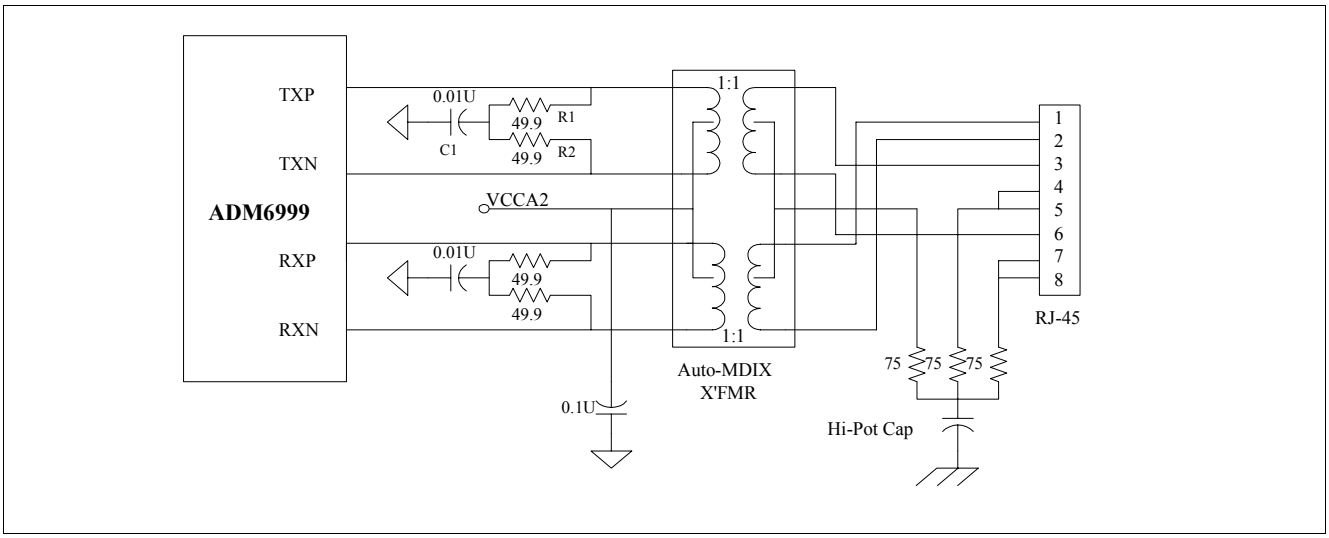


Figure 13 TP Interface

Transformer requirement:

- TX/RX rate 1:1
- TX/RX central tap connect together to VCCA2.

User can change TX/RX pin for easy layout but do not change polarity. ADM6999/X supports auto polarity on receiving side.

5.2 FX Interface

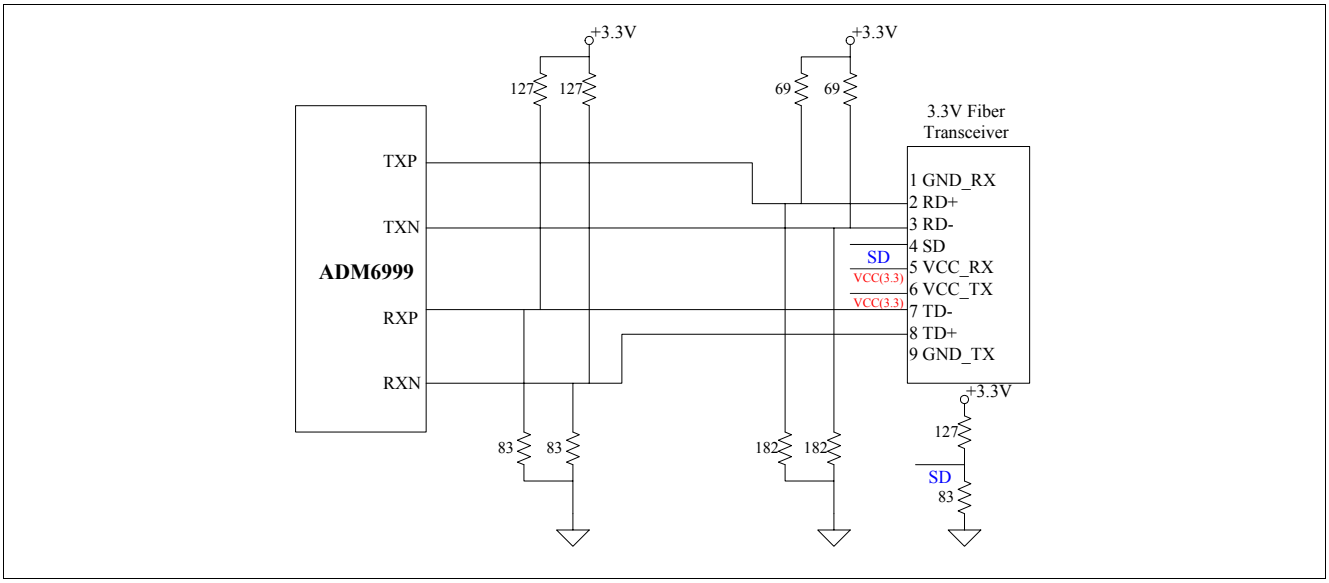


Figure 14 FX Interface

6 DC Characteristics

Table 19 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Supply	V_{CC}	-0.3	–	3.63	V	–
TX line driver	V_{cca2}	–	–	1.8	V	–
PLL voltage	V_{ccpll}	–	–	1.8	V	–
Digital core voltage	V_{ccik}	–	–	1.8	V	–
Input Voltage	V_{IN}	-0.3	–	V_{CC} + 0.3	V	–
Output Voltage	V_{out}	-0.3	–	V_{CC} + 0.3	V	–
Storage Temperature	T_{STG}	-55	–	155	°C	–
Power Dissipation	PD	–	–	1.8	W	–
ESD Rating	ESD	–	–	2 kV	V	–

Table 20 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Supply	V_{CC}	2.8	3.3	3.465	V	–
TX line driver	V_{cca2}	1.7	1.8	1.9	V	–
PLL voltage	V_{ccpll}	1.7	1.8	1.9	V	–
Digital core voltage	V_{ccik}	1.7	1.8	1.9	V	–
Input Voltage	V_{in}	0	–	V_{CC}	V	–
Power consumption	PC	–	1.8	–	W	–
Junction Operating Temperature	T_j	0	25	115	°C	–

Table 21 DC Electrical Characteristics for 3.3 V Operation[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Low Voltage	V_{IL}	–	–	0.3 * V_{CC}	V	CMOS
Input High Voltage	V_{IH}	0.7 * V_{CC}	–	–	V	CMOS
Output Low Voltage	V_{OL}	–	–	0.4	V	CMOS
Output High Voltage	V_{OH}	0.7 * V_{CC}	–	–	V	CMOS
Input Pull-up/down Resistance	R_I	–	100	–	kΩ	V_{IL} = 0 V or V_{IH} = V_{CC}

1) (under V_{CC} = 3.0 V ~ 3.6 V, T_j = 0 °C ~ 115 °C)

7 AC Characteristics

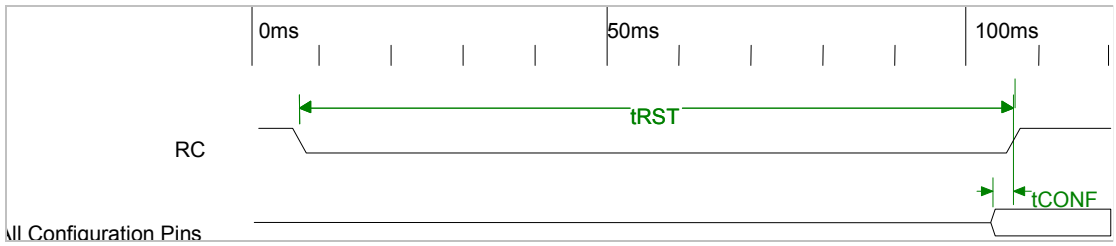


Figure 15 Power On Reset

Table 22 Power On Reset

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RST Low Period	T_{RST}	100	–	–	ms	–
Start of Idle Pulse Width	T_{CONF}	100	–	–	ns	–

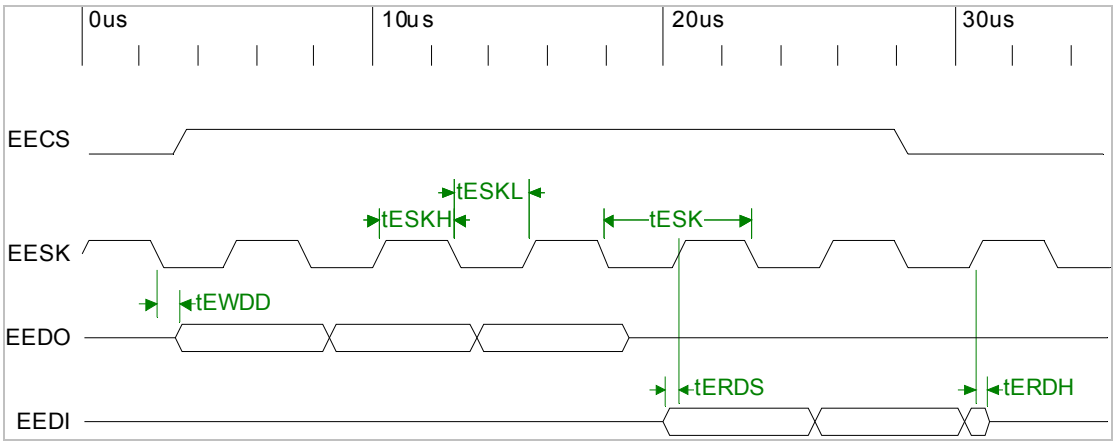


Figure 16 EEPROM Data Timing

Table 23 EEPROM Data Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EESK Period	T_{ESK}	–	5120	–	ns	–
EESK Low Period	T_{ESKL}	2550	–	2570	ns	–
EESK High Period	T_{ESKH}	2550	–	2570	ns	–
EEDI to EESK Rising Setup Time	T_{ERDS}	10	–	–	ns	–

Table 23 EEPROM Data Timing (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EEDI to EESK Rising Hold Time	T_{ERDH}	10	–	–	ns	–
EESK Falling to EEDO Output Delay Time	T_{EWDD}	–	–	20	ns	–

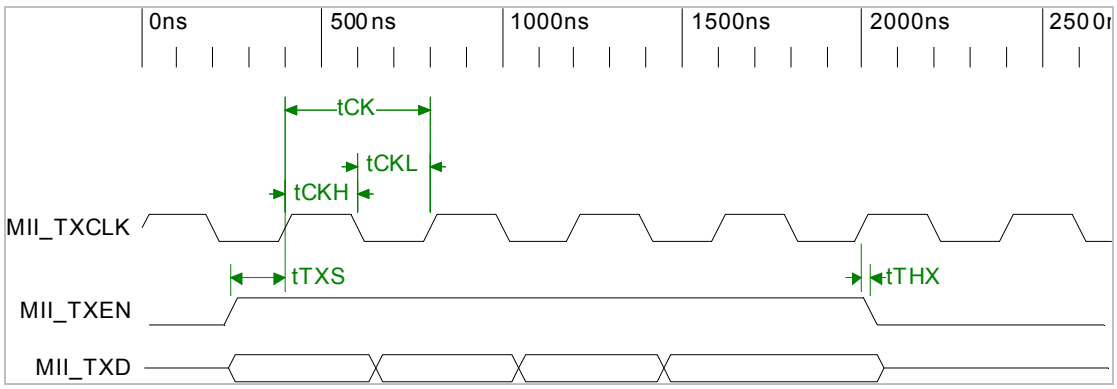


Figure 17 10Base-TX MII Input Timing

Table 24 10Base-TX MII Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_TXCLK Period	T_{CK}	–	400	–	ns	–
MII_TXCLK Low Period	T_{CKL}	160	–	240	ns	–
MII_TXCLK High Period	T_{CKH}	160	–	240	ns	–
MII_TXD, MII_TXEN to MII_TXCLK Rising Setup Time	T_{TXS}	10	–	–	ns	–
MII_TXD, MII_TXEN to MII_TXCLK Rising Hold Time	T_{TXH}	10	–	–	ns	–

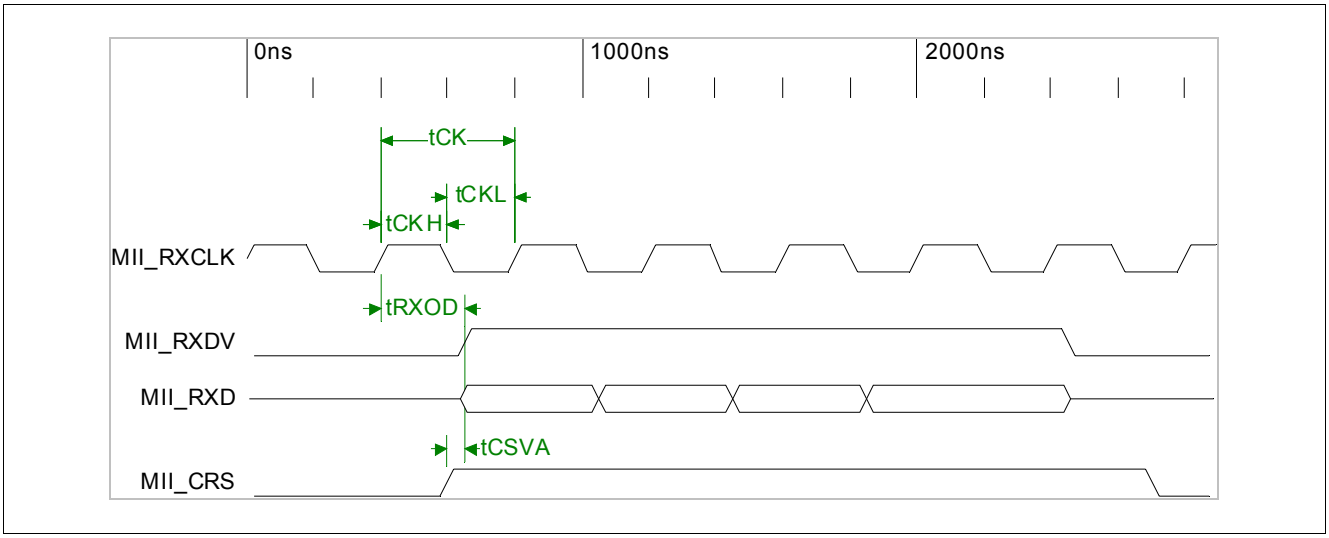


Figure 18 10Base-TX MII Output Timing

Table 25 10Base-TX MII Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_RXCLK Period	T_{CK}	–	400	–	ns	–
MII_RXCLK Low Period	T_{CKL}	160	–	240	ns	–
MII_RXCLK High Period	T_{CKH}	160	–	240	ns	–
MII_CRS Rising to MII_RXDV Rising	T_{CSVA}	0	–	10	ns	–
MII_RXCLK Rising to MII_RXD, MII_RXDV, MII_CRS Output Delay	T_{RXOD}	200	–	–	ns	–

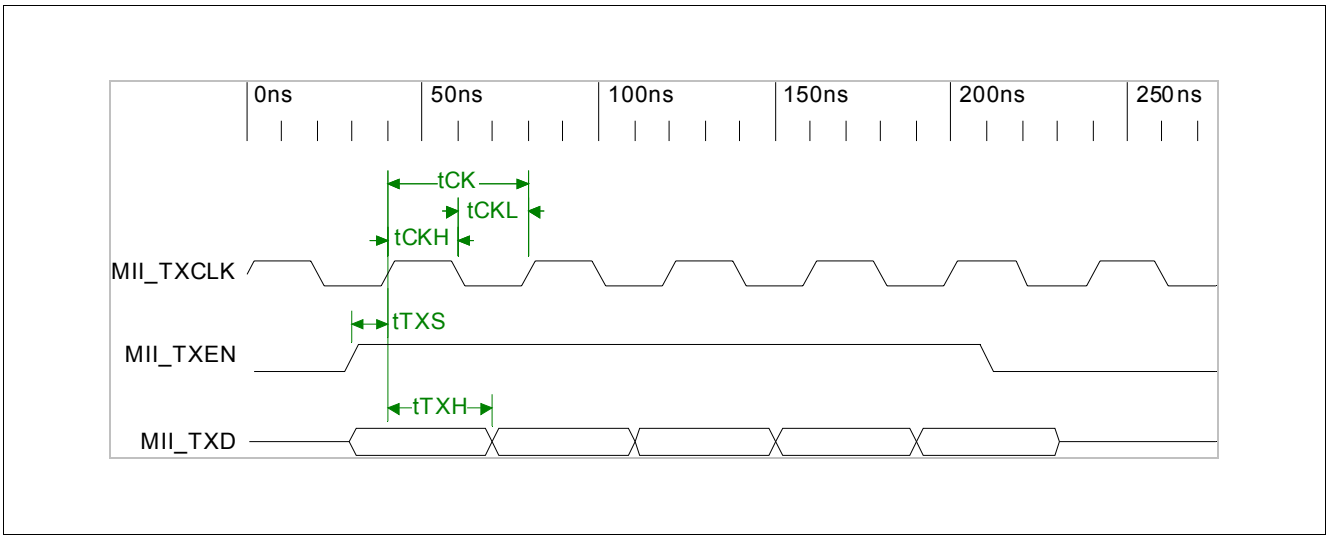


Figure 19 100Base-TX MII Input Timing

Table 26 100Base-TX MII Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_TXCLK Period	T_{CK}	–	40	–	ns	–
MII_TXCLK Low Period	T_{CKL}	16	–	24	ns	–
MII_TXCLK High Period	T_{CKH}	16	–	24	ns	–
MII_TXD, MII_TXEN to MII_TXCLK Rising Setup Time	T_{TXS}	10	–	–	ns	–
MII_TXD, MII_TXEN to MII_TXCLK Rising Hold Time	T_{TXH}	10	–	–	ns	–

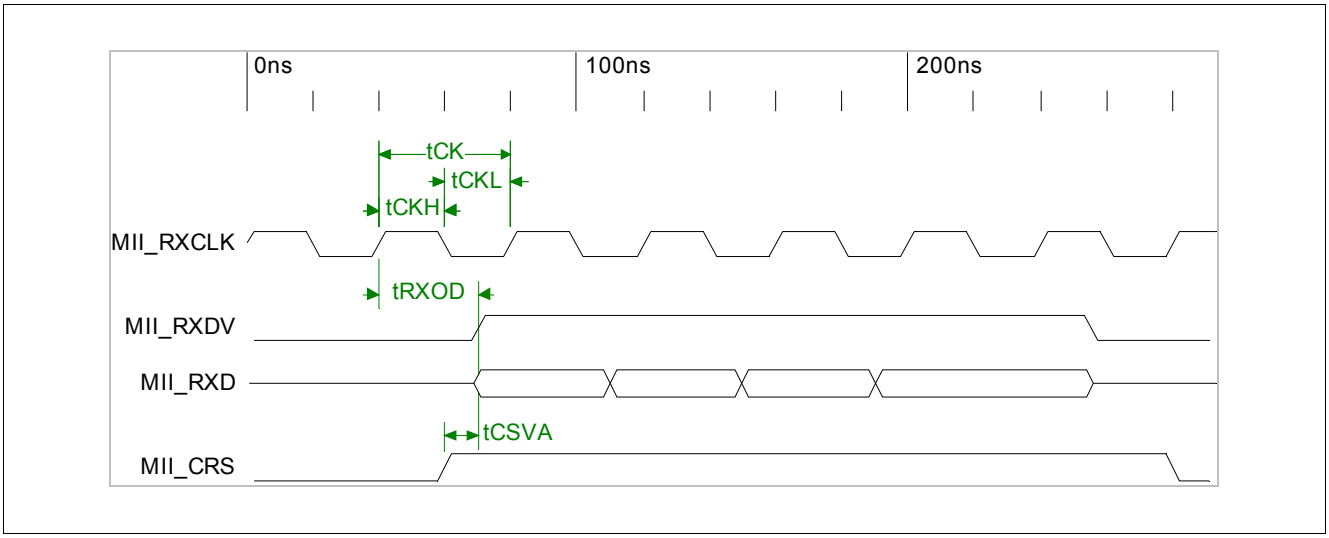


Figure 20 100Base-TX MII Output Timing

Table 27 100Base-TX MII Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_RXCLK Period	T_{CK}	–	40	–	ns	–
MII_RXCLK Low Period	T_{CKL}	16	–	24	ns	–
MII_RXCLK High Period	T_{CKH}	16	–	24	ns	–
MII_CRS Rising to MII_RXDV Rising	T_{CSVA}	0	–	10	ns	–
MII_RXCLK Rising to MII_RXD, MII_RXDV, MII_CRS Output Delay	T_{RXOD}	20	–	30	ns	–

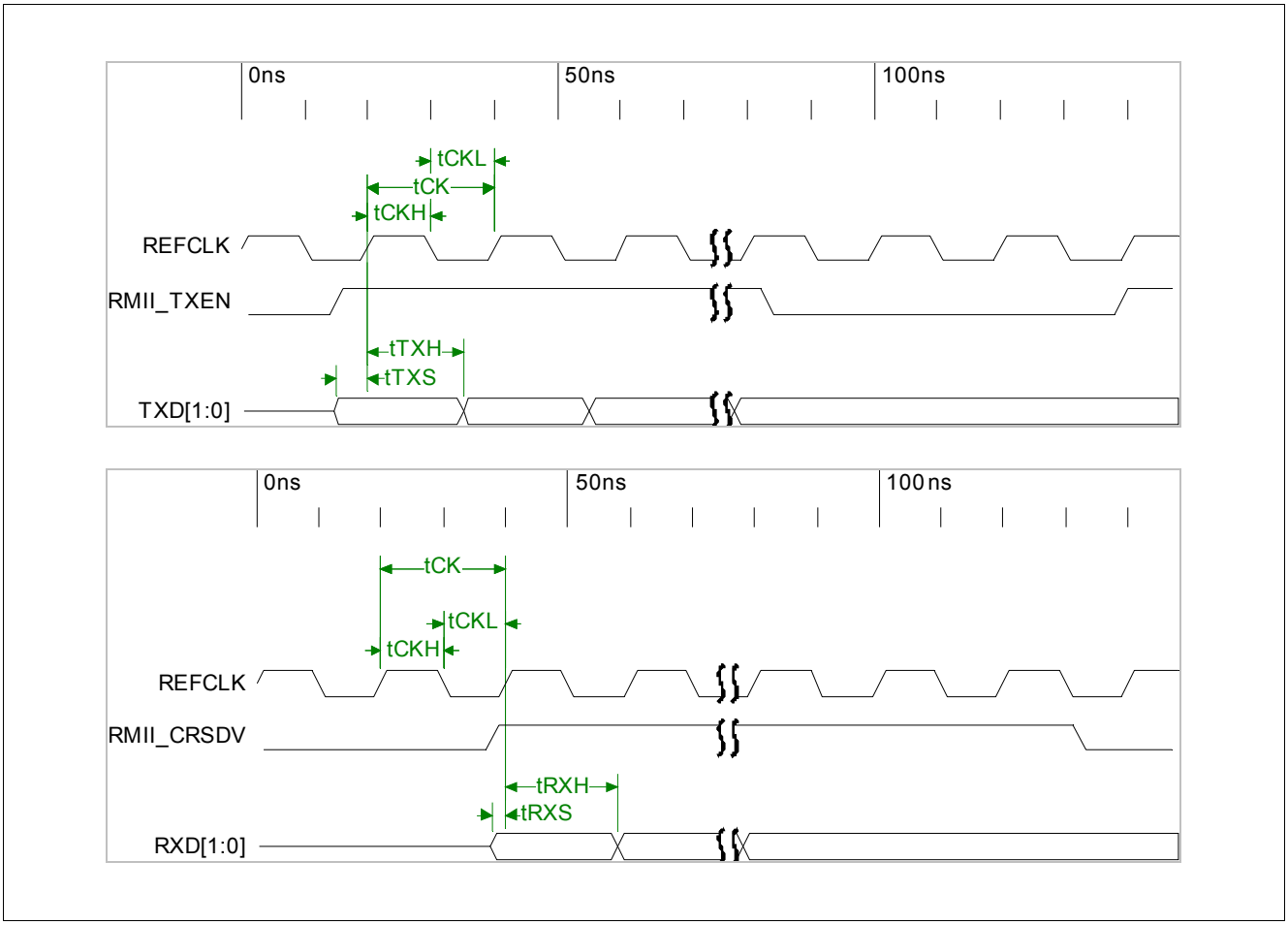


Figure 21 Reduce MII Timing

Table 28 Reduce MII Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RMII_REFCLK Period	T_{CK}	–	20	–	ns	–
RMII_REFCLK Low Period	T_{CKL}	–	10	–	ns	–
RMII_REFCLK High Period	T_{CKH}	–	10	–	ns	–
TXEN, TXD to REFCLK rising setup time	T_{TXS}	4	–	–	ns	–
TXE, TXD to REFCLK rising hold time	T_{TXH}	2	–	–	ns	–
CSRDV, RXD to REFCLK rising setup time	T_{RXS}	4	–	–		–
CRSDV, RXD to REFCLK rising hold time	T_{RXH}	2	–	–		–

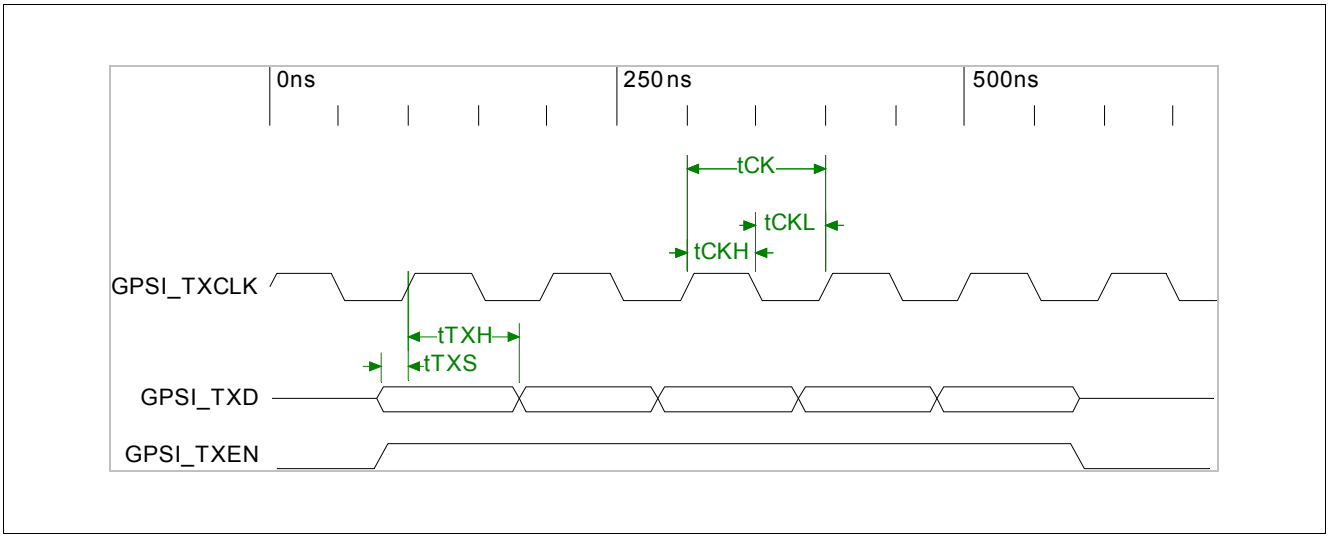


Figure 22 GPSI (7-wire) Input Timing

Table 29 GPSI (7-wire) Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
GPSI_TXCLK Period	T_{CK}	–	100	–	ns	–
GPSI_TXCLK Low Period	T_{CKL}	40	–	60	ns	–
GPSI_TXCLK High Period	T_{CKH}	40	–	60	ns	–
GPSI_TXD, GPSI_TXEN to GPSI_TXCLK Rising Setup Time	T_{TXS}	10	–	–	ns	–
GPSI_TXD, GPSI_TXEN to GPSI_TXCLK Rising Hold Time	T_{TXH}	10	–	–	ns	–

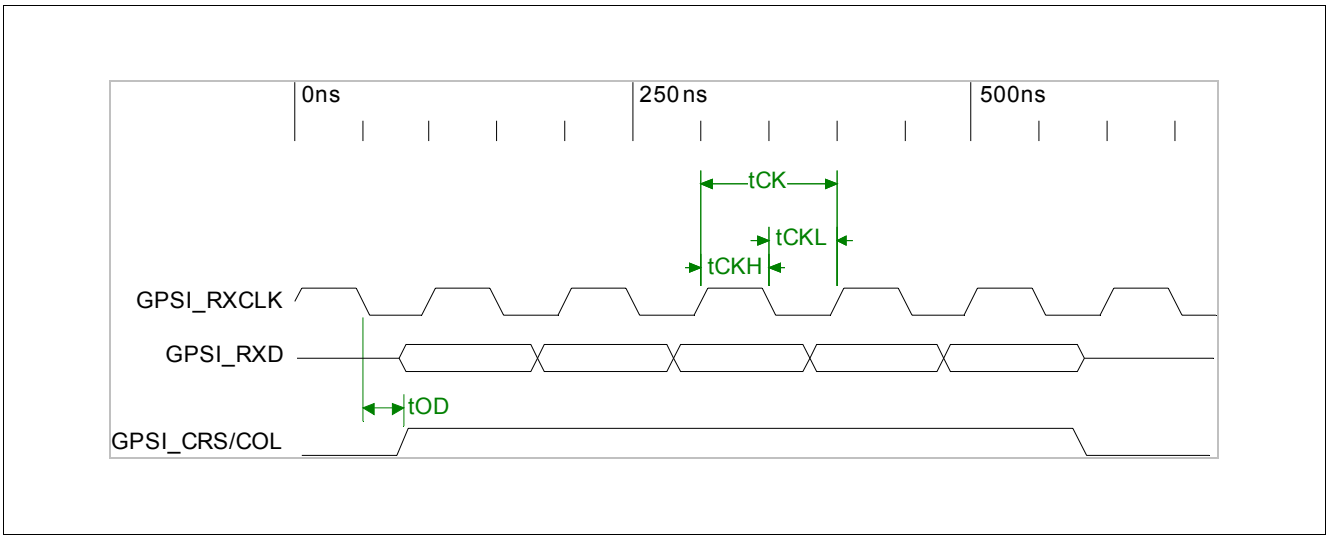


Figure 23 GPSI (7-wire) Output Timing

Table 30 GPSI (7-wire) Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
GPSI_RXCLK Period	T_{CK}	–	100	–	ns	–
GPSI_RXCLK Low Period	T_{CKL}	40	–	60	ns	–
GPSI_RXCLK High Period	T_{CKH}	40	–	60	ns	–
GPSI_RXCLK Rising to GPSI_CRS/GPSI_COL Output Delay	T_{OD}	50	–	70	ns	–

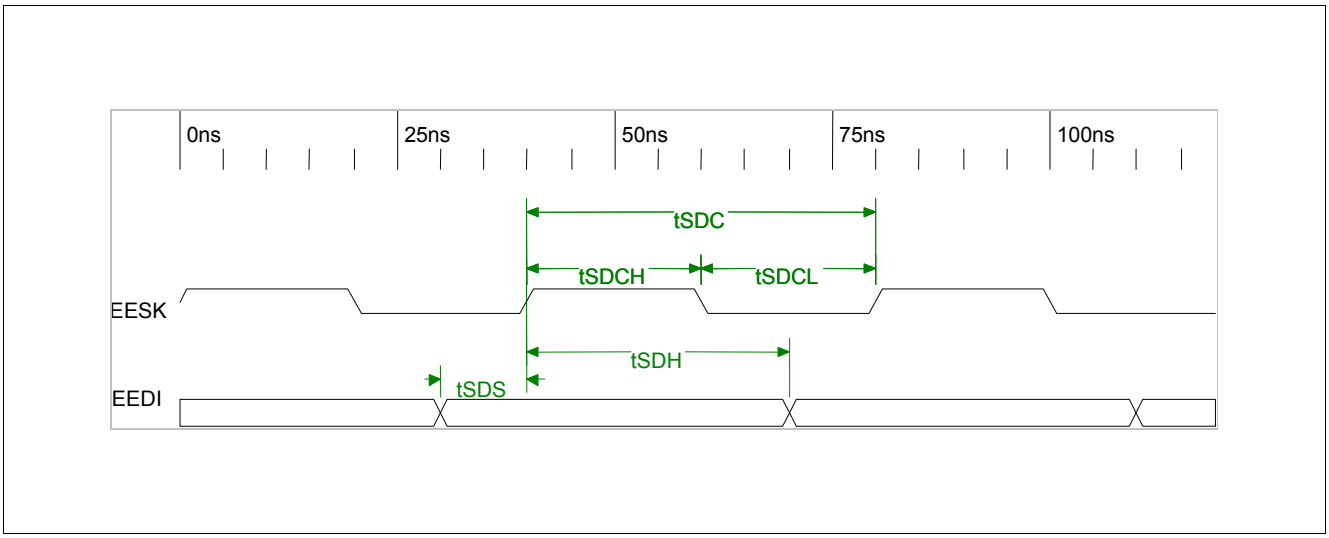


Figure 24 SMI Timing

Table 31 SMI Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EESK Period	T_{CK}	20	–	–	ns	–
EESK Low Period	T_{CKL}	10	–	–	ns	–
EESK High Period	T_{CKH}	10	–	–	ns	–
EEDI to EESK rising setup time on read/write cycle	T_{SDS}	4	–	–	ns	–
EEDI to EESK rising hold time on read/write cycle	T_{SDH}	2	–	–	ns	–

8 Package Outlines

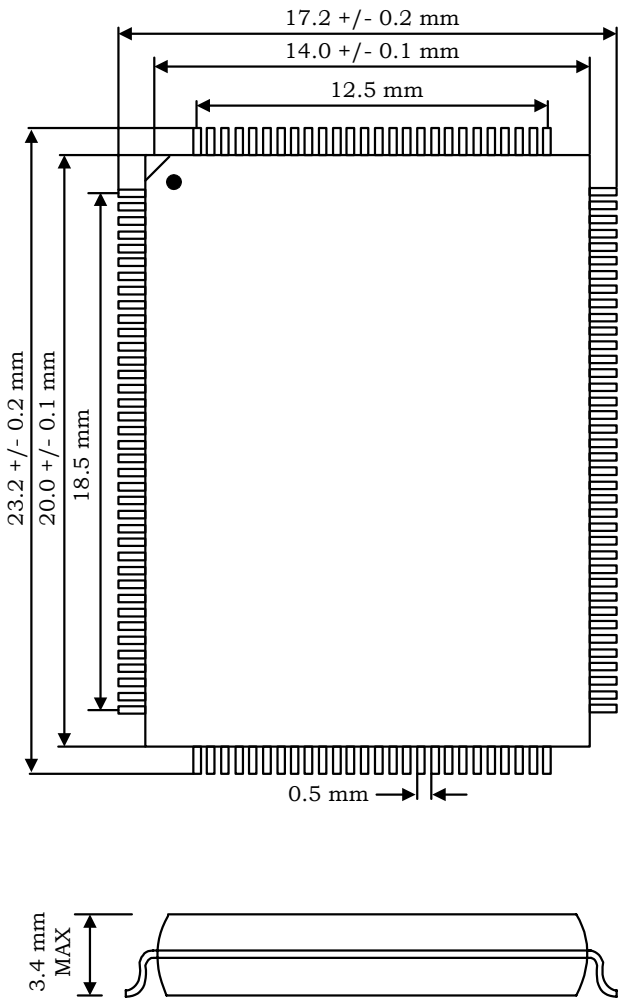


Figure 25 128 Pin PQFP Package

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