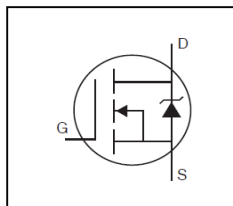


Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to T_{jmax}
- Lead-Free, RoHS Compliant
- Automotive Qualified *

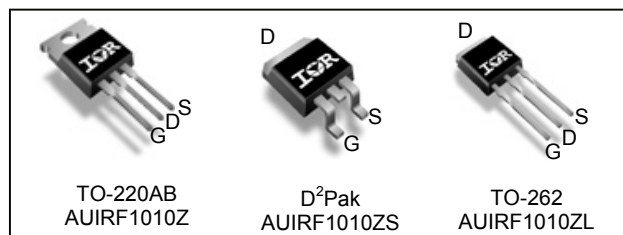


HEXFET® Power MOSFET

V_{DS}	55V
$R_{DS(on)}$ max.	7.5mΩ
I_D (Silicon Limited)	94A
I_D (Package Limited)	75A

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRF1010Z	TO-220	Tube	50	AUIRF1010Z
AUIRF1010ZL	TO-262	Tube	50	AUIRF1010ZL
AUIRF1010ZS	D²-Pak	Tube	50	AUIRF1010ZS
		Tape and Reel Left	800	AUIRF1010ZSTRL

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	94	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	66	
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	75	
I_{DM}	Pulsed Drain Current ①	360	
P_D @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation	140	W
	Linear Derating Factor	0.90	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	130	mJ
E_{AS} (tested)	Single Pulse Avalanche Energy Tested Value ⑥	180	
I_{AR}	Avalanche Current ①	See Fig.15,16, 12a, 12b	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw ⑦	10 lbf•in (1.1N•m)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	—	1.11	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ⑦	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ⑦	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑧	—	40	

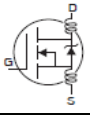
HEXFET® is a registered trademark of Infineon.

*Qualification standards can be found at www.infineon.com

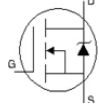
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.049	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	5.8	7.5	m Ω	$V_{GS} = 10V, I_D = 75A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Trans conductance	33	—	—	S	$V_{DS} = 25V, I_D = 75A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 55V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 55V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

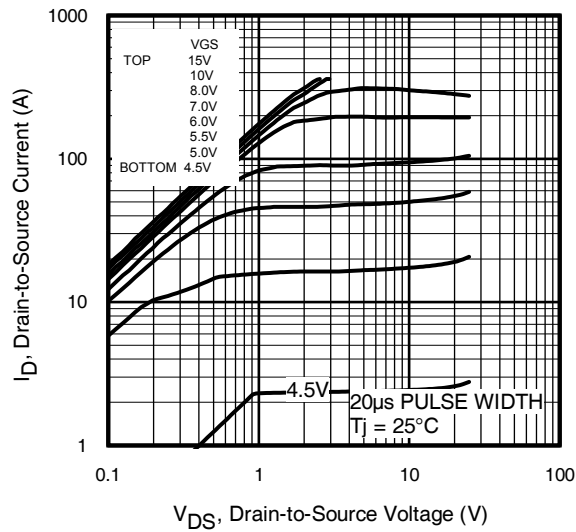
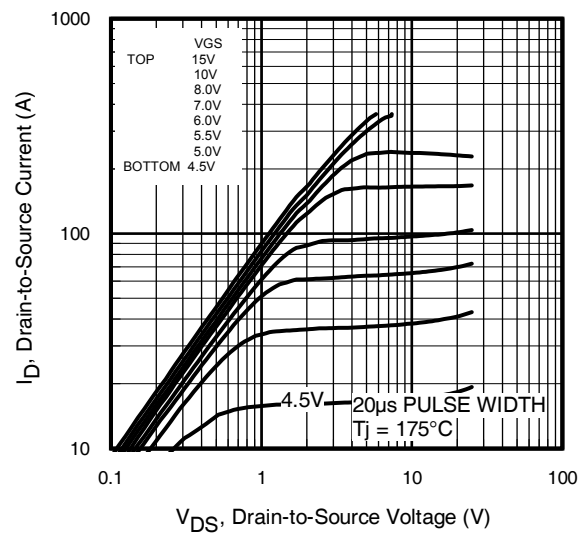
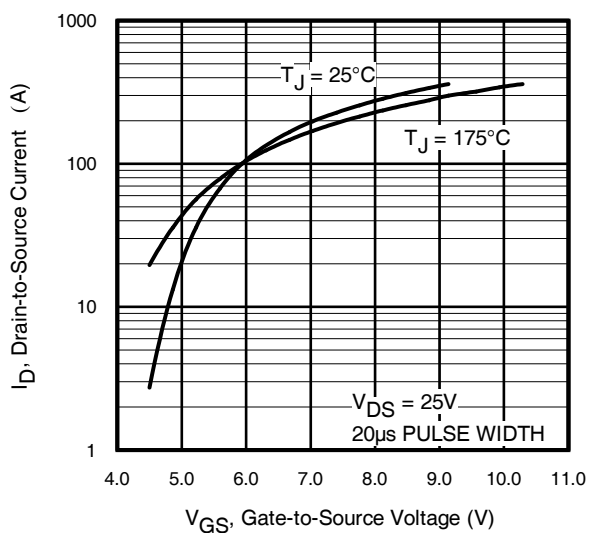
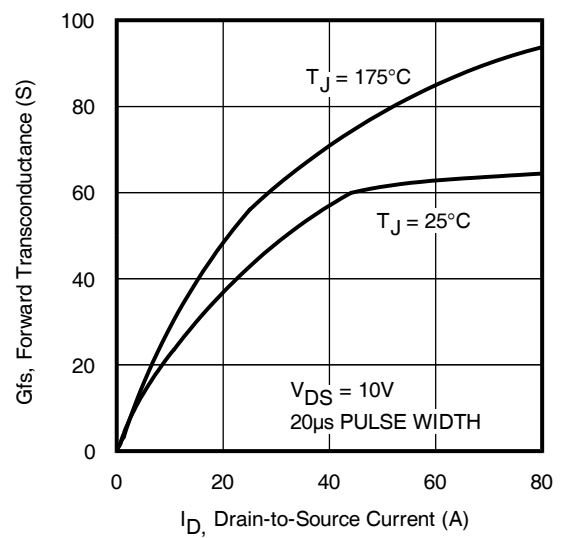
Q_g	Total Gate Charge	—	63	95	nC	$I_D = 75A$
Q_{gs}	Gate-to-Source Charge	—	19	—		$V_{DS} = 44V$
Q_{gd}	Gate-to-Drain Charge	—	24	—		$V_{GS} = 10V$ ③
$t_{d(on)}$	Turn-On Delay Time	—	18	—	ns	$V_{DD} = 28V$
t_r	Rise Time	—	150	—		$I_D = 75A$
$t_{d(off)}$	Turn-Off Delay Time	—	36	—		$R_G = 6.8\Omega$
t_f	Fall Time	—	92	—		$V_{GS} = 10V$ ③
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact :
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	2840	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	420	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	250	—		$f = 1.0\text{MHz}$, See Fig. 5
C_{oss}	Output Capacitance	—	1630	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	360	—		$V_{GS} = 0V, V_{DS} = 44V, f = 1.0\text{MHz}$
$C_{oss\text{ eff.}}$	Effective Output Capacitance	—	560	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 44V$ ④

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	75	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	360		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 75A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	22	33	ns	$T_J = 25^\circ\text{C}, I_F = 75A, V_{DD} = 25V$
Q_{rr}	Reverse Recovery Charge	—	15	23	nC	$di/dt = 100A/\mu s$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.05\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 75A$, $V_{GS} = 10V$. Part not recommended for use above this value.
- ③ Pulse width $\leq 1.0\text{ms}$; duty cycle $\leq 2\%$.
- ④ $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑤ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population, starting $T_J = 25^\circ\text{C}$, $L = 0.05\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 75A$, $V_{GS} = 10V$.
- ⑦ This is only applied to TO-220AB package.
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑨ R_θ is measured at T_J approximately 90°C .


Fig. 1 Typical Output Characteristics

Fig. 2 Typical Output Characteristics

Fig. 3 Typical Transfer Characteristics

Fig. 4 Typical Forward Trans conductance vs. Drain Current

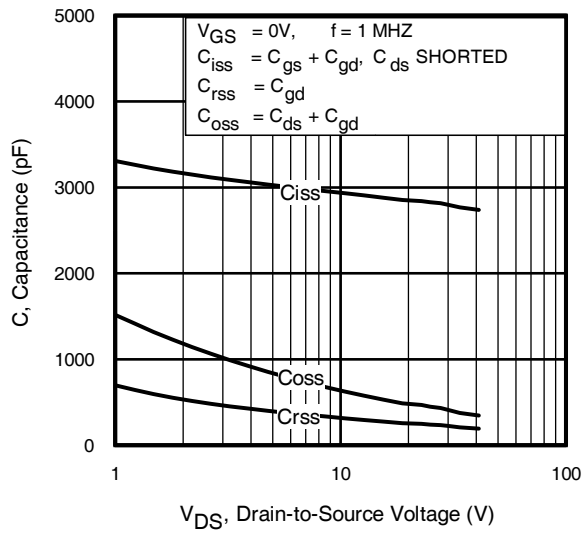


Fig 5. Typical Capacitance vs.
Drain-to-Source Voltage

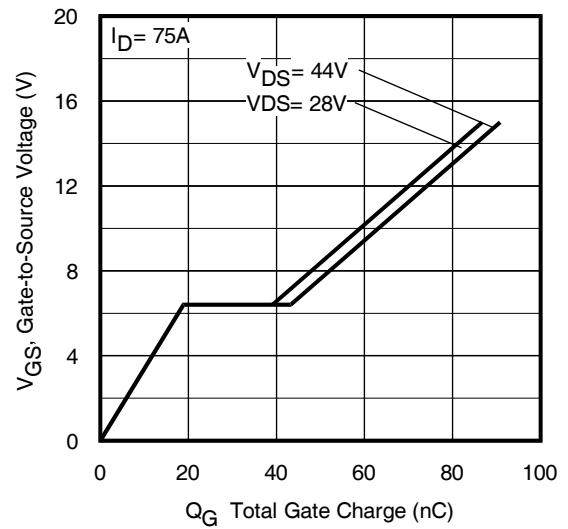


Fig 6. Typical Gate Charge vs.
Gate-to-Source Voltage

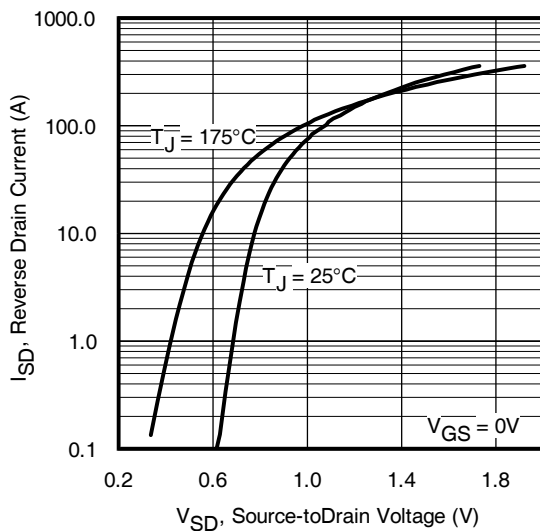


Fig. 7 Typical Source-to-Drain Diode
Forward Voltage

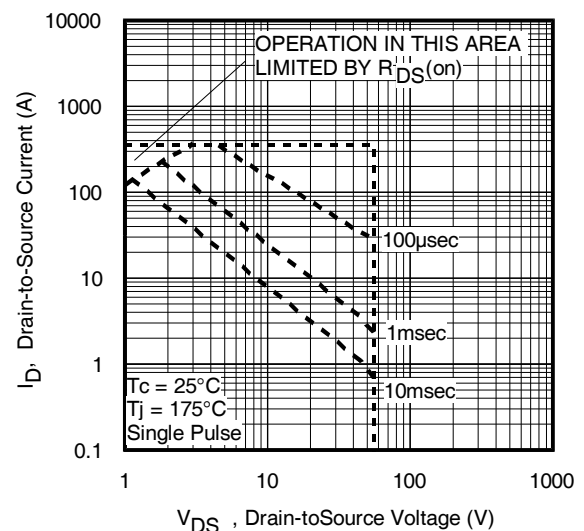
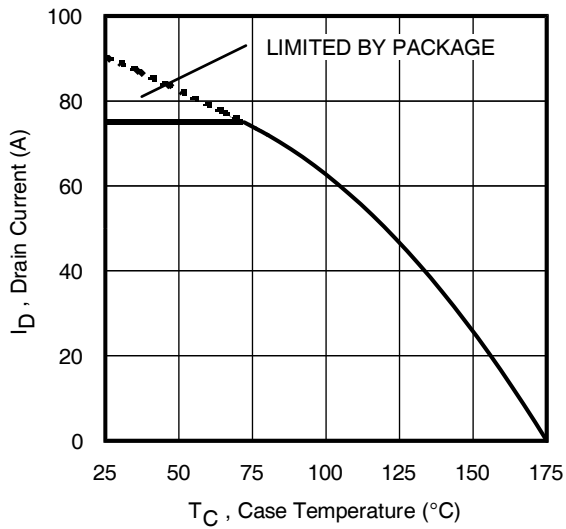
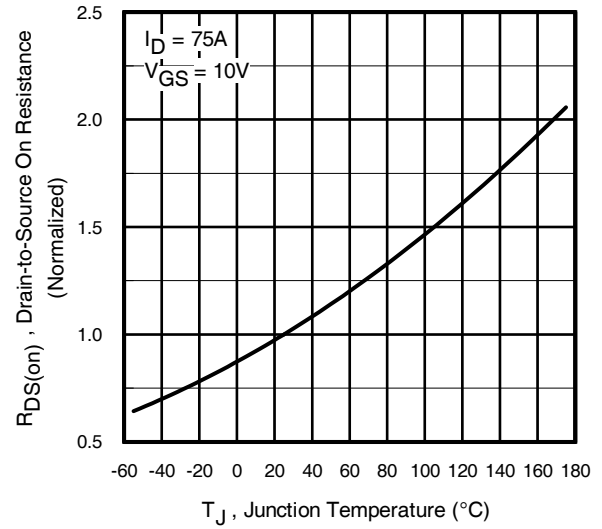
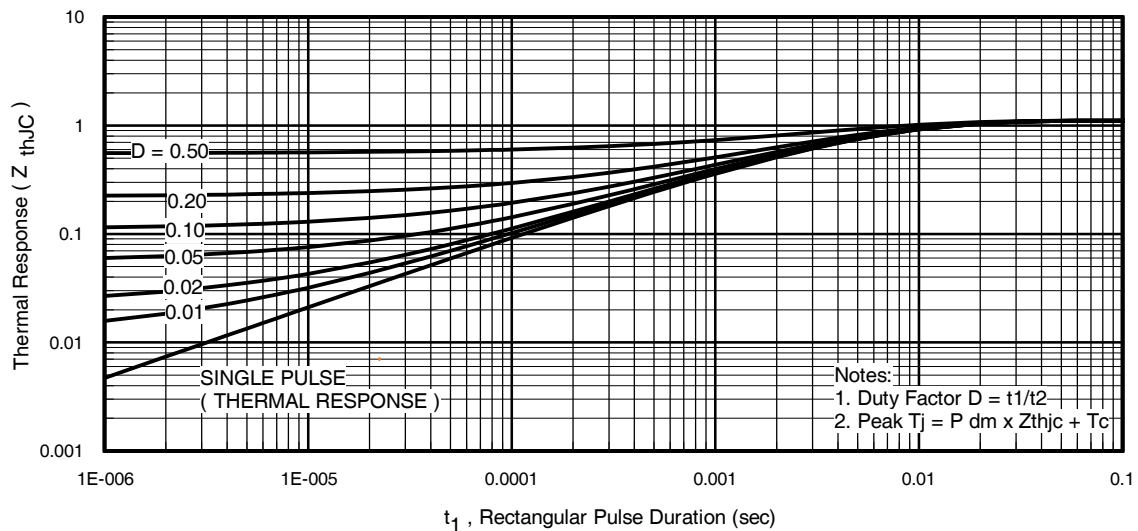
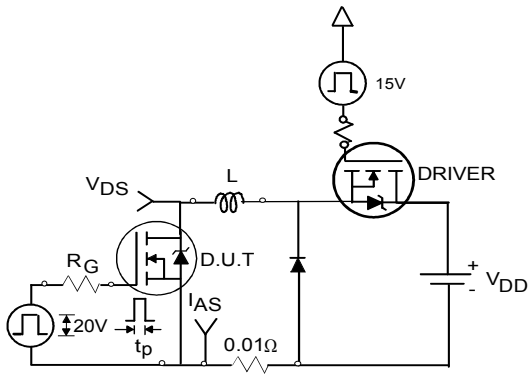
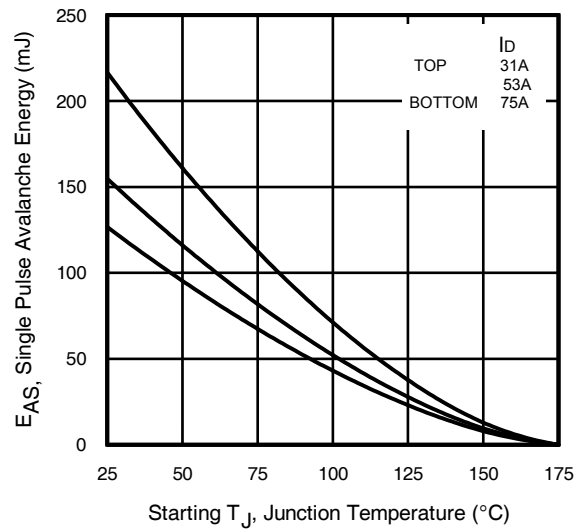
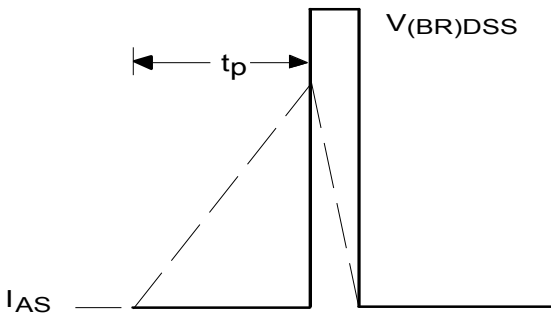
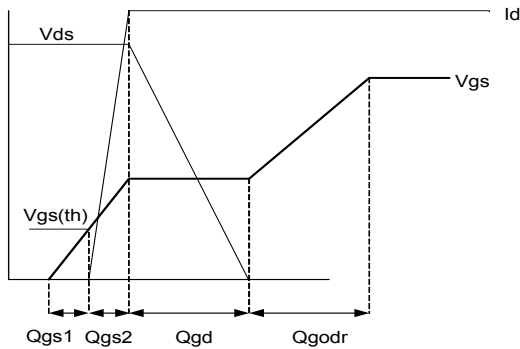
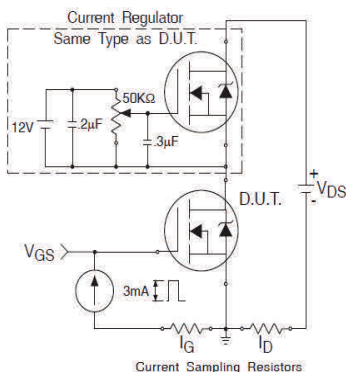
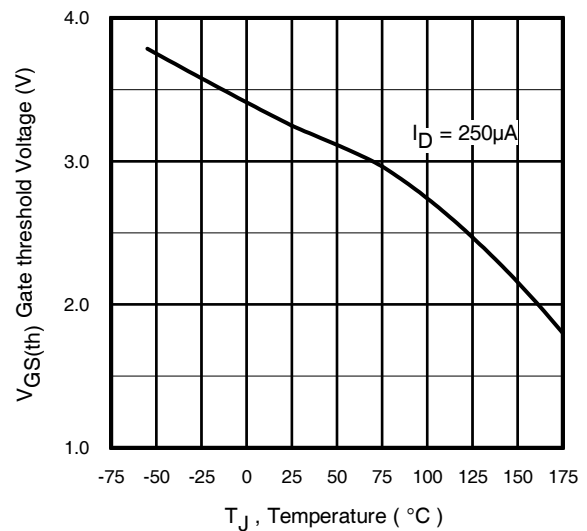


Fig 8. Maximum Safe Operating Area


Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Normalized On-Resistance vs. Temperature

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig 12a. Unclamped Inductive Test Circuit

Fig 12c. Maximum Avalanche Energy vs. Drain Current

Fig 12b. Unclamped Inductive Waveforms

Fig 13a. Gate Charge Waveform

Fig 13b. Gate Charge Test Circuit

Fig 14. Threshold Voltage vs. Temperature

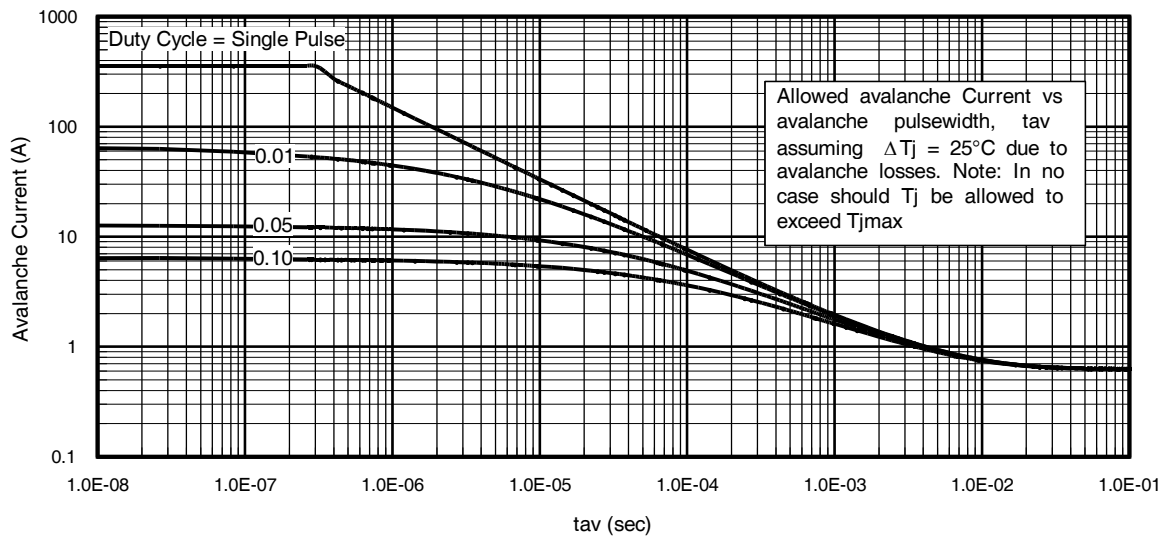


Fig 15. Typical Avalanche Current vs. Pulse width

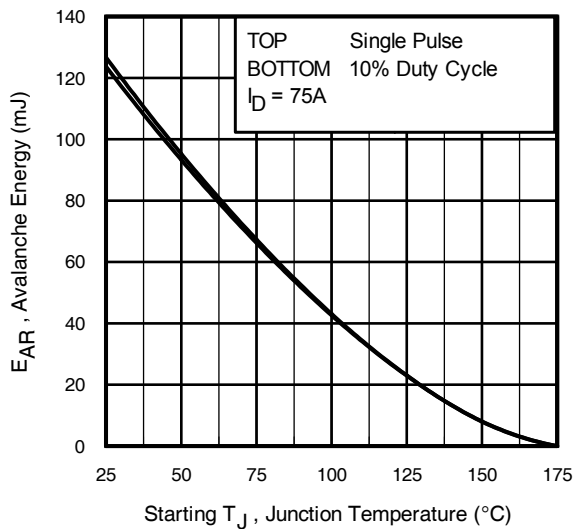


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.infineon.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{thJC}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

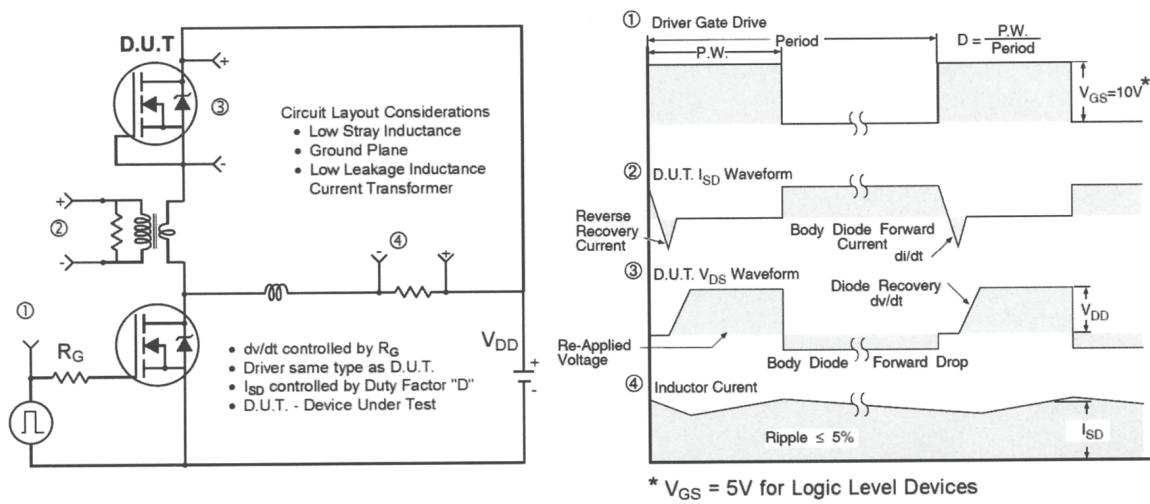


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

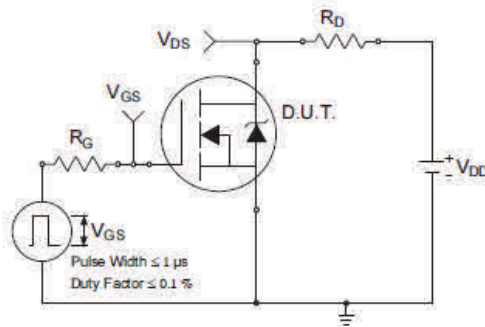


Fig 18a. Switching Time Test Circuit

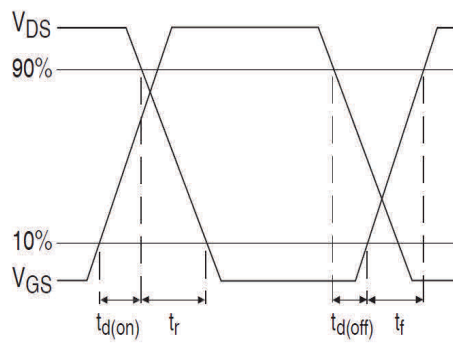


Fig 18b. Switching Time Waveforms

The technical drawings illustrate the design of a probe assembly:

- Top View:** Shows the overall layout with dimensions E , F , G , H , I , J , K , L , M , N , O , P , Q , R , S , T , U , V , W , X , Y , Z . It includes a circular feature with diameter $\Phi 1.01 \pm 0.01$ and a rectangular feature with dimensions 2×0.15 and 0.15 . A "LEAD TIP" is indicated.
- Side View:** Shows the profile of the assembly with dimensions A , $A1$, $A2$, B , $B1$, $B2$, C , D , E , F , G , H , I , J , K , L , M , N , O , P , Q , R , S , T , U , V , W , X , Y , Z . A "SEATING PLANE" is indicated.
- DETAIL B:** A magnified view of the probe tips, showing dimensions 1 , 2 , 3 , 4 , 5 , 6 , 7 , 8 , 9 , 10 , 11 , 12 , 13 , 14 , 15 , 16 , 17 , 18 , 19 , 20 , 21 , 22 , 23 , 24 , 25 , 26 , 27 , 28 , 29 , 30 , 31 , 32 , 33 , 34 , 35 , 36 , 37 , 38 , 39 , 40 , 41 , 42 , 43 , 44 , 45 , 46 , 47 , 48 , 49 , 50 , 51 , 52 , 53 , 54 , 55 , 56 , 57 , 58 , 59 , 60 , 61 , 62 , 63 , 64 , 65 , 66 , 67 , 68 , 69 , 70 , 71 , 72 , 73 , 74 , 75 , 76 , 77 , 78 , 79 , 80 , 81 , 82 , 83 , 84 , 85 , 86 , 87 , 88 , 89 , 90 , 91 , 92 , 93 , 94 , 95 , 96 , 97 , 98 , 99 , 100 .
- Cross-Section C-C & D-D:** Shows the internal structure of the probe base, including "PLATING" and "BASE METAL" layers, with dimensions 1 , 2 , 3 , 4 , 5 , 6 , 7 , 8 , 9 , 10 , 11 , 12 , 13 , 14 , 15 , 16 , 17 , 18 , 19 , 20 , 21 , 22 , 23 , 24 , 25 , 26 , 27 , 28 , 29 , 30 , 31 , 32 , 33 , 34 , 35 , 36 , 37 , 38 , 39 , 40 , 41 , 42 , 43 , 44 , 45 , 46 , 47 , 48 , 49 , 50 , 51 , 52 , 53 , 54 , 55 , 56 , 57 , 58 , 59 , 60 , 61 , 62 , 63 , 64 , 65 , 66 , 67 , 68 , 69 , 70 , 71 , 72 , 73 , 74 , 75 , 76 , 77 , 78 , 79 , 80 , 81 , 82 , 83 , 84 , 85 , 86 , 87 , 88 , 89 , 90 , 91 , 92 , 93 , 94 , 95 , 96 , 97 , 98 , 99 , 100 .

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTACT OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	5
A1	1.14	1.40	.045	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	
b2	1.14	1.78	.045	.070	5
b3	1.14	1.73	.045	.068	
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	7
D2	11.68	12.88	.460	.507	
E	9.65	10.67	.380	.420	
E1	6.86	8.89	.270	.350	7
E2	—	0.76	—	.030	8
e	2.54 BSC		.100 BSC		7,8
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	
ØP	3.54	4.08	.139	.161	3
Q	2.54	3.42	.100	.135	

1.- GATE
2.- DRAIN
3.- SOURCE

IGBTs, CoPACK

1.- GATE
2.- COLLECTOR
3.- EMITTER

DIODES

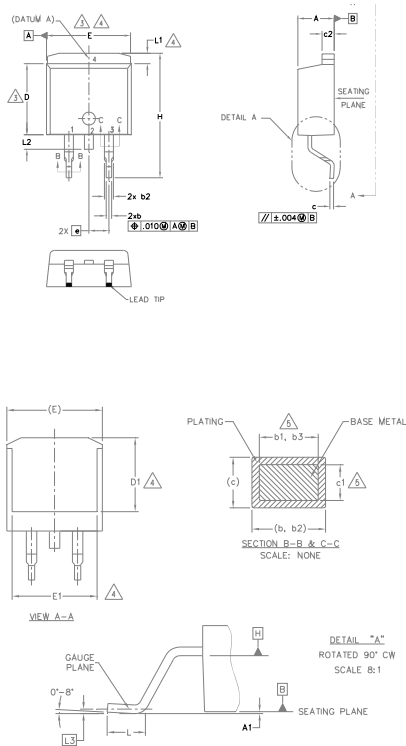
1.- ANODE
2.- CATHODE
3.- ANODE

Diagram illustrating the components of an IOR label:

- Part Number:** AUIRF1010Z
- IR Logo:** IOR
- Date Code:** YWWA
 - Y= Year
 - WW= Work Week
- Lot Code:** XX ● XX

2017-09-18

D²Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	5
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		4
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	
L2	—	1.78	—	.070	
L3	0.25 BSC		.010 BSC		

LEAD ASSIGNMENTS

DIODES

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2.- CATHODE
- 3.- ANODE

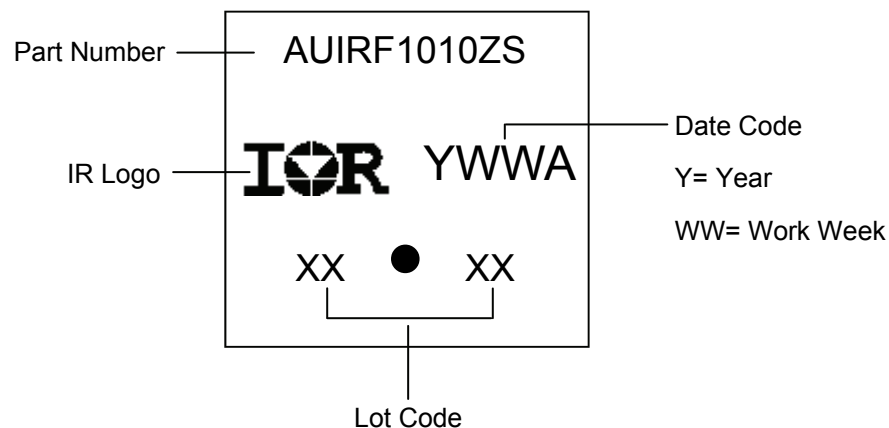
HEXFET

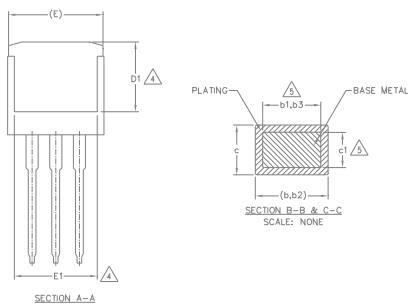
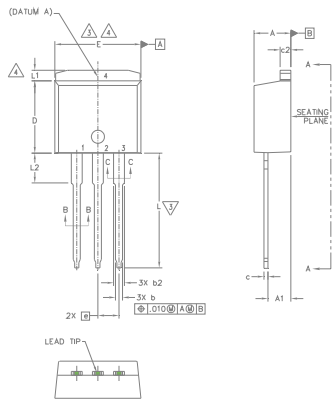
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

D²Pak (TO-263AB) Part Marking Information



TO-262 Package Outline (Dimensions are shown in millimeters (inches))

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS
IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

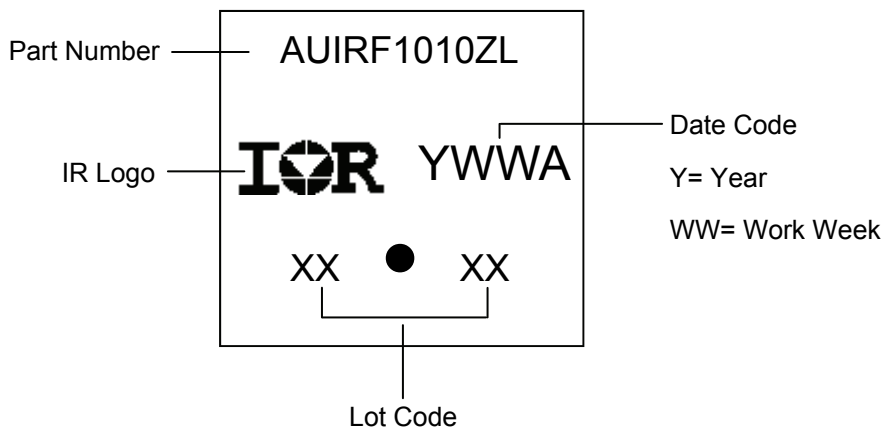
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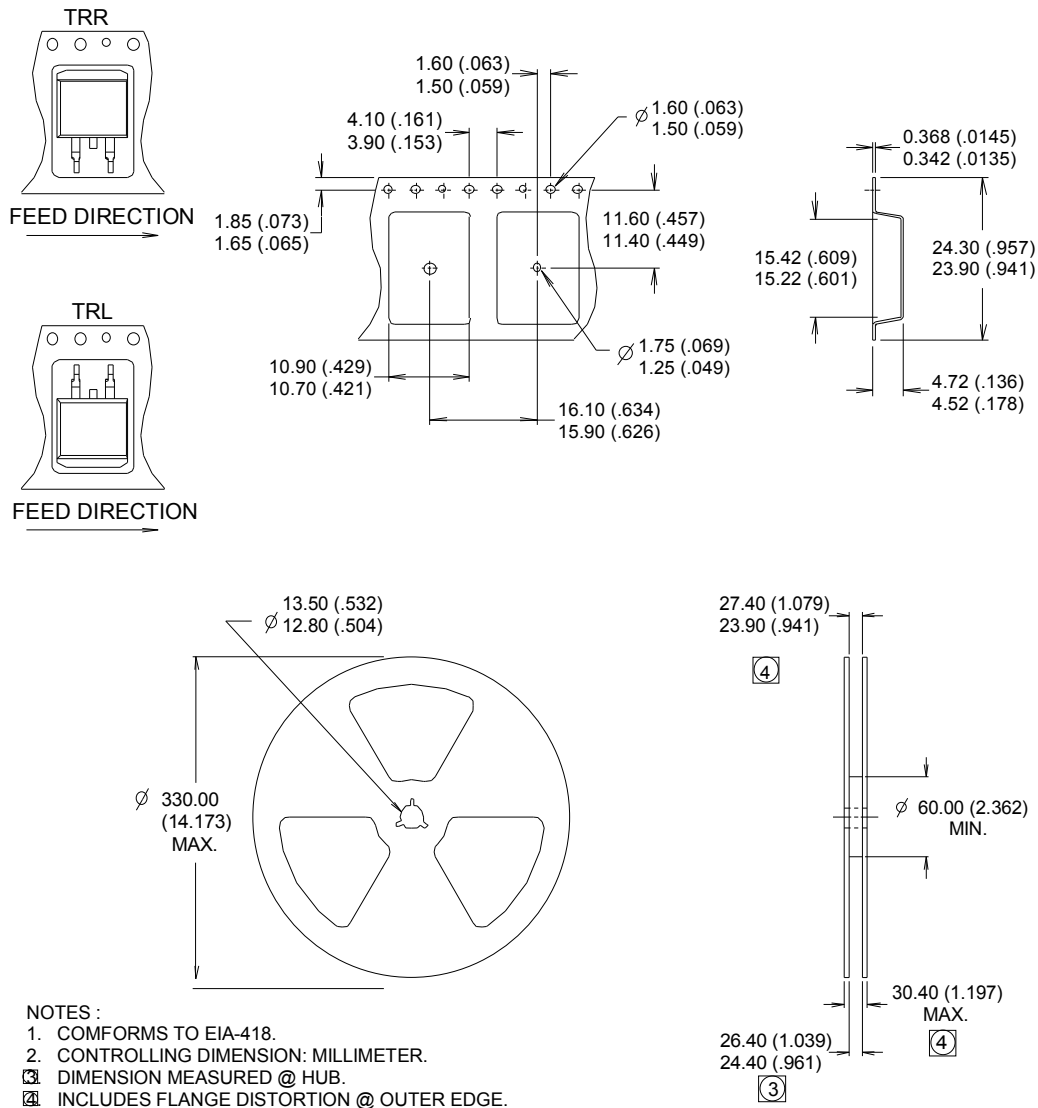
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

DIODES

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.- CATHODE
- 3.- ANODE

SYM BOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	5
b3	1.14	1.73	.045	.068	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	3,4
D	8.38	9.65	.330	.380	
D1	6.86	—	.270	—	
E	9.65	10.67	.380	.420	
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	—	1.65	—	.065	
L2	3.56	3.71	.140	.146	4

TO-262 Part Marking Information


D²Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))


Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		TO-220AB	N/A
		TO-262	MSL1
		D ² -Pak	
ESD	Machine Model	Class M4 (+/- 700V) [†] AEC-Q101-002	
	Human Body Model	Class H1C (+/-1500V) [†] AEC-Q101-001	
	Charged Device Model	Class C5 (+/-2000V) [†] AEC-Q101-005	
RoHS Compliant		Yes	

† Highest passing voltage.

Revision History

Date	Comments
11/6//2015	- Updated datasheet with corporate template - Corrected ordering table on page 1.
9/18/2017	Corrected typo error on part marking on page 9,10,11.

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