

# EFM8 Sleepy Bee Family

## EFM8SB2 Data Sheet



The EFM8SB2, part of the Sleepy Bee family of MCUs, is the world's most energy friendly 8-bit microcontrollers with a comprehensive feature set in small packages.

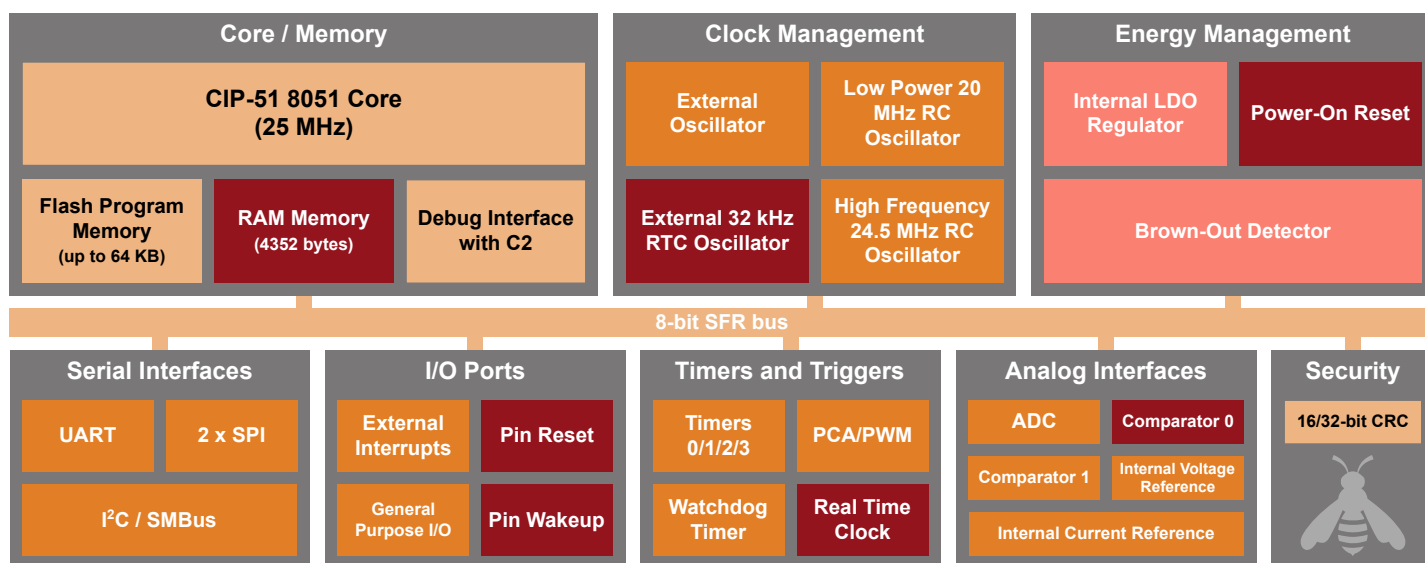
These devices offer lowest power consumption by combining innovative low energy techniques and short wakeup times from energy saving modes into small packages, making them well-suited for any battery operated applications. With an efficient 8051 core, 6-bit current reference, and precision analog, the EFM8SB2 family is also optimal for embedded applications.

EFM8SB2 applications include the following:

- Hand-held devices
- Battery-operated consumer electronics
- Industrial controls
- Sensor interfaces

### ENERGY FRIENDLY FEATURES

- Lowest MCU sleep current with supply brownout detection (50 nA)
- Lowest MCU active current with these features (170  $\mu$ A / MHz at 24.5 MHz clock rate)
- Lowest MCU sleep current using internal RTC operating and supply brownout detection (<300 nA)
- Ultra-fast wake up for digital and analog peripherals (< 2  $\mu$ s)
- Integrated low drop out (LDO) voltage regulator to maintain ultra-low active current at all voltages



Lowest power mode with peripheral operational:

Normal
  Idle
  Suspend
  Sleep

## 1. Feature List

The EFM8SB2 highlighted features are listed below.

- Core:
  - Pipelined CIP-51 Core
  - Fully compatible with standard 8051 instruction set
  - 70% of instructions execute in 1-2 clock cycles
  - 25 MHz maximum operating frequency
- Memory:
  - Up to 64 kB flash memory, in-system re-programmable from firmware.
  - Up to 4352 bytes RAM (including 256 bytes standard 8051 RAM and 4096 bytes on-chip XRAM)
- Power:
  - Internal LDO regulator for CPU core voltage
  - Power-on reset circuit and brownout detectors
- I/O: Up to 24 total multifunction I/O pins:
  - Flexible peripheral crossbar for peripheral routing
  - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- Clock Sources:
  - Internal 20 MHz low power oscillator with  $\pm 10\%$  accuracy
  - Internal 24.5 MHz precision oscillator with  $\pm 2\%$  accuracy
  - External RTC 32 kHz crystal
  - External crystal, RC, C, and CMOS clock options
- Timers/Counters and PWM:
  - 32-bit Real Time Clock (RTC)
  - 6-channel programmable counter array (PCA) supporting PWM, capture/compare, and frequency output modes with watchdog timer function
  - 4 x 16-bit general-purpose timers
- Communications and Digital Peripherals:
  - UART
  - 2 x SPI™ Master / Slave
  - SMBus™/I2C™ Master / Slave
  - External Memory Interface (EMIF)
  - 16-bit/32-bit CRC unit, supporting automatic CRC of flash at 1024-byte boundaries
- Analog:
  - Programmable current reference (IREF0)
  - 10-Bit Analog-to-Digital Converter (ADC0)
  - 2 x Low-current analog comparators
- On-Chip, Non-Intrusive Debugging
  - Full memory and register inspection
  - Four hardware breakpoints, single-stepping
- Pre-loaded UART bootloader
- Temperature range -40 to 85 °C
- Single power supply 1.8 to 3.6 V
- QFP32, QFN32, and QFN24 packages

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8SB2 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing non-volatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Each device is specified for 1.8 to 3.6 V operation and is available in 24-pin QFN, 32-pin QFN, or 32-pin QFP packages. All package options are lead-free and RoHS compliant.

## 2. Ordering Information

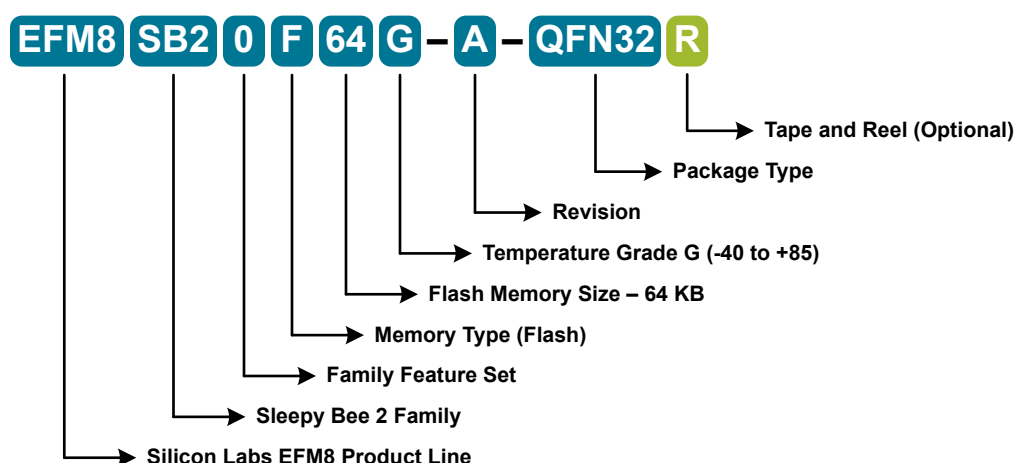


Figure 2.1. EFM8SB2 Part Numbering

All EFM8SB2 family members have the following features:

- CIP-51 Core running up to 25 MHz
- Three Internal Oscillators (24.5 MHz, 20 MHz, and 16 kHz)
- SMBus / I2C
- 2 x SPI
- UART
- 6-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- 4 16-bit Timers
- 2 Analog Comparators
- 6-bit programmable current reference
- 10-bit Analog-to-Digital Converter with integrated multiplexer, voltage reference, and temperature sensor
- Low-current 32 kHz oscillator and Real Time Clock
- 16-bit CRC Unit
- Pre-loaded UART bootloader

In addition to these features, each part number in the EFM8SB2 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

Table 2.1. Product Selection Guide

| Ordering Part Number | Flash Memory (kB) | RAM (Bytes) | Digital Port I/Os (Total) | ADC Channels | Comparator Inputs | Pb-free (RoHS Compliant) | Temperature Range | Package |
|----------------------|-------------------|-------------|---------------------------|--------------|-------------------|--------------------------|-------------------|---------|
| EFM8SB20F64G-A-QFN32 | 64                | 4352        | 24                        | 23           | 12                | Yes                      | -40 to +85 C      | QFN32   |
| EFM8SB20F64G-A-QFP32 | 64                | 4352        | 24                        | 23           | 12                | Yes                      | -40 to +85 C      | QFP32   |
| EFM8SB20F64G-A-QFN24 | 64                | 4352        | 16                        | 15           | 8                 | Yes                      | -40 to +85 C      | QFN24   |
| EFM8SB20F32G-A-QFN32 | 32                | 4352        | 24                        | 23           | 12                | Yes                      | -40 to +85 C      | QFN32   |
| EFM8SB20F32G-A-QFP32 | 32                | 4352        | 24                        | 23           | 12                | Yes                      | -40 to +85 C      | QFP32   |
| EFM8SB20F32G-A-QFN24 | 32                | 4352        | 16                        | 15           | 8                 | Yes                      | -40 to +85 C      | QFN24   |

| Ordering Part Number | Flash Memory (kB) | RAM (Bytes) | Digital Port I/Os (Total) | ADC Channels | Comparator Inputs | Pb-free (RoHS Compliant) | Temperature Range | Package |
|----------------------|-------------------|-------------|---------------------------|--------------|-------------------|--------------------------|-------------------|---------|
| EFM8SB20F16G-A-QFN24 | 16                | 4352        | 16                        | 15           | 8                 | Yes                      | -40 to +85 C      | QFN24   |

## 3. System Overview

### 3.1 Introduction

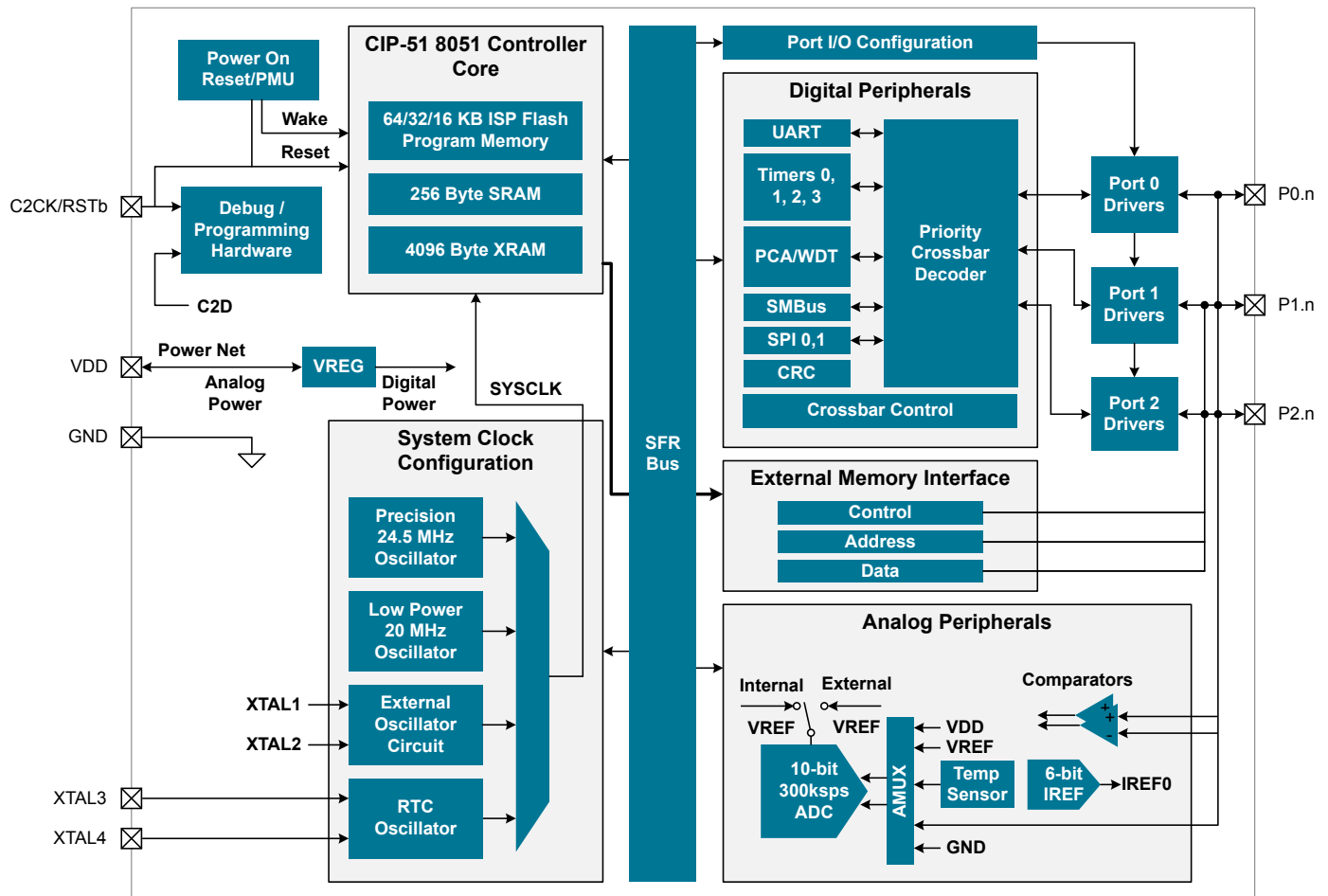


Figure 3.1. Detailed EFM8SB2 Block Diagram

### 3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

**Table 3.1. Power Modes**

| Power Mode | Details  | Mode Entry   | Wake-Up Sources   |
|------------|--|--|---|
| Normal     | Core and all peripherals clocked and fully operational   | —  | —   |
| Idle       | <ul style="list-style-type: none"> <li>Core halted</li> <li>All peripherals clocked and fully operational</li> <li>Code resumes execution on wake event</li> </ul>   | Set IDLE bit in PCON0  | Any interrupt   |
| Suspend    | <ul style="list-style-type: none"> <li>Core and digital peripherals halted</li> <li>Internal oscillators disabled</li> <li>Code resumes execution on wake event</li> </ul>   | <ol style="list-style-type: none"> <li>Switch SYSCLK to HFOSC0 or LPOSC0</li> <li>Set SUSPEND bit in PMU0CF</li> </ol> | <ul style="list-style-type: none"> <li>RTC0 Alarm Event</li> <li>RTC0 Fail Event</li> <li>Port Match Event</li> <li>Comparator 0 Rising Edge</li> </ul> |
| Sleep      | <ul style="list-style-type: none"> <li>Most internal power nets shut down</li> <li>Select circuits remain powered</li> <li>Pins retain state</li> <li>All RAM and SFRs retain state</li> <li>Code resumes execution on wake event</li> </ul> | <ol style="list-style-type: none"> <li>Disable unused analog peripherals</li> <li>Set SLEEP bit in PMU0CF</li> </ol>   | <ul style="list-style-type: none"> <li>RTC0 Alarm Event</li> <li>RTC0 Fail Event</li> <li>Port Match Event</li> <li>Comparator 0 Rising Edge</li> </ul> |

### 3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P2.6 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pin P2.7 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P2.7.

- Up to 24 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each pin.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 16 direct-pin interrupt sources with shared interrupt vector (Port Match).

### 3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 20 MHz low power oscillator divided by 8.

- Provides clock to core and peripherals.
- 20 MHz low power oscillator (LPOSC0), accurate to +/- 10% over supply and temperature corners.
- 24.5 MHz internal oscillator (HFOSC0), accurate to +/- 2% over supply and temperature corners.
- External RTC 32 kHz crystal.
- External RC, C, CMOS, and high-frequency crystal clock options (EXTCLK).
- Clock divider with eight settings for flexible clock scaling: Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.

### 3.5 Counters/Timers and PWM

#### Real Time Clock (RTC0)

The RTC is an ultra low power, 36 hour 32-bit independent time-keeping Real Time Clock with alarm. The RTC has a dedicated 32 kHz oscillator. No external resistor or loading capacitors are required, and a missing clock detector features alerts the system if the external crystal fails. The on-chip loading capacitors are programmable to 16 discrete levels allowing compatibility with a wide range of crystals.

The RTC module includes the following features:

- Up to 36 hours (32-bit) of independent time keeping.
- Support for external 32 kHz crystal or internal self-oscillate mode.
- Internal crystal loading capacitors with 16 levels.
- Operation in the lowest power mode and across the full supported voltage range.
- Alarm and oscillator failure events to wake from the lowest power mode or reset the device.

#### Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base.
- Programmable clock divisor and clock source selection.
- Up to six independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (edge-aligned operation).
- Frequency output mode.
- Capture on rising, falling or any edge.
- Compare function for arbitrary waveform generation.
- Software timer (internal compare) mode.
- Integrated watchdog timer.

#### Timers (Timer 0, Timer 1, Timer 2, and Timer 3)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2 and Timer 3 are 16-bit timers including the following features:

- Clock sources include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8.
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- Comparator 0 or RTC0 capture (Timer 2)
- Comparator 1 or EXTCLK/8 capture (Timer 3)

## Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) integrated within the PCA0 peripheral. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software. The state of the RSTb pin is unaffected by this reset.

The Watchdog Timer integrated in the PCA0 peripheral has the following features:

- Programmable timeout interval
- Runs from the selected PCA clock source
- Automatically enabled after any system reset

## 3.6 Communications and Other Digital Peripherals

### Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions
- Baud rates up to  $\text{SYSCLK}/2$  (transmit) or  $\text{SYSCLK}/8$  (receive)
- 8- or 9-bit data
- Automatic start and stop generation

### Serial Peripheral Interface (SPI0 and SPI1)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

The SPI module includes the following features:

- Supports 3- or 4-wire operation in master or slave modes.
- Supports external clock frequencies up to  $\text{SYSCLK} / 2$  in master mode and  $\text{SYSCLK} / 10$  in slave mode.
- Support for four clock phase and polarity options.
- 8-bit dedicated clock rate generator.
- Support for multiple masters on the same data lines.

### System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I<sup>2</sup>C serial bus.

The SMBus module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to inhibit all slave states.
- Programmable data setup/hold times.



## External Memory Interface (EMIF0)

The External Memory Interface (EMIF) enables access of off-chip memories and memory-mapped devices connected to the GPIO ports. The external memory space may be accessed using the external move instruction (MOVX) with the target address specified in either 8-bit or 16-bit formats.

- Supports multiplexed memory access.
- Four external memory modes:
  - Internal only.
  - Split mode without bank select.
  - Split mode with bank select.
  - External only
- Configurable ALE (address latch enable) timing.
- Configurable address setup and hold times.
- Configurable write and read pulse widths.

## 16/32-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit or 32-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module includes the following features:

- Support for CCITT-16 polynomial (0x1021).
- Support for CRC-32 polynomial (0x04C11DB7).
- Byte-level bit reversal.
- Automatic CRC of flash contents on one or more 1024-byte blocks.
- Initial seed selection of 0x0000/0x00000000 or 0xFFFF/0xFFFFFFFF.

## 3.7 Analog

### Programmable Current Reference (IREF0)

The programmable current reference (IREF0) module enables current source or sink with two output current settings: Low Power Mode and High Current Mode. The maximum current output in Low Power Mode is 63  $\mu\text{A}$  (1  $\mu\text{A}$  steps) and the maximum current output in High Current Mode is 504  $\mu\text{A}$  (8  $\mu\text{A}$  steps).

The IREF module includes the following features:

- Capable of sourcing or sinking current in programmable steps.
- Two operational modes: Low Power Mode and High Current Mode.

## 10-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 10- and 8-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 22 external inputs.
- Single-ended 10-bit mode.
- Supports an output update rate of 300 ksp/s samples per second.
- Operation in low power modes at lower conversion speeds.
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer sources.
- Output data window comparator allows automatic range checking.
- Support for burst mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Conversion complete and window compare interrupts supported.
- Flexible output data formatting.
- Includes an internal 1.65 V fast-settling reference and support for external reference.
- Integrated temperature sensor.

## Low Current Comparators (CMP0, CMP1)

Analog comparators are used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator module includes the following features:

- Up to 12 external positive inputs.
- Up to 11 external negative inputs.
- Additional input options:
  - Capacitive Sense Comparator output.
  - VDD.
  - VDD divided by 2.
  - Internal connection to LDO output.
  - Direct connection to GND.
- Synchronous and asynchronous outputs can be routed to pins via crossbar.
- Programmable hysteresis between 0 and +/-20 mV.
- Programmable response time.
- Interrupts generated on rising, falling, or both edges.

### 3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset
- RTC0 alarm or oscillator failure

### 3.9 Debugging

The EFM8SB2 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

### 3.10 Bootloader

All devices come pre-programmed with a UART bootloader. This bootloader resides in flash and can be erased if it is not needed.

## 4. Electrical Specifications

### 4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in [Table 4.1 Recommended Operating Conditions on page 11](#), unless stated otherwise.

**Table 4.1. Recommended Operating Conditions**

| Parameter  | Symbol                | Test Condition    | Min | Typ | Max | Unit |
|--|-----------------------|-------------------|-----|-----|-----|------|
| Operating Supply Voltage on VDD                        | V <sub>DD</sub>       |                   | 1.8 | 2.4 | 3.6 | V    |
| Minimum RAM Data Retention Voltage on VDD <sup>1</sup> | V <sub>RAM</sub>      | Not in Sleep Mode | —   | 1.4 | —   | V    |
|  |                       | Sleep Mode        | —   | 0.3 | 0.5 | V    |
| System Clock Frequency                                 | f <sub>SYSCLOCK</sub> |                   | 0   | —   | 25  | MHz  |
| Operating Ambient Temperature                          | T <sub>A</sub>        |                   | −40 | —   | 85  | °C   |

**Note:**

1. All voltages with respect to GND.

**Table 4.2. Power Consumption**

| Parameter   | Symbol              | Conditions   | Min | Typ  | Max | Units  |
|---|---------------------|--|-----|------|-----|--------|
| Digital Supply Current  |                     |  |     |      |     |        |
| Normal Mode supply current - Full speed with code executing from flash <sup>3, 4, 5</sup> | I <sub>DD</sub>     | V <sub>DD</sub> = 1.8–3.6 V, f <sub>SYSCLOCK</sub> = 24.5 MHz          | —   | 4.1  | 5.0 | mA     |
|   |                     | V <sub>DD</sub> = 1.8–3.6 V, f <sub>SYSCLOCK</sub> = 20 MHz            | —   | 3.5  | —   | mA     |
|   |                     | V <sub>DD</sub> = 1.8–3.6 V, f <sub>SYSCLOCK</sub> = 32.768 kHz        | —   | 90   | —   | μA     |
| Normal Mode supply current frequency sensitivity <sup>1, 3, 5</sup>                       | I <sub>DDFREQ</sub> | V <sub>DD</sub> = 1.8–3.6 V, T = 25 °C, f <sub>SYSCLOCK</sub> < 14 MHz | —   | 226  | —   | μA/MHz |
|   |                     | V <sub>DD</sub> = 1.8–3.6 V, T = 25 °C, f <sub>SYSCLOCK</sub> > 14 MHz | —   | 120  | —   | μA/MHz |
| Idle Mode supply current - Core halted with peripherals running <sup>4, 6</sup>           | I <sub>DD</sub>     | V <sub>DD</sub> = 1.8–3.6 V, f <sub>SYSCLOCK</sub> = 24.5 MHz          | —   | 2.5  | 3.0 | mA     |
|   |                     | V <sub>DD</sub> = 1.8–3.6 V, f <sub>SYSCLOCK</sub> = 20 MHz            | —   | 1.8  | —   | mA     |
|   |                     | V <sub>DD</sub> = 1.8–3.6 V, f <sub>SYSCLOCK</sub> = 32.768 kHz        | —   | 84   | —   | μA     |
| Idle Mode Supply Current Frequency Sensitivity <sup>1, 6</sup>                            | I <sub>DDFREQ</sub> | V <sub>DD</sub> = 1.8–3.6 V, T = 25 °C                                 | —   | 95   | —   | μA/MHz |
| Suspend Mode Supply Current   | I <sub>DD</sub>     | V <sub>DD</sub> = 1.8–3.6 V  | —   | 77   | —   | μA     |
| Sleep Mode Supply Current with RTC running from 32.768 kHz crystal                        | I <sub>DD</sub>     | 1.8 V, T = 25 °C   | —   | 0.60 | —   | μA     |
|   |                     | 3.6 V, T = 25 °C   | —   | 0.85 | —   | μA     |
|   |                     | 1.8 V, T = 85 °C   | —   | 1.30 | —   | μA     |
|   |                     | 3.6 V, T = 85 °C   | —   | 1.90 | —   | μA     |

| Parameter   | Symbol       | Conditions   | Min | Typ  | Max | Units         |
|---|--------------|--|-----|------|-----|---------------|
| Sleep Mode Supply Current (RTC off)                                 | $I_{DD}$     | 1.8 V, T = 25 °C                                     | —   | 0.05 | —   | $\mu\text{A}$ |
|   |              | 3.6 V, T = 25 °C                                     | —   | 0.12 | —   | $\mu\text{A}$ |
|   |              | 1.8 V, T = 85 °C                                     | —   | 0.75 | —   | $\mu\text{A}$ |
|   |              | 3.6 V, T = 85 °C                                     | —   | 1.20 | —   | $\mu\text{A}$ |
| V <sub>DD</sub> Monitor Supply Current                              | $I_{VMON}$   |  | —   | 7    | —   | $\mu\text{A}$ |
| Oscillator Supply Current   | $I_{HFOSC0}$ | 25 °C  | —   | 300  | —   | $\mu\text{A}$ |
| ADC0 Always-on Power Supply Current <sup>7</sup>                    | $I_{ADC}$    | 300 ksp/s<br>V <sub>DD</sub> = 3.0 V                 | —   | 800  | —   | $\mu\text{A}$ |
|   |              | Tracking<br>V <sub>DD</sub> = 3.0 V                  | —   | 680  | —   | $\mu\text{A}$ |
| Comparator 0 (CMP0) Supply Current                                  | $I_{CMP}$    | CPMD = 11  | —   | 0.4  | —   | $\mu\text{A}$ |
|   |              | CPMD = 10  | —   | 2.6  | —   | $\mu\text{A}$ |
|   |              | CPMD = 01  | —   | 8.8  | —   | $\mu\text{A}$ |
|   |              | CPMD = 00  | —   | 23   | —   | $\mu\text{A}$ |
| Internal Fast-settling 1.65V ADC0 Reference, Always-on <sup>8</sup> | $I_{VREFFS}$ |  | —   | 200  | —   | $\mu\text{A}$ |
| On-chip Precision Reference   | $I_{VREFP}$  |  | —   | 15   | —   | $\mu\text{A}$ |
| Temp sensor Supply Current  | $I_{TSENSE}$ |  | —   | 35   | —   | $\mu\text{A}$ |
| Programmable Current Reference (IREF0) Supply Current <sup>9</sup>  | $I_{IREF}$   | Current Source, Either Power Mode, Any Output Code   | —   | 10   | —   | $\mu\text{A}$ |
|   |              | Low Power Mode, Current Sink<br>IREF0DAT = 000001    | —   | 1    | —   | $\mu\text{A}$ |
|   |              | Low Power Mode, Current Sink<br>IREF0DAT = 111111    | —   | 11   | —   | $\mu\text{A}$ |
|   |              | High Current Mode, Current Sink<br>IREF0DAT = 000001 | —   | 12   | —   | $\mu\text{A}$ |
|   |              | High Current Mode, Current Sink<br>IREF0DAT = 111111 | —   | 81   | —   | $\mu\text{A}$ |

| Parameter   | Symbol | Conditions | Min | Typ | Max | Units |
|---|--------|------------|-----|-----|-----|-------|
| <b>Note:</b>  |        |            |     |     |     |       |
| 1. Based on device characterization data; Not production tested.  |        |            |     |     |     |       |
| 2. SYSCLK must be at least 32 kHz to enable debugging.  |        |            |     |     |     |       |
| 3. Digital Supply Current depends upon the particular code being executed. The values in this table are obtained with the CPU executing an “sjmp \$” loop, which is the compiled form of a while(1) loop in C. One iteration requires 3 CPU clock cycles, and the flash memory is read on each cycle. The supply current will vary slightly based on the physical location of the sjmp instruction and the number of flash address lines that toggle as a result. In the worst case, current can increase by up to 30% if the sjmp loop straddles a 128-byte flash address boundary (e.g., 0x007F to 0x0080). Real-world code with larger loops and longer linear sequences will have few transitions across the 128-byte address boundaries. |        |            |     |     |     |       |
| 4. Includes supply current from regulator and oscillator source (24.5 MHz high-frequency oscillator, 20 MHz low-power oscillator, or 32.768 kHz RTC oscillator).  |        |            |     |     |     |       |
| 5. IDD can be estimated for frequencies < 10 MHz by simply multiplying the frequency of interest by the frequency sensitivity number for that range, then adding an offset of 90 $\mu$ A. When using these numbers to estimate $I_{DD}$ for > 10 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: $V_{DD} = 3.0$ V; $F = 20$ MHz, $I_{DD} = 4.1$ mA – (25 MHz – 20 MHz) x 0.120 mA/MHz = 3.5 mA assuming the same oscillator setting.  |        |            |     |     |     |       |
| 6. Idle IDD can be estimated by taking the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: $V_{DD} = 3.0$ V; $F = 5$ MHz, Idle $I_{DD} = 2.5$ mA – (25 MHz – 5 MHz) x 0.095 mA/MHz = 0.6 mA.  |        |            |     |     |     |       |
| 7. ADC0 always-on power excludes internal reference supply current.   |        |            |     |     |     |       |
| 8. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.  |        |            |     |     |     |       |
| 9. IREF0 supply current only. Does not include current sourced or sunk from IREF0 output pin.   |        |            |     |     |     |       |

**Table 4.3. Reset and Supply Monitor**

| Parameter   | Symbol     | Test Condition  | Min | Typ  | Max  | Unit    |
|---|------------|---|-----|------|------|---------|
| VDD Supply Monitor Threshold                                      | $V_{VDDM}$ | Reset Trigger   | 1.7 | 1.75 | 1.8  | V       |
|   | $V_{WARN}$ | Early Warning   | 1.8 | 1.85 | 1.9  | V       |
| VDD Supply Monitor Turn-On Time                                   | $t_{MON}$  |   | —   | 300  | —    | ns      |
| Power-On Reset (POR) Monitor Threshold                            | $V_{POR}$  | Initial Power-On (Rising Voltage on $V_{DD}$ )          | —   | 0.75 | —    | V       |
|   |            | Falling Voltage on $V_{DD}$                             | 0.7 | 0.8  | 0.9  | V       |
|   |            | Brownout Recovery (Rising Voltage on $V_{DD}$ )         | —   | 0.95 | —    | V       |
| $V_{DD}$ Ramp Time  | $t_{RMP}$  | Time to $V_{DD} \geq 1.8$ V                             | —   | —    | 3    | ms      |
| Reset Delay   | $t_{RST}$  | Time between release of reset source and code execution | —   | 10   | —    | $\mu$ s |
| RST Low Time to Generate Reset                                    | $t_{RSTL}$ |   | 15  | —    | —    | $\mu$ s |
| Missing Clock Detector Response Time (final rising edge to reset) | $t_{MCD}$  | $F_{SYSCLK} > 1$ MHz                                    | 100 | 650  | 1000 | $\mu$ s |
| Missing Clock Detector Trigger Frequency                          | $F_{MCD}$  |   | —   | 7    | 10   | kHz     |

**Table 4.4. Flash Memory**

| Parameter               | Symbol      | Test Condition | Min | Typ | Max | Units   |
|-------------------------|-------------|----------------|-----|-----|-----|---------|
| Write Time <sup>1</sup> | $t_{WRITE}$ | One Byte       | 57  | 64  | 71  | $\mu$ s |
| Erase Time <sup>1</sup> | $t_{ERASE}$ | One Page       | 28  | 32  | 36  | ms      |

| Parameter   | Symbol   | Test Condition | Min | Typ  | Max | Units  |
|---|----------|----------------|-----|------|-----|--------|
| Endurance (Write/Erase Cycles)  | $N_{WE}$ |                | 1 k | 30 k | —   | Cycles |
| <b>Note:</b><br>1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.<br>2. Data Retention Information is published in the Quarterly Quality and Reliability Report. |          |                |     |      |     |        |

**Table 4.5. Power Management Timing**

| Parameter                 | Symbol           | Test Condition                  | Min | Typ | Max | Units   |
|---------------------------|------------------|---------------------------------|-----|-----|-----|---------|
| Idle Mode Wake-up Time    | $t_{IDLEWK}$     |                                 | 2   | —   | 3   | SYSCLKs |
| Suspend Mode Wake-up Time | $t_{SUS-PENDWK}$ | CLKDIV = 0x00<br>Precision Osc. | —   | 400 | —   | ns      |
|                           |                  | CLKDIV = 0x00<br>Low Power Osc. | —   | 1.3 | —   | $\mu$ s |
| Sleep Mode Wake-up Time   | $t_{SLEEPWK}$    |                                 | —   | 2   | —   | $\mu$ s |

**Table 4.6. Internal Oscillators**

| Parameter                              | Symbol       | Test Condition                    | Min | Typ         | Max | Unit |
|--|--------------|-----------------------------------|-----|-------------|-----|------|
| High Frequency Oscillator 0 (24.5 MHz) |              |                                   |     |             |     |      |
| Oscillator Frequency                   | $f_{HFOSC0}$ | Full Temperature and Supply Range | 24  | 24.5        | 25  | MHz  |
| Low Power Oscillator (20 MHz)          |              |                                   |     |             |     |      |
| Oscillator Frequency                   | $f_{LPOSC}$  | Full Temperature and Supply Range | 18  | 20          | 22  | MHz  |
| RTC in Self-Oscillate Mode             |              |                                   |     |             |     |      |
| Oscillator Frequency                   | $f_{LFOSC}$  | Bias Off                          | —   | 12 $\pm$ 5  | —   | kHz  |
|  |              | Bias On                           | —   | 25 $\pm$ 10 | —   | kHz  |

**Table 4.7. Crystal Oscillator**

| Parameter         | Symbol     | Test Condition | Min  | Typ | Max | Unit |
|-------------------|------------|----------------|------|-----|-----|------|
| Crystal Frequency | $f_{XTAL}$ |                | 0.02 | -   | 25  | MHz  |

**Table 4.8. External Clock Input**

| Parameter   | Symbol      | Test Condition | Min | Typ | Max | Unit |
|---|-------------|----------------|-----|-----|-----|------|
| External Input CMOS Clock Frequency (at EXTCLK pin) | $f_{CMOS}$  |                | 0   | —   | 25  | MHz  |
| External Input CMOS Clock High Time                 | $t_{CMOSH}$ |                | 18  | —   | —   | ns   |
| External Input CMOS Clock Low Time                  | $t_{CMOSL}$ |                | 18  | —   | —   | ns   |

Table 4.9. ADC

| Parameter   | Symbol              | Test Condition           | Min | Typ   | Max                  | Unit   |
|---|---------------------|--------------------------|-----|-------|----------------------|--------|
| Resolution  | N <sub>bits</sub>   |                          | 10  |       |                      | Bits   |
| Throughput Rate   | f <sub>S</sub>      |                          | —   | —     | 300                  | ksps   |
| Tracking Time   | t <sub>TRK</sub>    |                          | 1.5 | —     | —                    | μs     |
| Power-On Time   | t <sub>PWR</sub>    |                          | 1.5 | —     | —                    | μs     |
| SAR Clock Frequency   | f <sub>SAR</sub>    | High Speed Mode,         | —   | —     | 8.33                 | MHz    |
| Conversion Time   | T <sub>CNV</sub>    |                          | 13  | —     | —                    | Clocks |
| Sample/Hold Capacitor   | C <sub>SAR</sub>    | Gain = 1                 | —   | 30    | —                    | pF     |
|   |                     | Gain = 0.5               | —   | 28    | —                    | pF     |
| Input Pin Capacitance   | C <sub>IN</sub>     |                          | —   | 20    | —                    | pF     |
| Input Mux Impedance   | R <sub>MUX</sub>    |                          | —   | 5     | —                    | kΩ     |
| Voltage Reference Range   | V <sub>REF</sub>    |                          | 1   | —     | V <sub>DD</sub>      | V      |
| Input Voltage Range <sup>1</sup>  | V <sub>IN</sub>     | Gain = 1                 | 0   | —     | V <sub>REF</sub>     | V      |
|   |                     | Gain = 0.5               | 0   | —     | 2 x V <sub>REF</sub> | V      |
| Power Supply Rejection Ratio  | PSRR <sub>ADC</sub> | Internal High Speed VREF | —   | 67    | —                    | dB     |
|   |                     | External VREF            | —   | 74    | —                    | dB     |
| DC Performance  |                     |                          |     |       |                      |        |
| Integral Nonlinearity   | INL                 |                          | —   | ±0.5  | ±1                   | LSB    |
| Differential Nonlinearity (Guaranteed Monotonic)  | DNL                 |                          | —   | ±0.5  | ±1                   | LSB    |
| Offset Error  | E <sub>OFF</sub>    | VREF = 1.65 V            | –2  | 0     | 2                    | LSB    |
| Offset Temperature Coefficient  | TC <sub>OFF</sub>   |                          | —   | 0.004 | —                    | LSB/°C |
| Slope Error   | E <sub>M</sub>      |                          | —   | ±0.06 | ±0.24                | %      |
| Dynamic Performance 10 kHz Sine Wave Input 1dB below full scale, Max throughput         |                     |                          |     |       |                      |        |
| Signal-to-Noise   | SNR                 |                          | 54  | 58    | —                    | dB     |
| Signal-to-Noise Plus Distortion   | SNDR                |                          | 54  | 58    | —                    | dB     |
| Total Harmonic Distortion (Up to 5th Harmonic)  | THD                 |                          | —   | -73   | —                    | dB     |
| Spurious-Free Dynamic Range   | SFDR                |                          | —   | 75    | —                    | dB     |
| <b>Note:</b><br>1. Absolute input pin voltage is limited by the V <sub>DD</sub> supply. |                     |                          |     |       |                      |        |

Table 4.10. Voltage References

| Parameter                        | Symbol             | Test Condition | Min  | Typ  | Max  | Unit |
|----------------------------------|--------------------|----------------|------|------|------|------|
| Internal Fast Settling Reference |                    |                |      |      |      |      |
| Output Voltage                   | V <sub>REFFS</sub> |                | 1.60 | 1.65 | 1.70 | V    |



| Parameter                         | Symbol         | Test Condition                                      | Min   | Typ  | Max      | Unit    |
|-----------------------------------|----------------|---|-------|------|----------|---------|
| Temperature Coefficient           | $TC_{REFFS}$   |   | —     | 50   | —        | ppm/°C  |
| Turn-on Time                      | $t_{VREFFS}$   |   | —     | —    | 1.5      | μs      |
| Power Supply Rejection            | $PSRR_{REFFS}$ |   | —     | 400  | —        | ppm/V   |
| On-chip Precision Reference       |                |   |       |      |          |         |
| Output Voltage                    | $V_{REFP}$     |   | 1.645 | 1.68 | 1.715    | V       |
| Turn-on Time, settling to 0.5 LSB | $t_{VREFP}$    | 4.7 μF tantalum + 0.1 μF ceramic bypass on VREF pin | —     | 15   | —        | ms      |
|                                   |                | 0.1 μF ceramic bypass on VREF pin                   | —     | 300  | —        | μs      |
|                                   |                | No bypass on VREF pin                               | —     | 25   | —        | μs      |
| Load Regulation                   | $LR_{VREFP}$   | Load = 0 to 200 μA to GND                           | —     | 400  | —        | μV / μA |
| Short-circuit current             | $ISC_{VREFP}$  |   | —     | 3.5  | —        | mA      |
| Power Supply Rejection            | $PSRR_{VREFP}$ |   | —     | 140  | —        | ppm/V   |
| External Reference                |                |   |       |      |          |         |
| Input Voltage                     | $V_{EXTREF}$   |   | 1     | —    | $V_{DD}$ | V       |
| Input Current                     | $I_{EXTREF}$   | Sample Rate = 300 ksps; $V_{REF} = 3.0$ V           | —     | 5.25 | —        | μA      |

**Table 4.11. Temperature Sensor**

| Parameter   | Symbol    | Test Condition | Min | Typ  | Max | Unit  |
|---|-----------|----------------|-----|------|-----|-------|
| Offset  | $V_{OFF}$ | $T_A = 0$ °C   | —   | 940  | —   | mV    |
| Offset Error <sup>1</sup>   | $E_{OFF}$ | $T_A = 0$ °C   | —   | 18   | —   | mV    |
| Slope   | $M$       |                | —   | 3.40 | —   | mV/°C |
| Slope Error <sup>1</sup>  | $E_M$     |                | —   | 40   | —   | μV/°C |
| Linearity   |           |                | —   | ±1   | —   | °C    |
| Turn-on Time  | $t_{PWR}$ |                | —   | 1.8  | —   | μs    |
| <b>Note:</b><br>1. Represents one standard deviation from the mean. |           |                |     |      |     |       |

**Table 4.12. Comparators**

| Parameter                                | Symbol      | Test Condition       | Min | Typ  | Max | Unit |
|--|-------------|----------------------|-----|------|-----|------|
| Response Time, CPMD = 00 (Highest Speed) | $t_{RESP0}$ | +100 mV Differential | —   | 130  | —   | ns   |
|  |             | –100 mV Differential | —   | 200  | —   | ns   |
| Response Time, CPMD = 11 (Lowest Power)  | $t_{RESP3}$ | +100 mV Differential | —   | 1.75 | —   | μs   |
|  |             | –100 mV Differential | —   | 6.2  | —   | μs   |

| Parameter                                 | Symbol             | Test Condition         | Min   | Typ  | Max                   | Unit |
|---|--------------------|------------------------|-------|------|-----------------------|------|
| Positive Hysterisis<br>Mode 0 (CPMD = 00) | HYS <sub>CP+</sub> | CPHYP = 00             | —     | 0.4  | —                     | mV   |
|   |                    | CPHYP = 01             | —     | 8    | —                     | mV   |
|   |                    | CPHYP = 10             | —     | 16   | —                     | mV   |
|   |                    | CPHYP = 11             | —     | 32   | —                     | mV   |
| Negative Hysterisis<br>Mode 0 (CPMD = 00) | HYS <sub>CP-</sub> | CPHYN = 00             | —     | -0.4 | —                     | mV   |
|   |                    | CPHYN = 01             | —     | -8   | —                     | mV   |
|   |                    | CPHYN = 10             | —     | -16  | —                     | mV   |
|   |                    | CPHYN = 11             | —     | -32  | —                     | mV   |
| Positive Hysterisis<br>Mode 1 (CPMD = 01) | HYS <sub>CP+</sub> | CPHYP = 00             | —     | 0.5  | —                     | mV   |
|   |                    | CPHYP = 01             | —     | 6    | —                     | mV   |
|   |                    | CPHYP = 10             | —     | 12   | —                     | mV   |
|   |                    | CPHYP = 11             | —     | 24   | —                     | mV   |
| Negative Hysterisis<br>Mode 1 (CPMD = 01) | HYS <sub>CP-</sub> | CPHYN = 00             | —     | -0.5 | —                     | mV   |
|   |                    | CPHYN = 01             | —     | -6   | —                     | mV   |
|   |                    | CPHYN = 10             | —     | -12  | —                     | mV   |
|   |                    | CPHYN = 11             | —     | -24  | —                     | mV   |
| Positive Hysterisis<br>Mode 2 (CPMD = 10) | HYS <sub>CP+</sub> | CPHYP = 00             | —     | 0.7  | —                     | mV   |
|   |                    | CPHYP = 01             | —     | 4.5  | —                     | mV   |
|   |                    | CPHYP = 10             | —     | 9    | —                     | mV   |
|   |                    | CPHYP = 11             | —     | 18   | —                     | mV   |
| Negative Hysterisis<br>Mode 2 (CPMD = 10) | HYS <sub>CP-</sub> | CPHYN = 00             | —     | -0.6 | —                     | mV   |
|   |                    | CPHYN = 01             | —     | -4.5 | —                     | mV   |
|   |                    | CPHYN = 10             | —     | -9   | —                     | mV   |
|   |                    | CPHYN = 11             | —     | -18  | —                     | mV   |
| Positive Hysterisis<br>Mode 3 (CPMD = 11) | HYS <sub>CP+</sub> | CPHYP = 00             | —     | 1.5  | —                     | mV   |
|   |                    | CPHYP = 01             | —     | 4    | —                     | mV   |
|   |                    | CPHYP = 10             | —     | 8    | —                     | mV   |
|   |                    | CPHYP = 11             | —     | 16   | —                     | mV   |
| Negative Hysterisis<br>Mode 3 (CPMD = 11) | HYS <sub>CP-</sub> | CPHYN = 00             | —     | -1.5 | —                     | mV   |
|   |                    | CPHYN = 01             | —     | -4   | —                     | mV   |
|   |                    | CPHYN = 10             | —     | -8   | —                     | mV   |
|   |                    | CPHYN = 11             | —     | -16  | —                     | mV   |
| Input Range (CP+ or CP-)                  | V <sub>IN</sub>    |                        | -0.25 | —    | V <sub>DD</sub> +0.25 | V    |
| Input Pin Capacitance                     | C <sub>CP</sub>    |                        | —     | 12   | —                     | pF   |
| Common-Mode Rejection Ratio               | CMRR <sub>CP</sub> |                        | —     | 70   | —                     | dB   |
| Power Supply Rejection Ratio              | PSRR <sub>CP</sub> |                        | —     | 72   | —                     | dB   |
| Input Offset Voltage                      | V <sub>OFF</sub>   | T <sub>A</sub> = 25 °C | -10   | 0    | 10                    | mV   |

| Parameter           | Symbol            | Test Condition | Min | Typ | Max | Unit  |
|---------------------|-------------------|----------------|-----|-----|-----|-------|
| Input Offset Tempco | TC <sub>OFF</sub> |                | —   | 3.5 | —   | μV/°C |

**Table 4.13. Programmable Current Reference (IREF0)**

| Parameter  | Symbol              | Conditions                    | Min | Typ   | Max                   | Units |
|--|---------------------|-------------------------------|-----|-------|-----------------------|-------|
| Static Performance   |                     |                               |     |       |                       |       |
| Resolution   | N <sub>bits</sub>   |                               | 6   |       |                       | bits  |
| Output Compliance Range  | V <sub>IOUT</sub>   | Low Power Mode, Source        | 0   | —     | V <sub>DD</sub> – 0.4 | V     |
|  |                     | High Current Mode, Source     | 0   | —     | V <sub>DD</sub> – 0.8 | V     |
|  |                     | Low Power Mode, Sink          | 0.3 | —     | V <sub>DD</sub>       | V     |
|  |                     | High Current Mode, Sink       | 0.8 | —     | V <sub>DD</sub>       | V     |
| Integral Nonlinearity  | INL                 |                               | —   | <±0.2 | ±1.0                  | LSB   |
| Differential Nonlinearity  | DNL                 |                               | —   | <±0.2 | ±1.0                  | LSB   |
| Offset Error   | E <sub>OFF</sub>    |                               | —   | <±0.1 | ±0.5                  | LSB   |
| Full Scale Error   | E <sub>FS</sub>     | Low Power Mode, Source        | —   | —     | ±5                    | %     |
|  |                     | High Current Mode, Source     | —   | —     | ±6                    | %     |
|  |                     | Low Power Mode, Sink          | —   | —     | ±8                    | %     |
|  |                     | High Current Mode, Sink       | —   | —     | ±8                    | %     |
| Absolute Current Error   | E <sub>ABS</sub>    | Low Power Mode Sourcing 20 μA | —   | <±1   | ±3                    | %     |
| Dynamic Performance  |                     |                               |     |       |                       |       |
| Output Settling Time to 1/2 LSB  | t <sub>SETTLE</sub> |                               | —   | 300   | —                     | ns    |
| Startup Time   | t <sub>PWR</sub>    |                               | —   | 1     | —                     | μs    |
| <b>Note:</b><br>1. The PCA block may be used to improve IREF0 resolution by PWMing the two LSBs. |                     |                               |     |       |                       |       |

**Table 4.14. Port I/O**

| Parameter                        | Symbol          | Test Condition                 | Min                   | Typ | Max                   | Unit |
|----------------------------------|-----------------|--------------------------------|-----------------------|-----|-----------------------|------|
| Output High Voltage (High Drive) | V <sub>OH</sub> | I <sub>OH</sub> = –3 mA        | V <sub>DD</sub> – 0.7 | —   | —                     | V    |
| Output Low Voltage (High Drive)  | V <sub>OL</sub> | I <sub>OL</sub> = 8.5 mA       | —                     | —   | 0.6                   | V    |
| Output High Voltage (Low Drive)  | V <sub>OH</sub> | I <sub>OH</sub> = –1 mA        | V <sub>DD</sub> – 0.7 | —   | —                     | V    |
| Output Low Voltage (Low Drive)   | V <sub>OL</sub> | I <sub>OL</sub> = 1.4 mA       | —                     | —   | 0.6                   | V    |
| Input High Voltage               | V <sub>IH</sub> | V <sub>DD</sub> = 2.0 to 3.6 V | V <sub>DD</sub> – 0.6 | —   | —                     | V    |
|                                  |                 | V <sub>DD</sub> = 1.8 to 2.0 V | 0.7 x V <sub>DD</sub> | —   | —                     | V    |
| Input Low Voltage                | V <sub>IL</sub> | V <sub>DD</sub> = 2.0 to 3.6 V | —                     | —   | 0.6                   | V    |
|                                  |                 | V <sub>DD</sub> = 1.8 to 2.0 V | —                     | —   | 0.3 x V <sub>DD</sub> | V    |

| Parameter            | Symbol   | Test Condition                                   | Min | Typ | Max | Unit          |
|----------------------|----------|--|-----|-----|-----|---------------|
| Weak Pull-Up Current | $I_{PU}$ | $V_{DD} = 1.8\text{ V}$<br>$V_{IN} = 0\text{ V}$ | —   | –4  | —   | $\mu\text{A}$ |
|                      |          | $V_{DD} = 3.6\text{ V}$<br>$V_{IN} = 0\text{ V}$ | –35 | –20 | —   | $\mu\text{A}$ |
| Input Leakage        | $I_{LK}$ | Weak pullup disabled or pin in analog mode       | –1  | —   | 1   | $\mu\text{A}$ |

## 4.2 Thermal Conditions

**Table 4.15. Thermal Conditions**

| Parameter                       | Symbol        | Test Condition  | Min | Typ | Max | Unit                 |
|---------------------------------|---------------|-----------------|-----|-----|-----|----------------------|
| Thermal Resistance <sup>1</sup> | $\theta_{JA}$ | QFN-24 Packages | —   | 35  | —   | $^{\circ}\text{C/W}$ |
|                                 |               | QFN-32 Packages | —   | 28  | —   | $^{\circ}\text{C/W}$ |
|                                 |               | QFP-32 Packages | —   | 80  | —   | $^{\circ}\text{C/W}$ |

**Note:**

1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

## 4.3 Absolute Maximum Ratings

Stresses above those listed in [Table 4.16 Absolute Maximum Ratings on page 19](#) may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

**Table 4.16. Absolute Maximum Ratings**

| Parameter                                      | Symbol      | Test Condition             | Min     | Max            | Unit               |
|--|-------------|----------------------------|---------|----------------|--------------------|
| Ambient Temperature Under Bias                 | $T_{BIAS}$  |                            | –55     | 125            | $^{\circ}\text{C}$ |
| Storage Temperature                            | $T_{STG}$   |                            | –65     | 150            | $^{\circ}\text{C}$ |
| Voltage on $V_{DD}$                            | $V_{DD}$    |                            | GND–0.3 | 4.0            | V                  |
| Voltage on I/O pins or RSTb                    | $V_{IN}$    | $V_{DD} > 2.2\text{ V}$    | GND–0.3 | 5.8            | V                  |
|  |             | $V_{DD} \leq 2.2\text{ V}$ | GND–0.3 | $V_{DD} + 3.6$ | V                  |
| Total Current Sunk into Supply Pin             | $I_{VDD}$   |                            | —       | 400            | mA                 |
| Total Current Sourced out of Ground Pin        | $I_{GND}$   |                            | 400     | —              | mA                 |
| Current Sourced or Sunk by Any I/O Pin or RSTb | $I_{IO}$    |                            | –100    | 100            | mA                 |
| Maximum Total Current through all Port Pins    | $I_{IOTOT}$ |                            | —       | 200            | mA                 |
| Operating Junction Temperature                 | $T_J$       |                            | –40     | 105            | $^{\circ}\text{C}$ |

Exposure to maximum rating conditions for extended periods may affect device reliability.

#### 4.4 Typical Performance Curves

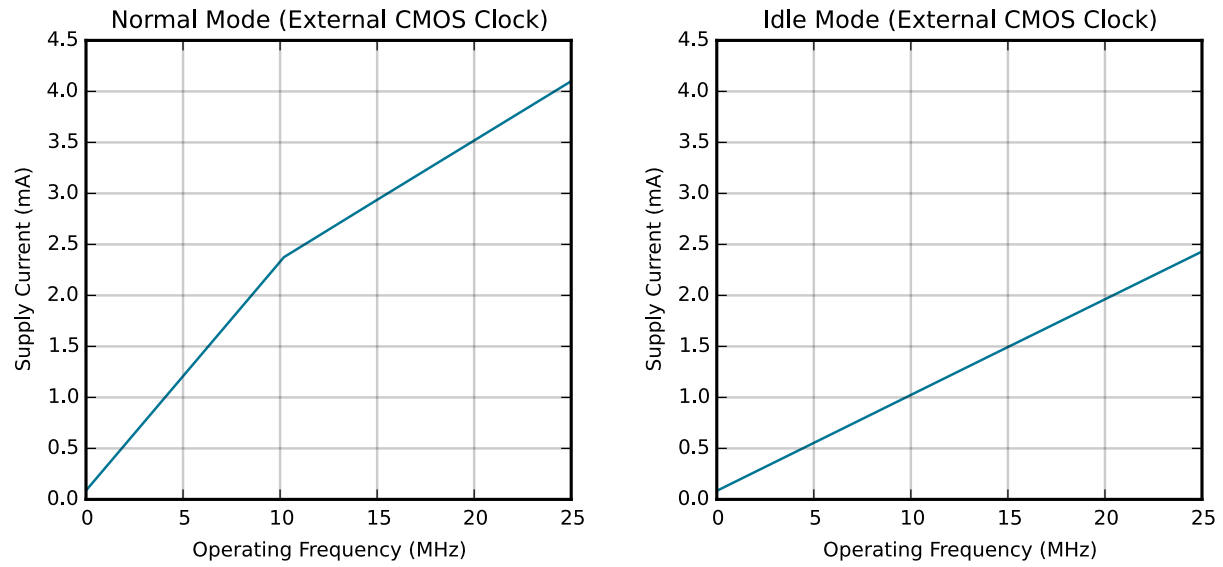


Figure 4.1. Typical Operating Supply Current (full supply voltage range)

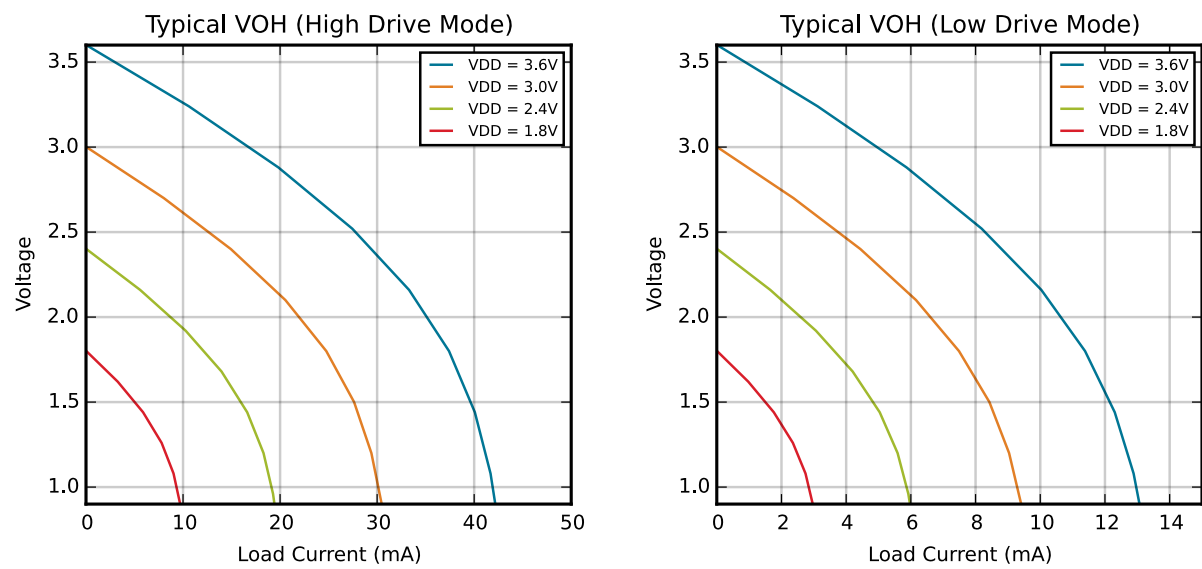
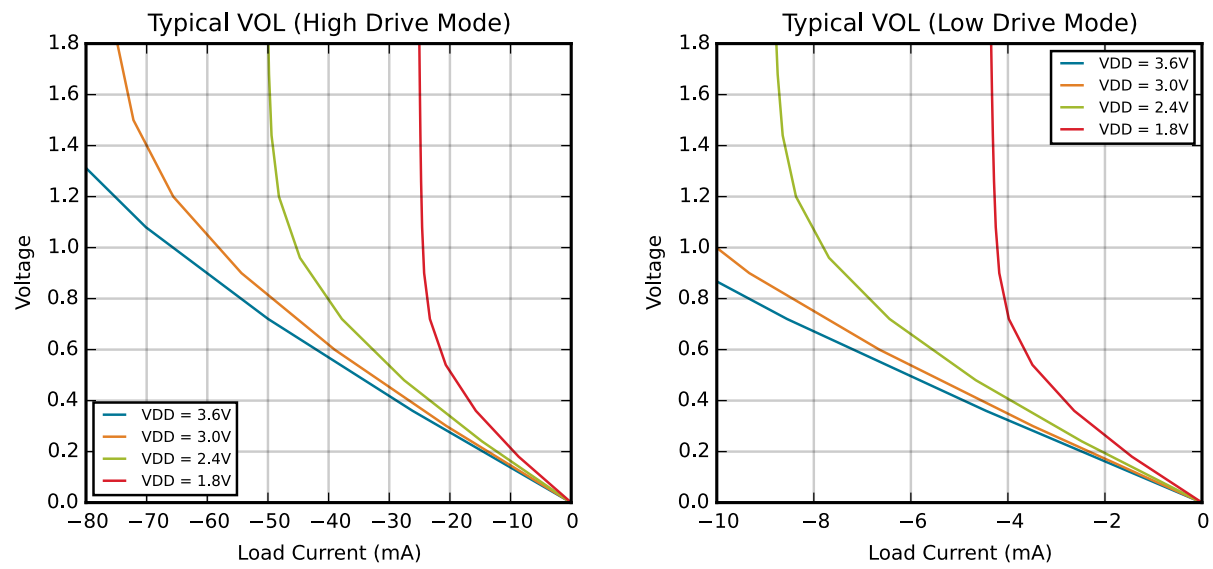


Figure 4.2. Typical  $V_{OH}$  Curves



**Figure 4.3. Typical  $V_{OL}$  Curves**

## 5. Typical Connection Diagrams

### 5.1 Power

Figure 5.1 Power Connection Diagram on page 22 shows a typical connection diagram for the power pins of the EFM8SB2 devices.

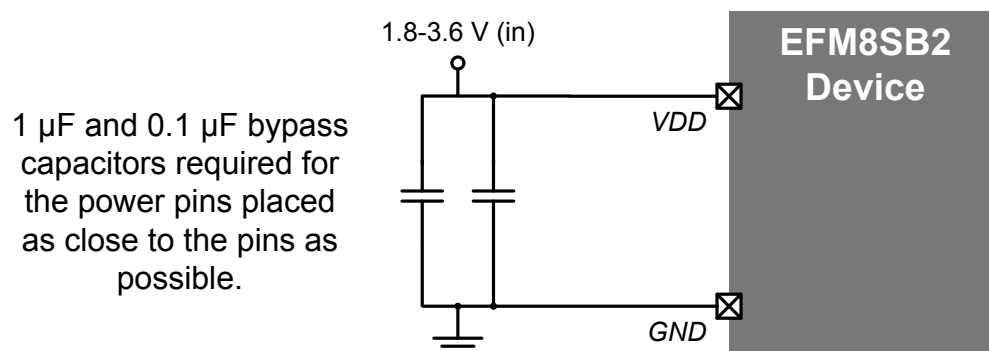


Figure 5.1. Power Connection Diagram

### 5.2 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN203: "8-bit MCU Printed Circuit Board Design Notes" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website ([www.silabs.com/8bit-appnotes](http://www.silabs.com/8bit-appnotes)).

## 6. Pin Definitions

### 6.1 EFM8SB2x-QFN32 Pin Definitions

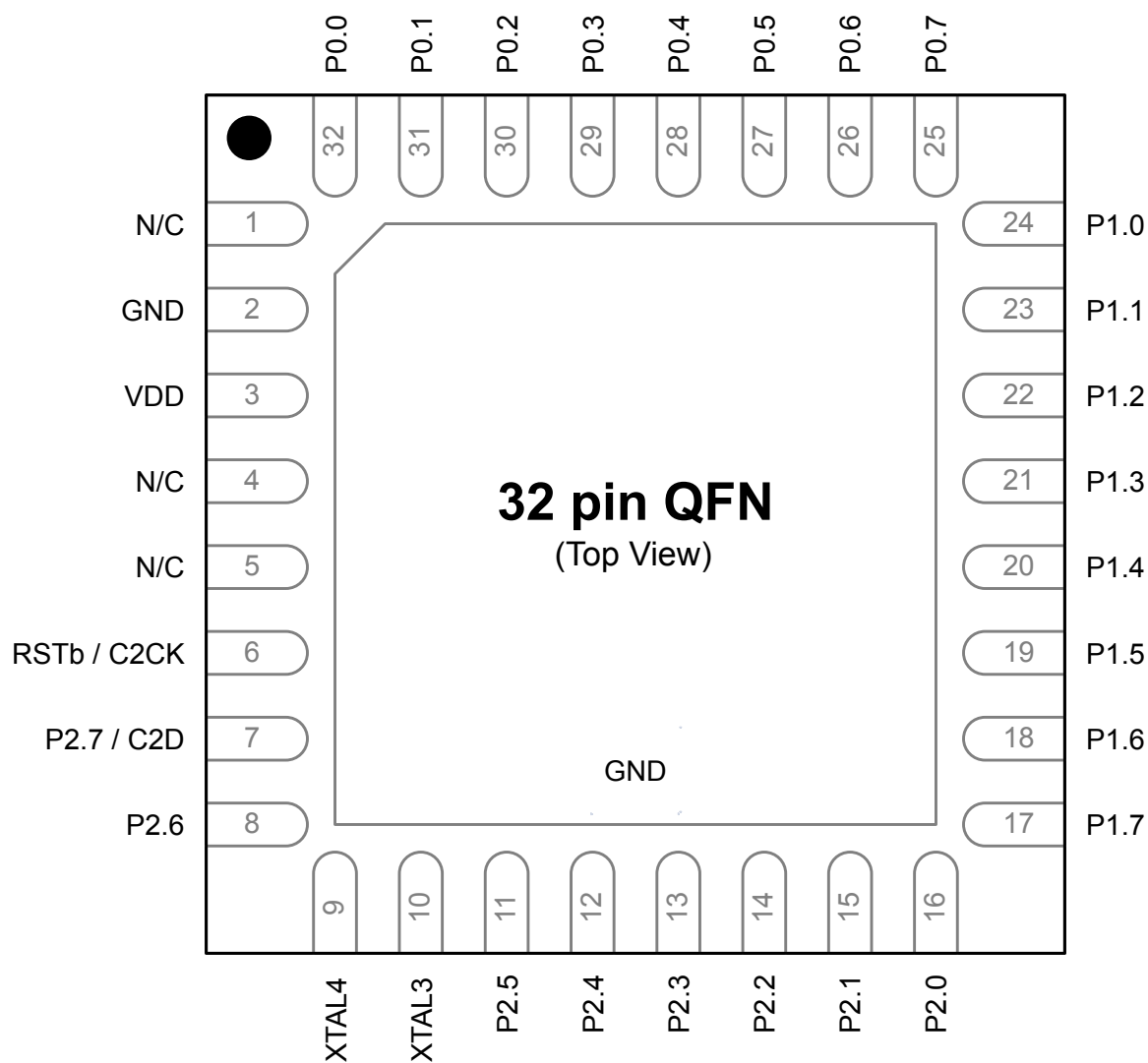


Figure 6.1. EFM8SB2x-QFN32 Pinout

Table 6.1. Pin Definitions for EFM8SB2x-QFN32

| Pin Number | Pin Name | Description        | Crossbar Capability | Additional Digital Functions | Analog Functions |
|------------|----------|--------------------|---------------------|------------------------------|------------------|
| 1          | N/C      | No Connection      |                     |                              |                  |
| 2          | GND      | Ground             |                     |                              |                  |
| 3          | VDD      | Supply Power Input |                     |                              |                  |
| 4          | N/C      | No Connection      |                     |                              |                  |



| Pin Number | Pin Name       | Description                          | Crossbar Capability | Additional Digital Functions | Analog Functions                |
|------------|----------------|--------------------------------------|---------------------|------------------------------|---------------------------------|
| 5          | N/C            | No Connection                        |                     |                              |                                 |
| 6          | RSTb /<br>C2CK | Active-low Reset /<br>C2 Debug Clock |                     |                              |                                 |
| 7          | P2.7 /<br>C2D  | Multifunction I/O /<br>C2 Debug Data |                     |                              |                                 |
| 8          | P2.6           | Multifunction I/O                    | Yes                 | EMIF_WRb                     | ADC0.22<br>CMP0P.11<br>CMP1P.11 |
| 9          | XTAL4          | RTC Crystal                          |                     |                              | XTAL4                           |
| 10         | XTAL3          | RTC Crystal                          |                     |                              | XTAL3                           |
| 11         | P2.5           | Multifunction I/O                    | Yes                 | EMIF_RDb                     | ADC0.21<br>CMP0N.10<br>CMP1N.10 |
| 12         | P2.4           | Multifunction I/O                    | Yes                 | EMIF_ALE                     | ADC0.20<br>CMP0P.10<br>CMP1P.10 |
| 13         | P2.3           | Multifunction I/O                    | Yes                 | EMIF_A11                     | ADC0.19<br>CMP0N.9<br>CMP1N.9   |
| 14         | P2.2           | Multifunction I/O                    | Yes                 | EMIF_A10                     | ADC0.18<br>CMP0P.9<br>CMP1P.9   |
| 15         | P2.1           | Multifunction I/O                    | Yes                 | EMIF_A9                      | ADC0.17<br>CMP0N.8<br>CMP1N.8   |
| 16         | P2.0           | Multifunction I/O                    | Yes                 | EMIF_A8                      | ADC0.16<br>CMP0P.8<br>CMP1P.8   |
| 17         | P1.7           | Multifunction I/O                    | Yes                 | P1MAT.7<br>EMIF_AD7          | ADC0.15<br>CMP0N.7<br>CMP1N.7   |
| 18         | P1.6           | Multifunction I/O                    | Yes                 | P1MAT.6<br>EMIF_AD6          | ADC0.14<br>CMP0P.7<br>CMP1P.7   |

| Pin Number | Pin Name | Description       | Crossbar Capability | Additional Digital Functions          | Analog Functions                      |
|------------|----------|-------------------|---------------------|---------------------------------------|---------------------------------------|
| 19         | P1.5     | Multifunction I/O | Yes                 | P1MAT.5<br>EMIF_AD5                   | ADC0.13<br>CMP0N.6<br>CMP1N.6         |
| 20         | P1.4     | Multifunction I/O | Yes                 | P1MAT.4<br>EMIF_AD4                   | ADC0.12<br>CMP0P.6<br>CMP1P.6         |
| 21         | P1.3     | Multifunction I/O | Yes                 | P1MAT.3<br>SPI1_NSS<br>EMIF_AD3       | ADC0.11<br>CMP0N.5<br>CMP1N.5         |
| 22         | P1.2     | Multifunction I/O | Yes                 | P1MAT.2<br>SPI1_MOSI<br>EMIF_AD2      | ADC0.10<br>CMP0P.5<br>CMP1P.5         |
| 23         | P1.1     | Multifunction I/O | Yes                 | P1MAT.1<br>SPI1_MISO<br>EMIF_AD1      | ADC0.9<br>CMP0N.4<br>CMP1N.4          |
| 24         | P1.0     | Multifunction I/O | Yes                 | P1MAT.0<br>SPI1_SCK<br>EMIF_AD0       | ADC0.8<br>CMP0P.4<br>CMP1P.4          |
| 25         | P0.7     | Multifunction I/O | Yes                 | P0MAT.7<br>INT0.7<br>INT1.7           | ADC0.7<br>IREF0<br>CMP0N.3<br>CMP1N.3 |
| 26         | P0.6     | Multifunction I/O | Yes                 | P0MAT.6<br>CNVSTR<br>INT0.6<br>INT1.6 | ADC0.6<br>CMP0P.3<br>CMP1P.3          |
| 27         | P0.5     | Multifunction I/O | Yes                 | P0MAT.5<br>INT0.5<br>INT1.5           | ADC0.5<br>CMP0N.2<br>CMP1N.2          |
| 28         | P0.4     | Multifunction I/O | Yes                 | P0MAT.4<br>INT0.4<br>INT1.4           | ADC0.4<br>CMP0P.2<br>CMP1P.2          |
| 29         | P0.3     | Multifunction I/O | Yes                 | P0MAT.3<br>EXTCLK<br>INT0.3<br>INT1.3 | ADC0.3<br>XTAL2<br>CMP0N.1<br>CMP1N.1 |

| Pin Number | Pin Name | Description       | Crossbar Capability | Additional Digital Functions | Analog Functions                      |
|------------|----------|-------------------|---------------------|------------------------------|---------------------------------------|
| 30         | P0.2     | Multifunction I/O | Yes                 | P0MAT.2<br>INT0.2<br>INT1.2  | ADC0.2<br>CMP0P.1<br>CMP1P.1<br>XTAL1 |
| 31         | P0.1     | Multifunction I/O | Yes                 | P0MAT.1<br>INT0.1<br>INT1.1  | ADC0.1<br>AGND<br>CMP0N.0<br>CMP1N.0  |
| 32         | P0.0     | Multifunction I/O | Yes                 | P0MAT.0<br>INT0.0<br>INT1.0  | ADC0.0<br>CMP0P.0<br>CMP1P.0<br>VREF  |
| Center     | GND      | Ground            |                     |                              |                                       |

## 6.2 EFM8SB2x-QFN24 Pin Definitions

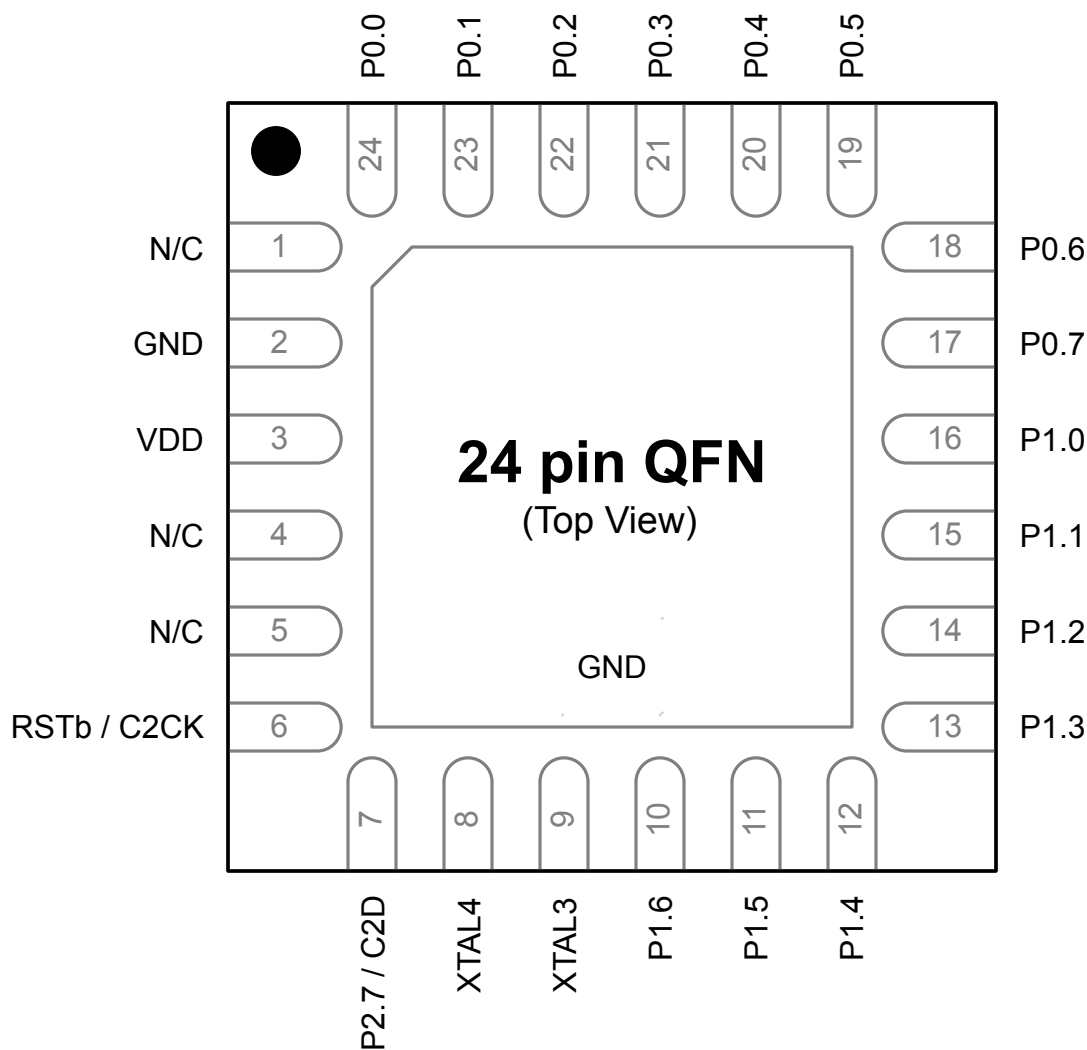


Figure 6.2. EFM8SB2x-QFN24 Pinout

Table 6.2. Pin Definitions for EFM8SB2x-QFN24

| Pin Number | Pin Name | Description        | Crossbar Capability | Additional Digital Functions | Analog Functions |
|------------|----------|--------------------|---------------------|------------------------------|------------------|
| 1          | N/C      | No Connection      |                     |                              |                  |
| 2          | GND      | Ground             |                     |                              |                  |
| 3          | VDD      | Supply Power Input |                     |                              |                  |
| 4          | N/C      | No Connection      |                     |                              |                  |
| 5          | N/C      | No Connection      |                     |                              |                  |

| Pin Number | Pin Name       | Description                          | Crossbar Capability | Additional Digital Functions          | Analog Functions                      |
|------------|----------------|--------------------------------------|---------------------|---------------------------------------|---------------------------------------|
| 6          | RSTb /<br>C2CK | Active-low Reset /<br>C2 Debug Clock |                     |                                       |                                       |
| 7          | P2.7 /<br>C2D  | Multifunction I/O /<br>C2 Debug Data |                     |                                       |                                       |
| 8          | XTAL4          | RTC Crystal                          |                     |                                       | XTAL4                                 |
| 9          | XTAL3          | RTC Crystal                          |                     |                                       | XTAL3                                 |
| 10         | P1.6           | Multifunction I/O                    | Yes                 |                                       | ADC0.14<br>CMP0P.7<br>CMP1P.7         |
| 11         | P1.5           | Multifunction I/O                    | Yes                 | P1MAT.5                               | ADC0.13<br>CMP0N.6<br>CMP1N.6         |
| 12         | P1.4           | Multifunction I/O                    | Yes                 | P1MAT.4                               | ADC0.12<br>CMP0P.6<br>CMP1P.6         |
| 13         | P1.3           | Multifunction I/O                    | Yes                 | P1MAT.3<br>SPI1_NSS                   | ADC0.11<br>CMP0N.5<br>CMP1N.5         |
| 14         | P1.2           | Multifunction I/O                    | Yes                 | P1MAT.2<br>SPI1_MOSI                  | ADC0.10<br>CMP0P.5<br>CMP1P.5         |
| 15         | P1.1           | Multifunction I/O                    | Yes                 | P1MAT.1<br>SPI1_MISO                  | ADC0.9<br>CMP0N.4<br>CMP1N.4          |
| 16         | P1.0           | Multifunction I/O                    | Yes                 | P1MAT.0<br>SPI1_SCK                   | ADC0.8<br>CMP0P.4<br>CMP1P.4          |
| 17         | P0.7           | Multifunction I/O                    | Yes                 | P0MAT.7<br>INT0.7<br>INT1.7           | ADC0.7<br>IREF0<br>CMP0N.3<br>CMP1N.3 |
| 18         | P0.6           | Multifunction I/O                    | Yes                 | P0MAT.6<br>CNVSTR<br>INT0.6<br>INT1.6 | ADC0.6<br>CMP0P.3<br>CMP1P.3          |

| Pin Number | Pin Name | Description       | Crossbar Capability | Additional Digital Functions          | Analog Functions                      |
|------------|----------|-------------------|---------------------|---------------------------------------|---------------------------------------|
| 19         | P0.5     | Multifunction I/O | Yes                 | P0MAT.5<br>INT0.5<br>INT1.5           | ADC0.5<br>CMP0N.2<br>CMP1N.2          |
| 20         | P0.4     | Multifunction I/O | Yes                 | P0MAT.4<br>INT0.4<br>INT1.4           | ADC0.4<br>CMP0P.2<br>CMP1P.2          |
| 21         | P0.3     | Multifunction I/O | Yes                 | P0MAT.3<br>EXTCLK<br>INT0.3<br>INT1.3 | ADC0.3<br>XTAL2<br>CMP0N.1<br>CMP1N.1 |
| 22         | P0.2     | Multifunction I/O | Yes                 | P0MAT.2<br>INT0.2<br>INT1.2           | ADC0.2<br>CMP0P.1<br>CMP1P.1<br>XTAL1 |
| 23         | P0.1     | Multifunction I/O | Yes                 | P0MAT.1<br>INT0.1<br>INT1.1           | ADC0.1<br>AGND<br>CMP0N.0<br>CMP1N.0  |
| 24         | P0.0     | Multifunction I/O | Yes                 | P0MAT.0<br>INT0.0<br>INT1.0           | ADC0.0<br>CMP0P.0<br>CMP1P.0<br>VREF  |
| Center     | GND      | Ground            |                     |                                       |                                       |

### 6.3 EFM8SB2x-QFP32 Pin Definitions

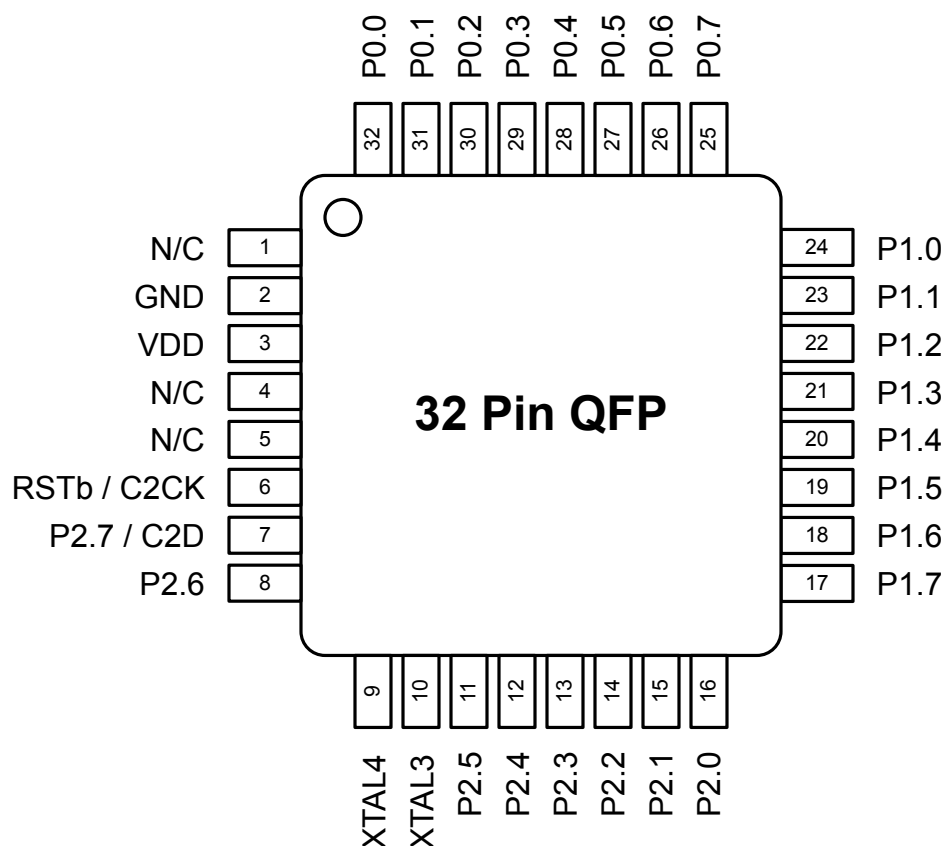


Figure 6.3. EFM8SB2x-QFP32 Pinout

Table 6.3. Pin Definitions for EFM8SB2x-QFP32

| Pin Number | Pin Name       | Description                          | Crossbar Capability | Additional Digital Functions | Analog Functions |
|------------|----------------|--------------------------------------|---------------------|------------------------------|------------------|
| 1          | N/C            | No Connection                        |                     |                              |                  |
| 2          | GND            | Ground                               |                     |                              |                  |
| 3          | VDD            | Supply Power Input                   |                     |                              |                  |
| 4          | N/C            | No Connection                        |                     |                              |                  |
| 5          | N/C            | No Connection                        |                     |                              |                  |
| 6          | RSTb /<br>C2CK | Active-low Reset /<br>C2 Debug Clock |                     |                              |                  |
| 7          | P2.7 /<br>C2D  | Multifunction I/O /<br>C2 Debug Data |                     |                              |                  |

| Pin Number | Pin Name | Description       | Crossbar Capability | Additional Digital Functions | Analog Functions                |
|------------|----------|-------------------|---------------------|------------------------------|---------------------------------|
| 8          | P2.6     | Multifunction I/O | Yes                 | EMIF_WRb                     | ADC0.22<br>CMP0P.11<br>CMP1P.11 |
| 9          | XTAL4    | RTC Crystal       |                     |                              | XTAL4                           |
| 10         | XTAL3    | RTC Crystal       |                     |                              | XTAL3                           |
| 11         | P2.5     | Multifunction I/O | Yes                 | EMIF_RDb                     | ADC0.21<br>CMP0N.10<br>CMP1N.10 |
| 12         | P2.4     | Multifunction I/O | Yes                 | EMIF_ALE                     | ADC0.20<br>CMP0P.10<br>CMP1P.10 |
| 13         | P2.3     | Multifunction I/O | Yes                 | EMIF_A11                     | ADC0.19<br>CMP0N.9<br>CMP1N.9   |
| 14         | P2.2     | Multifunction I/O | Yes                 | EMIF_A10                     | ADC0.18<br>CMP0P.9<br>CMP1P.9   |
| 15         | P2.1     | Multifunction I/O | Yes                 | EMIF_A9                      | ADC0.17<br>CMP0N.8<br>CMP1N.8   |
| 16         | P2.0     | Multifunction I/O | Yes                 | EMIF_A8                      | ADC0.16<br>CMP0P.8<br>CMP1P.8   |
| 17         | P1.7     | Multifunction I/O | Yes                 | P1MAT.7<br>EMIF_AD7          | ADC0.15<br>CMP0N.7<br>CMP1N.7   |
| 18         | P1.6     | Multifunction I/O | Yes                 | P1MAT.6<br>EMIF_AD6          | ADC0.14<br>CMP0P.7<br>CMP1P.7   |
| 19         | P1.5     | Multifunction I/O | Yes                 | P1MAT.5<br>EMIF_AD5          | ADC0.13<br>CMP0N.6<br>CMP1N.6   |
| 20         | P1.4     | Multifunction I/O | Yes                 | P1MAT.4<br>EMIF_AD4          | ADC0.12<br>CMP0P.6<br>CMP1P.6   |



| Pin Number | Pin Name | Description       | Crossbar Capability | Additional Digital Functions          | Analog Functions                      |
|------------|----------|-------------------|---------------------|---------------------------------------|---------------------------------------|
| 21         | P1.3     | Multifunction I/O | Yes                 | P1MAT.3<br>SPI1_NSS<br>EMIF_AD3       | ADC0.11<br>CMP0N.5<br>CMP1N.5         |
| 22         | P1.2     | Multifunction I/O | Yes                 | P1MAT.2<br>SPI1_MOSI<br>EMIF_AD2      | ADC0.10<br>CMP0P.5<br>CMP1P.5         |
| 23         | P1.1     | Multifunction I/O | Yes                 | P1MAT.1<br>SPI1_MISO<br>EMIF_AD1      | ADC0.9<br>CMP0N.4<br>CMP1N.4          |
| 24         | P1.0     | Multifunction I/O | Yes                 | P1MAT.0<br>SPI1_SCK<br>EMIF_AD0       | ADC0.8<br>CMP0P.4<br>CMP1P.4          |
| 25         | P0.7     | Multifunction I/O | Yes                 | P0MAT.7<br>INT0.7<br>INT1.7           | ADC0.7<br>IREF0<br>CMP0N.3<br>CMP1N.3 |
| 26         | P0.6     | Multifunction I/O | Yes                 | P0MAT.6<br>CNVSTR<br>INT0.6<br>INT1.6 | ADC0.6<br>CMP0P.3<br>CMP1P.3          |
| 27         | P0.5     | Multifunction I/O | Yes                 | P0MAT.5<br>INT0.5<br>INT1.5           | ADC0.5<br>CMP0N.2<br>CMP1N.2          |
| 28         | P0.4     | Multifunction I/O | Yes                 | P0MAT.4<br>INT0.4<br>INT1.4           | ADC0.4<br>CMP0P.2<br>CMP1P.2          |
| 29         | P0.3     | Multifunction I/O | Yes                 | P0MAT.3<br>EXTCLK<br>INT0.3<br>INT1.3 | ADC0.3<br>XTAL2<br>CMP0N.1<br>CMP1N.1 |
| 30         | P0.2     | Multifunction I/O | Yes                 | P0MAT.2<br>INT0.2<br>INT1.2           | ADC0.2<br>CMP0P.1<br>CMP1P.1<br>XTAL1 |

| Pin Number | Pin Name | Description       | Crossbar Capability | Additional Digital Functions | Analog Functions                     |
|------------|----------|-------------------|---------------------|------------------------------|--------------------------------------|
| 31         | P0.1     | Multifunction I/O | Yes                 | P0MAT.1<br>INT0.1<br>INT1.1  | ADC0.1<br>AGND<br>CMP0N.0<br>CMP1N.0 |
| 32         | P0.0     | Multifunction I/O | Yes                 | P0MAT.0<br>INT0.0<br>INT1.0  | ADC0.0<br>CMP0P.0<br>CMP1P.0<br>VREF |

## 7. QFN32 Package Specifications

### 7.1 QFN32 Package Dimensions

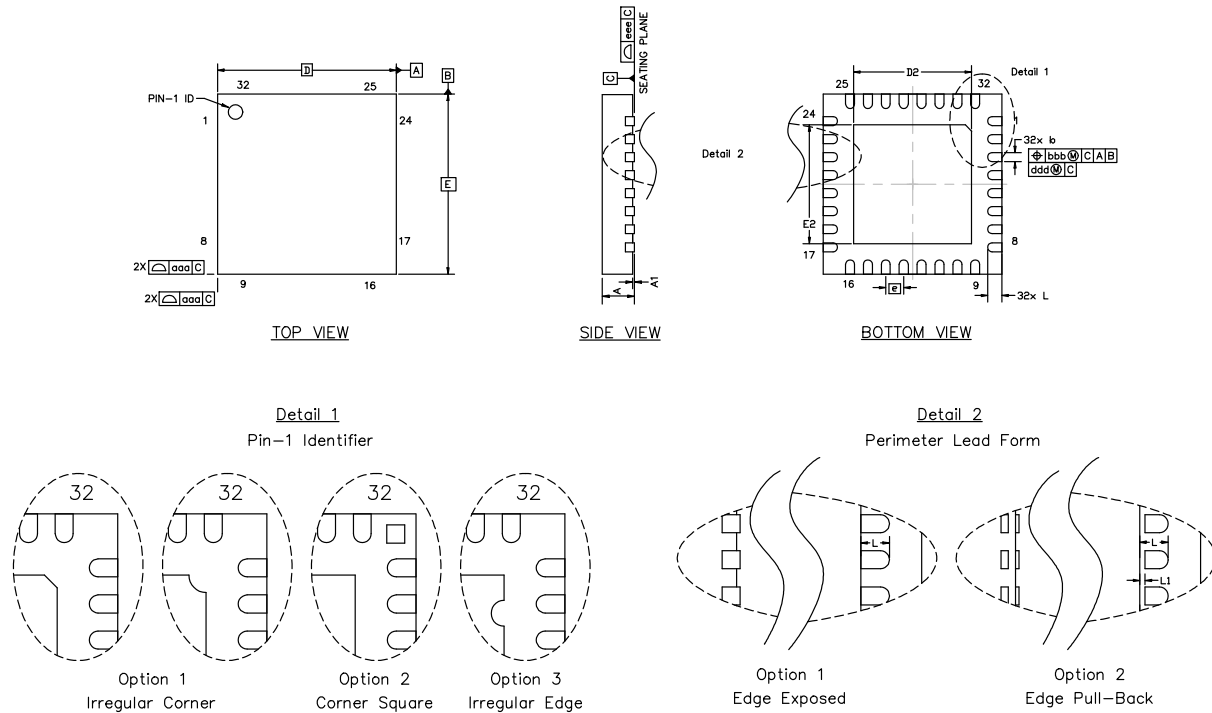


Figure 7.1. QFN32 Package Drawing

Table 7.1. QFN32 Package Dimensions

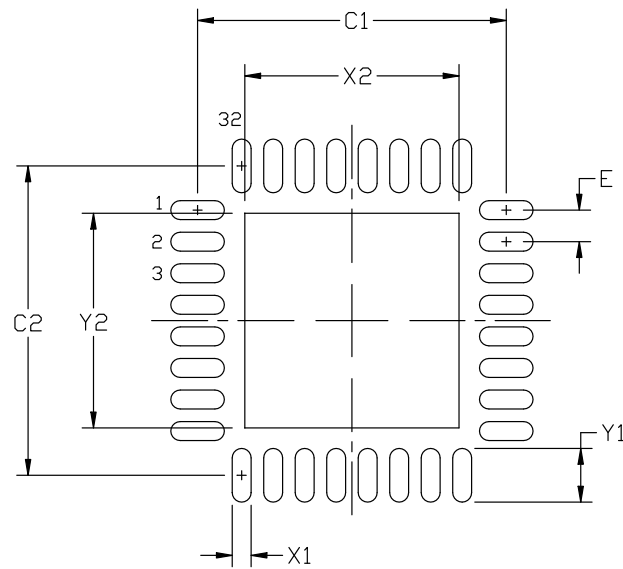
| Dimension | Min      | Typ  | Max  |
|-----------|----------|------|------|
| A         | 0.80     | 0.90 | 1.00 |
| A1        | 0.00     | 0.02 | 0.05 |
| b         | 0.18     | 0.25 | 0.30 |
| D         | 5.00 BSC |      |      |
| D2        | 3.20     | 3.30 | 3.40 |
| e         | 0.50 BSC |      |      |
| E         | 5.00 BSC |      |      |
| E2        | 3.20     | 3.30 | 3.40 |
| L         | 0.30     | 0.40 | 0.50 |
| L1        | 0.00     | —    | 0.15 |
| aaa       | —        | —    | 0.15 |

| Dimension | Min | Typ | Max  |
|-----------|-----|-----|------|
| bbb       | —   | —   | 0.10 |
| ddd       | —   | —   | 0.05 |
| eee       | —   | —   | 0.08 |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation VHHD except for custom features D2, E2, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

## 7.2 QFN32 PCB Land Pattern



**Figure 7.2. QFN32 PCB Land Pattern Drawing**

**Table 7.2. QFN32 PCB Land Pattern Dimensions**

| Dimension | Min      | Max  |
|-----------|----------|------|
| C1        | 4.80     | 4.90 |
| C2        | 4.80     | 4.90 |
| E         | 0.50 BSC |      |
| X1        | 0.20     | 0.30 |
| X2        | 3.20     | 3.40 |
| Y1        | 0.75     | 0.85 |
| Y2        | 3.20     | 3.40 |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu\text{m}$  minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 3 x 3 array of 1.0 mm x 1.0 mm openings on a 1.2 mm pitch should be used for the center pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

### 7.3 QFN32 Package Marking



Figure 7.3. QFN32 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

## 8. QFN24 Package Specifications

### 8.1 QFN24 Package Dimensions

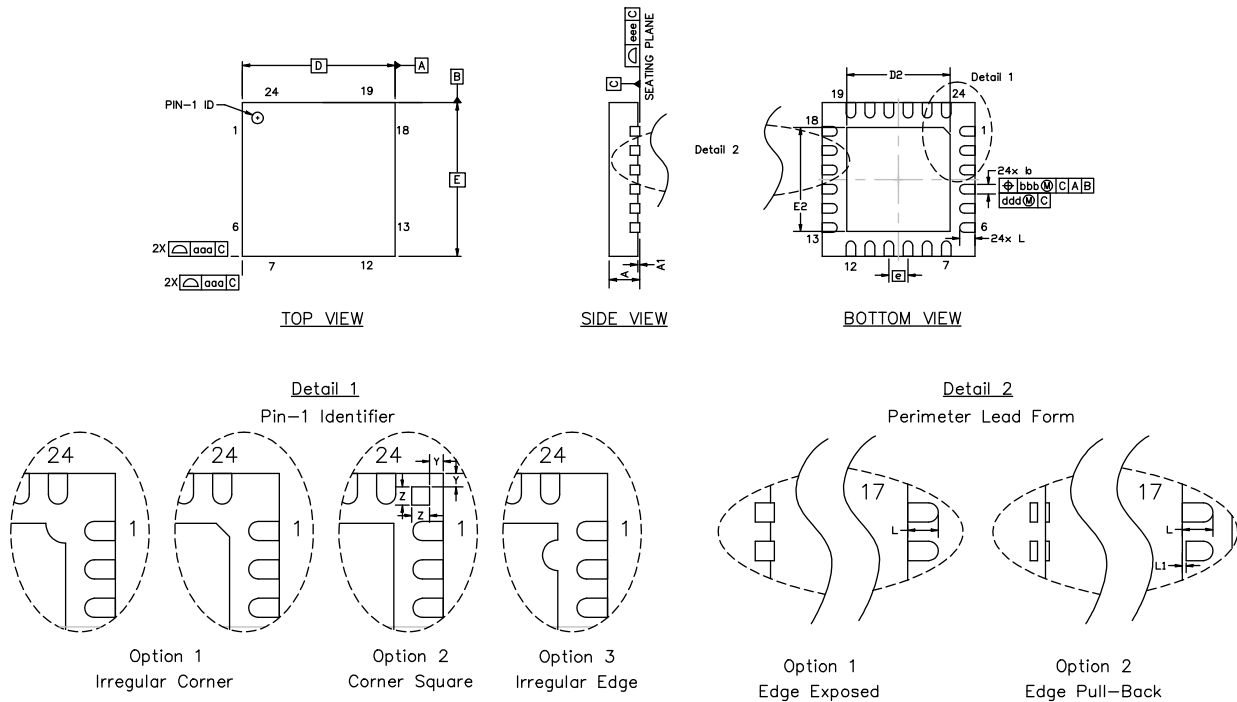


Figure 8.1. QFN24 Package Drawing

Table 8.1. QFN24 Package Dimensions

| Dimension | Min      | Typ  | Max  |
|-----------|----------|------|------|
| A         | 0.70     | 0.75 | 0.80 |
| A1        | 0.00     | 0.02 | 0.05 |
| b         | 0.18     | 0.25 | 0.30 |
| D         | 4.00 BSC |      |      |
| D2        | 2.55     | 2.70 | 2.80 |
| e         | 0.50 BSC |      |      |
| E         | 4.00 BSC |      |      |
| E2        | 2.55     | 2.70 | 2.80 |
| L         | 0.30     | 0.40 | 0.50 |
| L1        | 0.00     | —    | 0.15 |
| aaa       | —        | —    | 0.15 |

| Dimension | Min | Typ  | Max  |
|-----------|-----|------|------|
| bbb       | —   | —    | 0.10 |
| ddd       | —   | —    | 0.05 |
| eee       | —   | —    | 0.08 |
| Z         | —   | 0.24 | —    |
| Y         | —   | 0.18 | —    |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation WGGD except for custom features D2, E2, Z, Y, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.



## 8.2 QFN24 PCB Land Pattern

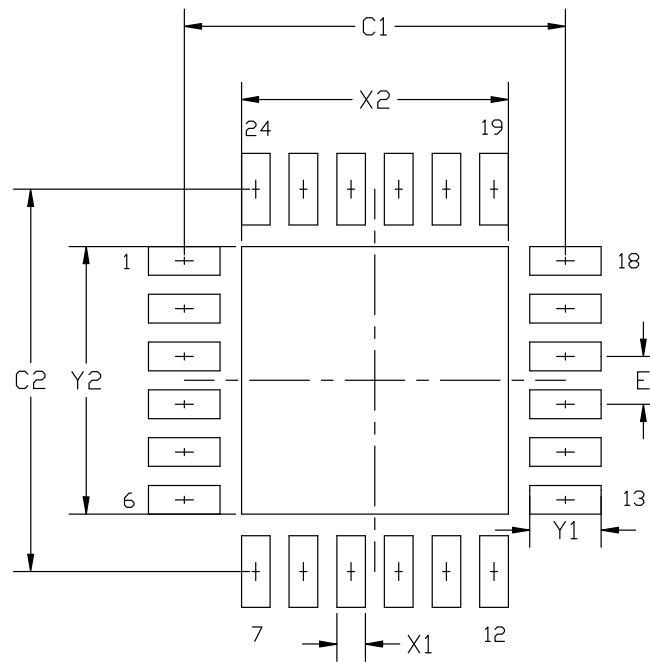


Figure 8.2. QFN24 PCB Land Pattern Drawing

Table 8.2. QFN24 PCB Land Pattern Dimensions

| Dimension | Min      | Max  |
|-----------|----------|------|
| C1        | 3.90     | 4.00 |
| C2        | 3.90     | 4.00 |
| E         | 0.50 BSC |      |
| X1        | 0.20     | 0.30 |
| X2        | 2.70     | 2.80 |
| Y1        | 0.65     | 0.75 |
| Y2        | 2.70     | 2.80 |

| Dimension   | Min | Max |
|---|-----|-----|
| <b>Note:</b> <ol style="list-style-type: none"> <li>1. All dimensions shown are in millimeters (mm) unless otherwise noted.</li> <li>2. This Land Pattern Design is based on the IPC-7351 guidelines.</li> <li>3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 <math>\mu\text{m}</math> minimum, all the way around the pad.</li> <li>4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.</li> <li>5. The stencil thickness should be 0.125 mm (5 mils).</li> <li>6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.</li> <li>7. A 2 x 2 array of 1.10 mm x 1.10 mm openings on 1.30 mm pitch should be used for the center ground pad.</li> <li>8. A No-Clean, Type-3 solder paste is recommended.</li> <li>9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.</li> </ol> |     |     |

### 8.3 QFN24 Package Marking



Figure 8.3. QFN24 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

## 9. QFP32 Package Specifications

### 9.1 QFP32 Package Dimensions

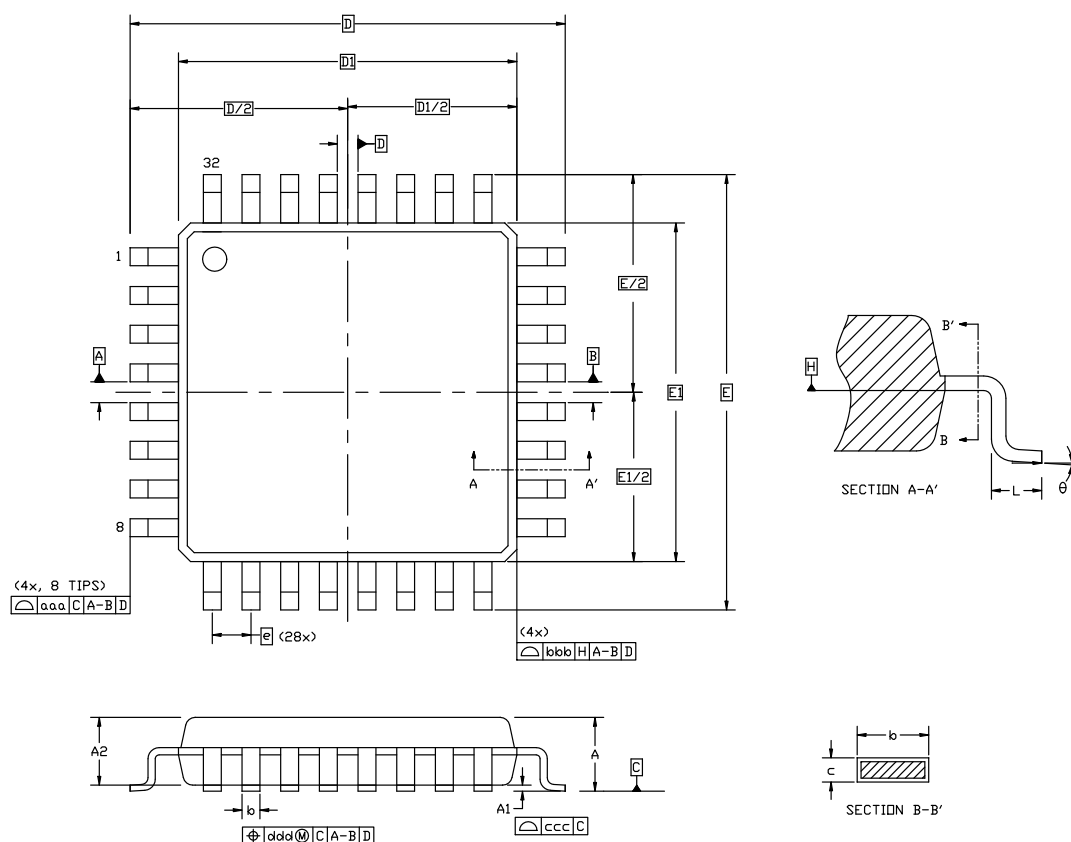


Figure 9.1. QFP32 Package Drawing

Table 9.1. QFP32 Package Dimensions

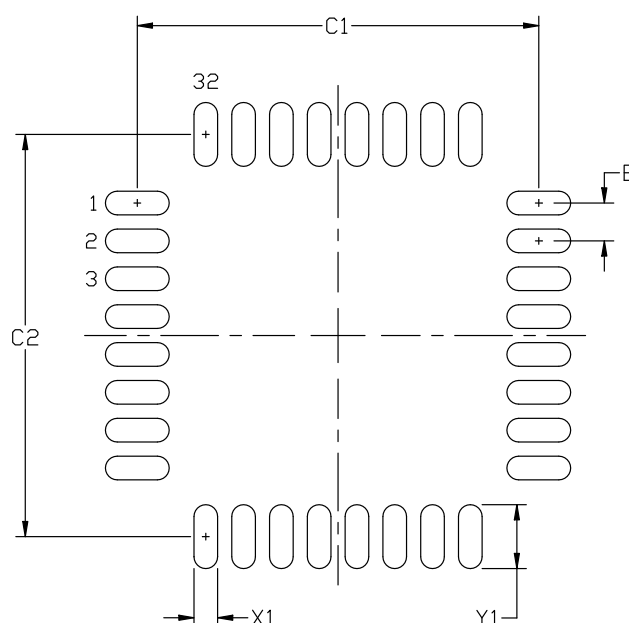
| Dimension | Min      | Typ  | Max  |
|-----------|----------|------|------|
| A         | —        | —    | 1.60 |
| A1        | 0.05     | —    | 0.15 |
| A2        | 1.35     | 1.40 | 1.45 |
| b         | 0.30     | 0.37 | 0.45 |
| D         | 9.00 BSC |      |      |
| D1        | 7.00 BSC |      |      |
| e         | 0.80 BSC |      |      |
| E         | 9.00 BSC |      |      |
| E1        | 7.00 BSC |      |      |
| L         | 0.45     | 0.60 | 0.75 |
| aaa       | 0.20     |      |      |

| Dimension | Min  | Typ  | Max |
|-----------|------|------|-----|
| bbb       | 0.20 |      |     |
| ccc       | 0.10 |      |     |
| ddd       | 0.20 |      |     |
| theta     | 0°   | 3.5° | 7°  |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation BBA.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

## 9.2 QFP32 PCB Land Pattern



**Figure 9.2. QFP32 PCB Land Pattern Drawing**

**Table 9.2. QFP32 PCB Land Pattern Dimensions**

| Dimension | Min      | Max  |
|-----------|----------|------|
| C1        | 8.40     | 8.50 |
| C2        | 8.40     | 8.50 |
| E         | 0.80 BSC |      |
| X1        | 0.40     | 0.50 |
| Y1        | 1.25     | 1.35 |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu\text{m}$  minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

### 9.3 QFP32 Package Marking

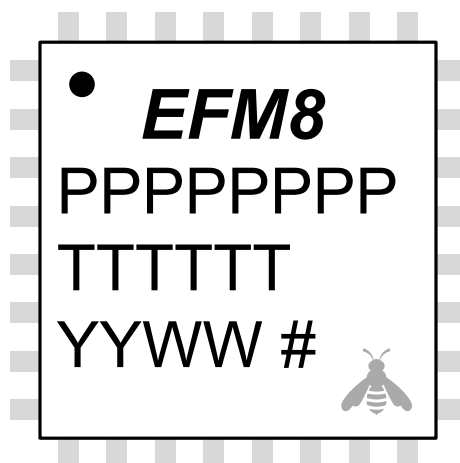


Figure 9.3. QFP32 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

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