

N-channel 800 V, 0.15  $\Omega$  typ., 24 A, MDmesh™ K5

Power MOSFET in a TO-247 package

Datasheet - production data

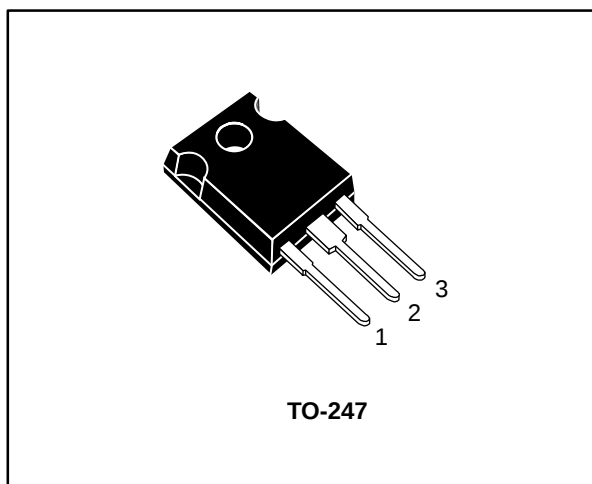
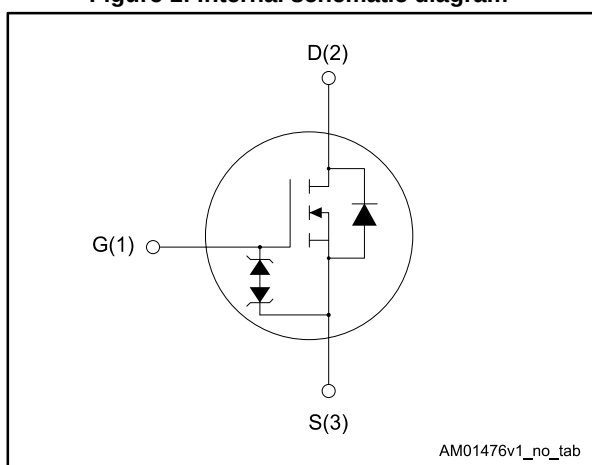


Figure 1: Internal schematic diagram



## Features table

| Order code | V <sub>DS</sub> | R <sub>DS(on)</sub> max. | I <sub>D</sub> |
|------------|-----------------|--------------------------|----------------|
| STW30N80K5 | 800 V           | 0.18 $\Omega$            | 24 A           |

## Features

- Industry's lowest R<sub>DS(on)</sub> x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

## Applications

- Switching applications

## Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

| Order code | Marking | Package | Packing |
|------------|---------|---------|---------|
| STW30N80K5 | 30N80K5 | TO-247  | Tube    |

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## Contents

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol         | Parameter                                                         | Value       | Unit               |
|----------------|-------------------------------------------------------------------|-------------|--------------------|
| $V_{DS}$       | Drain-source voltage                                              | 800         | V                  |
| $V_{GS}$       | Gate-source voltage                                               | $\pm 30$    | V                  |
| $I_D$          | Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$  | 24          | A                  |
| $I_D$          | Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$ | 15          | A                  |
| $I_{DM}^{(1)}$ | Drain current (pulsed)                                            | 96          | A                  |
| $P_{TOT}$      | Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$           | 250         | W                  |
| $dv/dt^{(2)}$  | Peak diode recovery voltage slope                                 | 4.5         | V/ns               |
| $dv/dt^{(3)}$  | MOSFET $dv/dt$ ruggedness                                         | 50          |                    |
| $T_{stg}$      | Storage temperature range                                         | - 55 to 150 | $^{\circ}\text{C}$ |
| $T_j$          | Operating junction temperature range                              |             |                    |

**Notes:**

(1)Pulse width limited by safe operating area

(2) $I_{SD} < 24\text{ A}$ ,  $di/dt < 100\text{ A}/\mu\text{s}$ ,  $V_{DSpeak} < V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ (3) $V_{DS} = 640\text{ V}$ 

Table 3: Thermal data

| Symbol         | Parameter                           | Value | Unit                        |
|----------------|-------------------------------------|-------|-----------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case    | 0.5   | $^{\circ}\text{C}/\text{W}$ |
| $R_{thj-amb}$  | Thermal resistance junction-ambient | 50    | $^{\circ}\text{C}/\text{W}$ |

Table 4: Avalanche characteristics

| Symbol   | Parameter                                                                                                                 | Value | Unit |
|----------|---------------------------------------------------------------------------------------------------------------------------|-------|------|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive<br>(pulse width limited by $T_{jmax.}$ )                                  | 8     | A    |
| $E_{AS}$ | Single pulse avalanche energy<br>(starting $T_j = 25\text{ }^{\circ}\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ ) | 440   | mJ   |

## 2 Electrical characteristics

(T<sub>CASE</sub> = 25 °C unless otherwise specified)

Table 5: On/off states

| Symbol               | Parameter                         | Test conditions                                                                        | Min. | Typ. | Max. | Unit |
|----------------------|-----------------------------------|----------------------------------------------------------------------------------------|------|------|------|------|
| V <sub>(BR)DSS</sub> | Drain-source breakdown voltage    | I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0 V                                           | 800  |      |      | V    |
| I <sub>DSS</sub>     | Zero gate voltage drain current   | V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 800 V                                         |      |      | 1    | μA   |
|                      |                                   | V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 800 V, T <sub>C</sub> = 125 °C <sup>(1)</sup> |      |      | 50   | μA   |
| I <sub>GSS</sub>     | Gate source leakage current       | V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V                                        |      |      | ±10  | μA   |
| V <sub>GS(th)</sub>  | Gate threshold voltage            | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100 μA                            | 3    | 4    | 5    | V    |
| R <sub>DS(on)</sub>  | Static drain-source on-resistance | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 12 A                                          |      | 0.15 | 0.18 | Ω    |

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test

Table 6: Dynamic

| Symbol                            | Parameter                             | Test conditions                                                                                                                       | Min. | Typ. | Max. | Unit |
|-----------------------------------|---------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| C <sub>iss</sub>                  | Input capacitance                     | V <sub>DS</sub> = 100 V, f = 1 MHz, V <sub>GS</sub> = 0 V                                                                             | -    | 1530 | -    | pF   |
| C <sub>oss</sub>                  | Output capacitance                    |                                                                                                                                       | -    | 145  | -    | pF   |
| C <sub>rss</sub>                  | Reverse transfer capacitance          |                                                                                                                                       | -    | 1.2  | -    | pF   |
| C <sub>o(er)</sub> <sup>(1)</sup> | Equivalent capacitance energy related | V <sub>GS</sub> = 0 V,<br>V <sub>DS</sub> = 0 to 640 V                                                                                | -    | 91   | -    | pF   |
| C <sub>o(tr)</sub> <sup>(2)</sup> | Equivalent capacitance time related   |                                                                                                                                       | -    | 244  | -    | pF   |
| Q <sub>g</sub>                    | Total gate charge                     | V <sub>DD</sub> = 640 V, I <sub>D</sub> = 24 A,<br>V <sub>GS</sub> = 10 V<br>(See Figure 16: "Test circuit for gate charge behavior") | -    | 43   | -    | nC   |
| Q <sub>gs</sub>                   | Gate-source charge                    |                                                                                                                                       | -    | 12.8 | -    | nC   |
| Q <sub>gd</sub>                   | Gate-drain charge                     |                                                                                                                                       | -    | 24.2 | -    | nC   |
| R <sub>g</sub>                    | Gate input resistance                 | f = 1 MHz, I <sub>D</sub> = 0 A                                                                                                       | -    | 3.5  | -    | Ω    |

**Notes:**

<sup>(1)</sup>Energy related is defined as a constant equivalent capacitance giving the same stored energy as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>

<sup>(2)</sup>Time related is defined as a constant equivalent capacitance giving the same stored energy as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>

Table 7: Switching times

| Symbol       | Parameter           | Test conditions                                                                                                                                                                                                                               | Min. | Typ. | Max. | Unit |
|--------------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DS} = 400\text{ V}$ , $I_D = 12\text{ A}$ , $R_G = 4.7\ \Omega$<br>$V_{GS} = 10\text{ V}$<br>(See <a href="#">Figure 15: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 20: "Switching time waveform"</a> ) | -    | 21   | -    | ns   |
| $t_r$        | Rise time           |                                                                                                                                                                                                                                               | -    | 15   | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time |                                                                                                                                                                                                                                               | -    | 100  | -    | ns   |
| $t_f$        | Fall time           |                                                                                                                                                                                                                                               | -    | 13.5 | -    | ns   |

Table 8: Source-drain diode

| Symbol          | Parameter                     | Test conditions                                                                                                                                                                                                                     | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |                                                                                                                                                                                                                                     | -    |      | 24   | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |                                                                                                                                                                                                                                     | -    |      | 96   | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{SD} = 24\text{ A}$ , $V_{GS} = 0\text{ V}$                                                                                                                                                                                      | -    |      | 1.5  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 24\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$<br>$V_{DD} = 60\text{ V}$<br>(See <a href="#">Figure 17: "Test circuit for inductive load switching and diode recovery times"</a> )                                     | -    | 555  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                                     | -    | 9.95 |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                                     | -    | 36   |      | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 24\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$<br>$V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$<br>(See <a href="#">Figure 17: "Test circuit for inductive load switching and diode recovery times"</a> ) | -    | 765  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                                     | -    | 13.2 |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                                     | -    | 34.5 |      | A             |

**Notes:**

<sup>(1)</sup>Pulse width limited by safe operating area.

<sup>(2)</sup>Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

Table 9: Gate-source Zener diode

| Symbol        | Parameter                     | Test conditions                                 | Min. | Typ. | Max. | Unit |
|---------------|-------------------------------|-------------------------------------------------|------|------|------|------|
| $V_{(BR)GSO}$ | Gate-source breakdown voltage | $I_{GS} = \pm 1\text{ mA}$ , $I_D = 0\text{ A}$ | 30   | -    | -    | V    |

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

## 2.1 Electrical characteristics (curves)

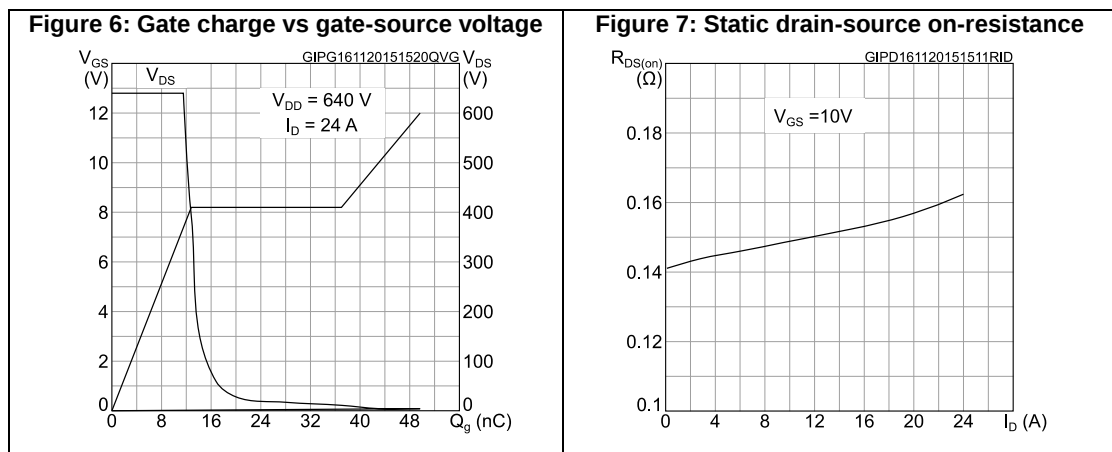
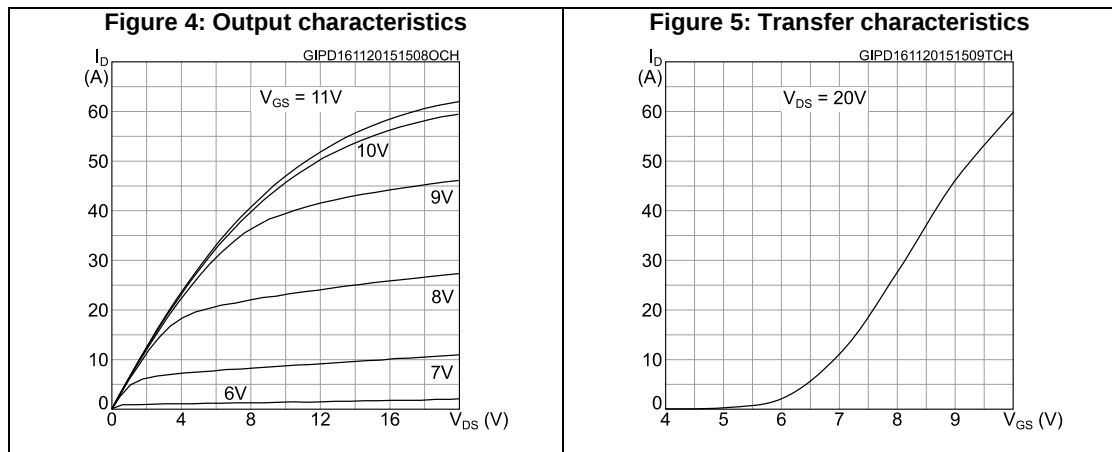
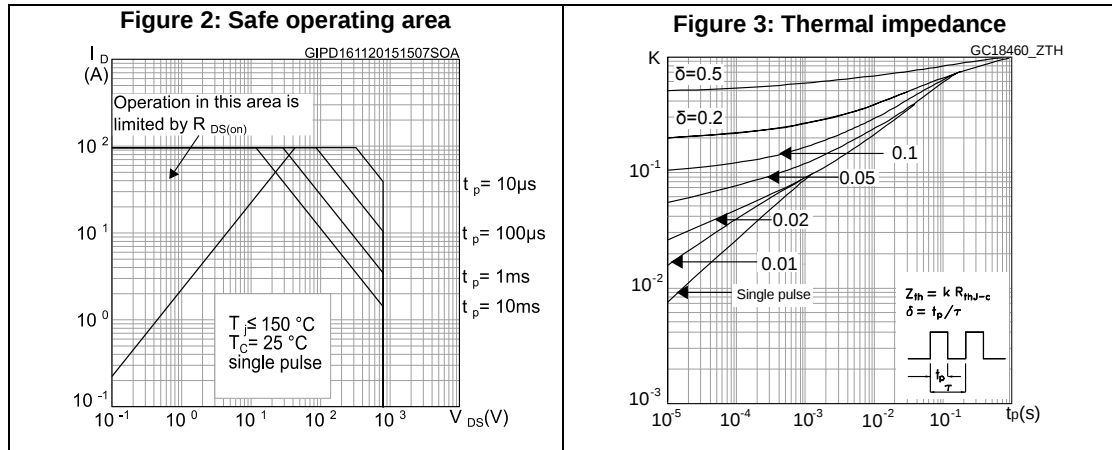


Figure 8: Capacitance variations

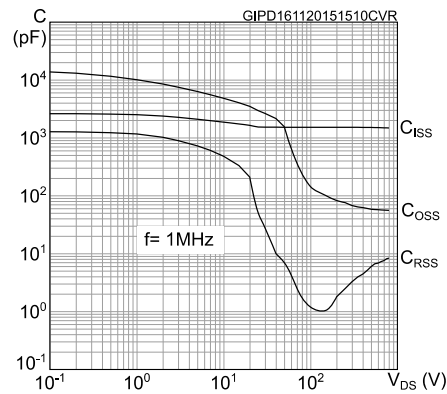


Figure 9: Normalized gate threshold voltage vs temperature

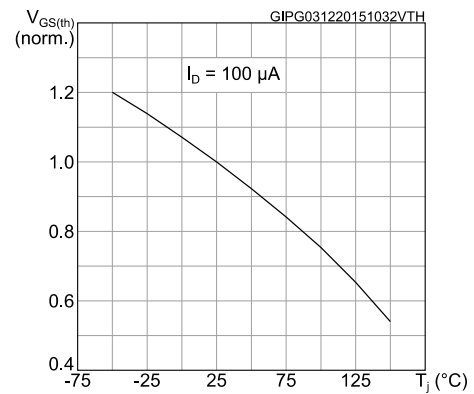


Figure 10: Normalized on-resistance vs temperature

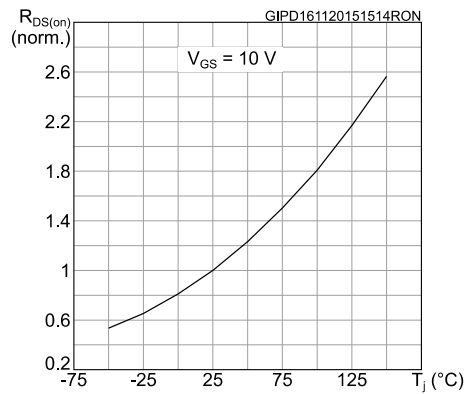


Figure 11: Normalized V(BR)DSS vs temperature

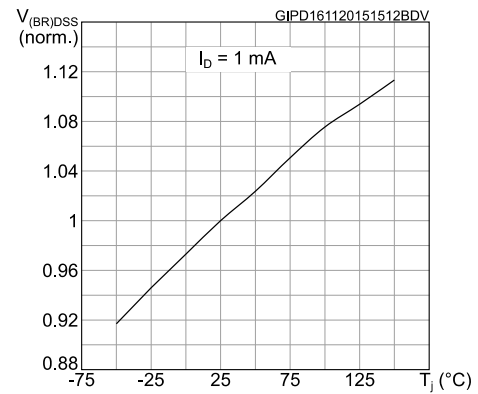


Figure 12: Maximum avalanche energy vs starting T\_J

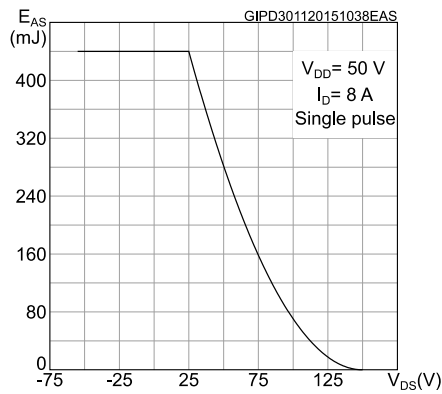


Figure 13: Source-drain diode forward characteristics

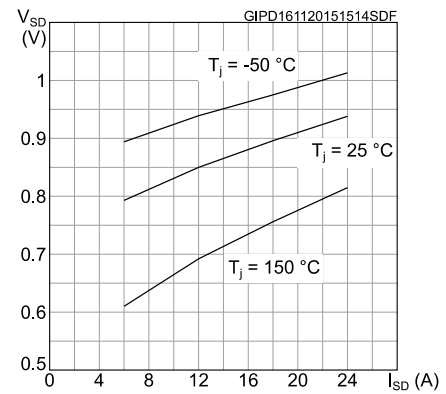
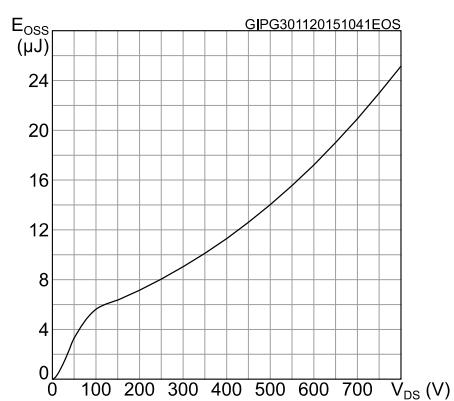
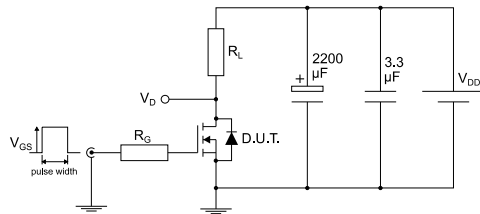


Figure 14: Output capacitance stored energy



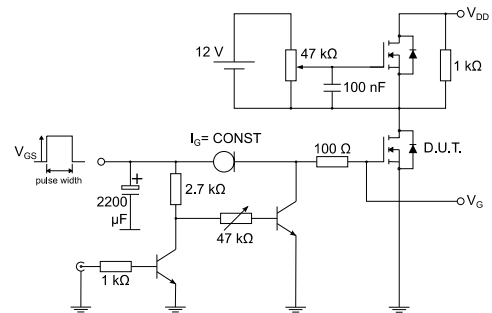
### 3 Test circuits

**Figure 15: Test circuit for resistive load switching times**



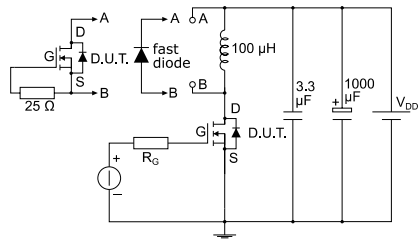
AM01468v1

**Figure 16: Test circuit for gate charge behavior**



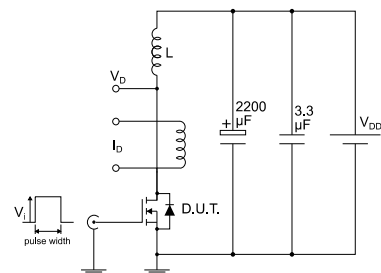
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**Figure 17: Test circuit for inductive load switching and diode recovery times**



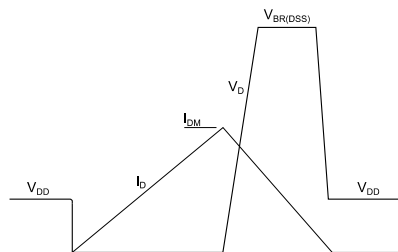
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**Figure 18: Unclamped inductive load test circuit**



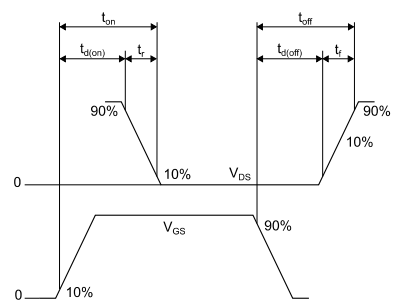
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**Figure 19: Unclamped inductive waveform**



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**Figure 20: Switching time waveform**



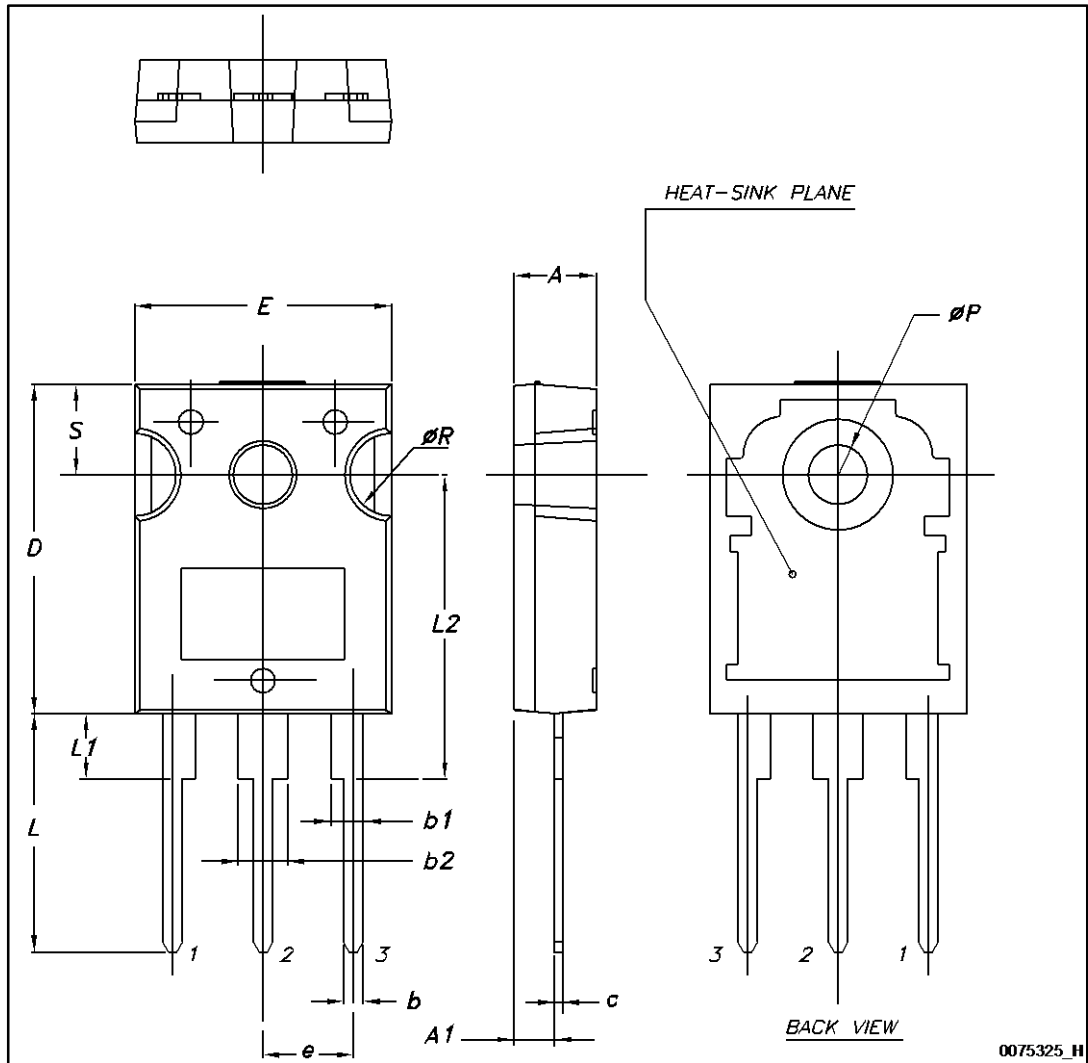
AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 TO-247 package information

Figure 21: TO-247 package outline



0075325\_H

Table 10: TO-247 package mechanical data

| Dim. | mm.   |       |       |
|------|-------|-------|-------|
|      | Min.  | Typ.  | Max.  |
| A    | 4.85  |       | 5.15  |
| A1   | 2.20  |       | 2.60  |
| b    | 1.0   |       | 1.40  |
| b1   | 2.0   |       | 2.40  |
| b2   | 3.0   |       | 3.40  |
| c    | 0.40  |       | 0.80  |
| D    | 19.85 |       | 20.15 |
| E    | 15.45 |       | 15.75 |
| e    | 5.30  | 5.45  | 5.60  |
| L    | 14.20 |       | 14.80 |
| L1   | 3.70  |       | 4.30  |
| L2   |       | 18.50 |       |
| ØP   | 3.55  |       | 3.65  |
| ØR   | 4.50  |       | 5.50  |
| S    | 5.30  | 5.50  | 5.70  |

## 5 Revision history

**Table 11: Document revision history**

| Date        | Revision | Changes                                                                              |
|-------------|----------|--------------------------------------------------------------------------------------|
| 03-Dec-2015 | 1        | First release.                                                                       |
| 21-Mar-2016 | 2        | Document status promoted from preliminary to production data.<br>Minor text changes. |

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