

# SNx4AHCT595 8-Bit Shift Registers With 3-State Output Registers

## 1 Features

- Inputs are TTL-voltage compatible
- 8-bit serial-in, parallel-out shift
- Shift register has direct clear
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD protection exceeds JESD 22:
  - 2000V Human-Body Model (A114-A)
  - 200V Machine Model (A115-A)
  - 1000V Charged-Device Model (C101)

## 2 Applications

- Network switches
- Power infrastructures
- PCs and notebooks
- LED displays
- Servers

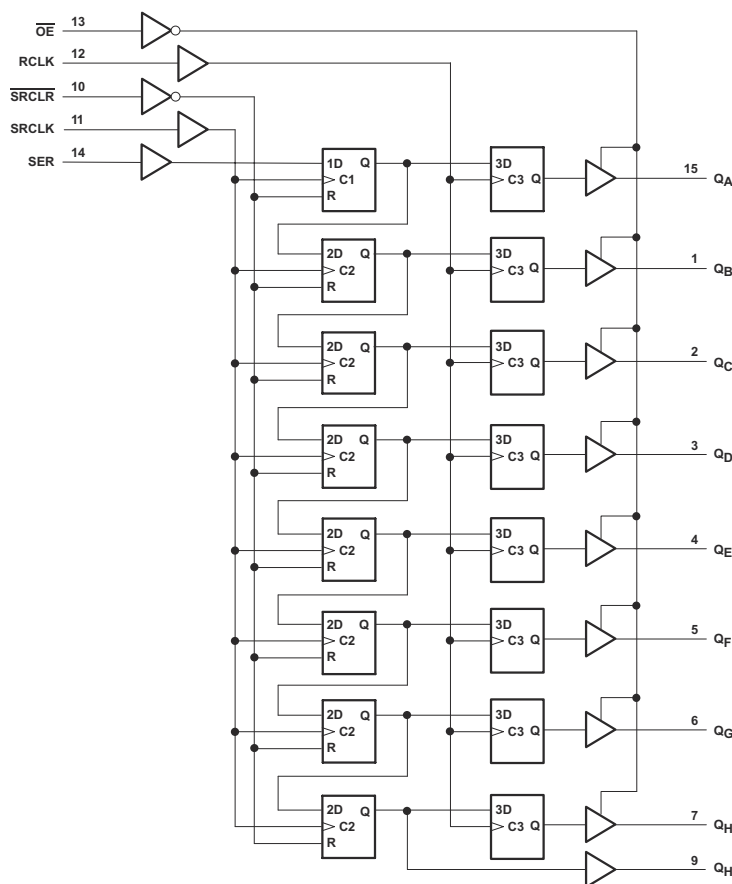
## 3 Description

The SNx4AHCT595 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE (NOM) <sup>(3)</sup>
SNx4AHCT595	BQB (WQFN, 16)	3.5mm × 2.5mm	3.5mm × 2.5mm
	PW (TSSOP, 16)	5.0mm × 6.4mm	5.0mm × 4.4mm

- For more information, see [Section 11](#).
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



Pin numbers shown are for the PW and BQB packages.

### Simplified Schematic

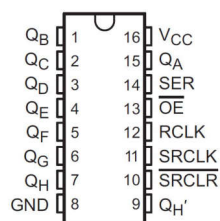


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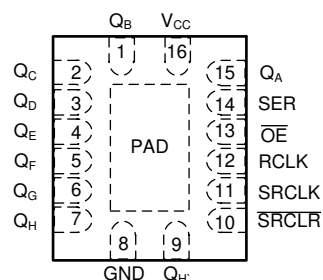
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## 4 Pin Configuration and Functions



**Figure 4-1.**  
**SN74AHCT595-Q1 PW Package (Top View)**



**Figure 4-2. SN74AHCT595-Q1 BQB Package, 16-Pin WQFN (Top View)**

**Table 4-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
Q <sub>B</sub>	1	O	Q <sub>B</sub> Output
Q <sub>C</sub>	2	O	Q <sub>C</sub> Output
Q <sub>D</sub>	3	O	Q <sub>D</sub> Output
Q <sub>E</sub>	4	O	Q <sub>E</sub> Output
Q <sub>F</sub>	5	O	Q <sub>F</sub> Output
Q <sub>G</sub>	6	O	Q <sub>G</sub> Output
Q <sub>H</sub>	7	O	Q <sub>H</sub> Output
GND	8	—	Ground Pin
Q <sub>H</sub> '	9	O	Q <sub>H</sub> ' Output
SRCLR	10	I	SRCLR Input
SRCLK	11	I	SRCLK Input
RCLK	12	I	RCLK Input
OE	13	I	Output Enable
SER	14	I	SER Input
Q <sub>A</sub>	15	O	Q <sub>A</sub> Output
V <sub>CC</sub>	16	—	Power Pin
Thermal Pad <sup>(2)</sup>		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) I = input, O = output

(2) BQB package only

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		-0.5	7	V
$V_I$	Input voltage range <sup>(2)</sup>		-0.5	7	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>		-0.5	7	V
$V_O$	Output voltage range <sup>(2)</sup>		-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < -0.5V$		-20	mA
$I_{OK}$	Output clamp current	$V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$		$\pm 20$	mA
$I_O$	Continuous output current	$V_O = 0$ to $V_{CC}$		$\pm 25$	mA
	Continuous output current through $V_{CC}$ or GND			$\pm 75$	mA
$T_J$	Junction temperature			150	°C
$T_{slg}$	Storage temperature		-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	$\pm 2000$	V

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specification	Description	Condition	MIN	MAX	UNIT
$V_{CC}$	Supply voltage		4.5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 5V$	2		V
$V_{IL}$	Low-Level input voltage	$V_{CC} = 5V$		0.8	V
$V_I$	Input Voltage		0	5.5	V
$V_O$	Output Voltage		0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 5V \pm 0.5V$		-8	mA
$I_{OL}$	Low-level output current	$V_{CC} = 5V \pm 0.5V$		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 5V \pm 0.5V$		20	ns/V
$T_A$	Operating free-air temperature		-40	125	°C

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AHCT595						UNIT
		BQB (WQFN)	D (SOIC)	DB (SSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	
		16 PINS						
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	91.8	93.8	97.5	47.5	126.2	135.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	87.7	54.7	47.7	34.9	68.7	70.3	
R <sub>θJB</sub>	Junction-to-board thermal resistance	61.6	50.9	48.1	27.5	77.3	81.3	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	11.9	20.8	9.8	19.8	22.3	22.5	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	61.4	50.7	47.6	27.4	76.9	80.8	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	39.4	N/A	N/A	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50μA	4.5V	4.4	4.5		4.4			V
	I <sub>OH</sub> = -8mA	4.5V	3.94			3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50μA	4.5V			0.1			0.1	V
	I <sub>OL</sub> = 8mA	4.5V			0.36			0.44	
I <sub>I</sub>	V <sub>I</sub> = 5.5V or GND and V <sub>CC</sub> = 0V to 5.5V	0V to 5.5V			±0.1			±1	μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND and V <sub>CC</sub> = 5.5V	5.5V			±0.25			±2.5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0, and V <sub>CC</sub> = 5.5V	5.5V			4			40	μA
ΔI <sub>CC</sub>	One input at 3.4V, Other inputs at V <sub>CC</sub> or GND	5V			1.35			1.5	mA
C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5V		4	10			10	pF
C <sub>O</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5V		5					pF
C <sub>PD</sub>	No load, F = 1MHz	5V		129					pF

## 5.6 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V <sub>CC</sub>	T <sub>A</sub> = 25°C		-40°C to 125°C		UNIT
				MIN	MAX	MIN	MAX	
t <sub>H</sub>	Hold time	SER after SRCLK↑	5V ± 0.5V	2		2		ns
t <sub>SU</sub>	Setup time	SER before SRCLK↑	5V ± 0.5V	3		3		ns
t <sub>SU</sub>	Setup time	SRCLK↑ before RCLK↑	5V ± 0.5V	5		5		ns
t <sub>SU</sub>	Setup time	SRCLR high (inactive) before SRCLK↑	5V ± 0.5V	2.9		3.8		ns
t <sub>SU</sub>	Setup time	SRCLR low before RCLK↑	5V ± 0.5V	5		5		ns
t <sub>W</sub>	Pulse duration	RCLK or SRCLK high or low	5V ± 0.5V	5		5.5		ns
t <sub>W</sub>	Pulse duration	SRCLR low	5V ± 0.5V	5		5.5		ns

## 5.7 Switching Characteristics

over operating free-air temperature range(unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V <sub>CC</sub>	T <sub>A</sub> = 25°C			-40°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
F <sub>MAX</sub>	-	-	C <sub>L</sub> = 15pF	5V ± 0.5V	135	175		115			MHz
t <sub>PZL</sub>	$\overline{OE}$	Q	C <sub>L</sub> = 15pF	5V ± 0.5V		5.4	8.6			12	ns
t <sub>PZH</sub>	$\overline{OE}$	Q	C <sub>L</sub> = 15pF	5V ± 0.5V		4.3	8.6			12	ns
t <sub>PLZ</sub>	$\overline{OE}$	Q	C <sub>L</sub> = 15pF	5V ± 0.5V		3.8	8	1		10.5	ns
t <sub>PHZ</sub>	$\overline{OE}$	Q	C <sub>L</sub> = 15pF	5V ± 0.5V		3.8	8	1		10.5	ns
t <sub>PLH</sub>	RCLK	QA-QH	C <sub>L</sub> = 15pF	5V ± 0.5V		4.3	7.4	1		9.5	ns
t <sub>PHL</sub>	RCLK	QA-QH	C <sub>L</sub> = 15pF	5V ± 0.5V		4.3	7.4	1		9.5	ns
t <sub>PLH</sub>	SRCLK	QH'	C <sub>L</sub> = 15pF	5V ± 0.5V		4.5	8.2	1		10.4	ns
t <sub>PHL</sub>	SRCLK	QH'	C <sub>L</sub> = 15pF	5V ± 0.5V		4.5	8.2	1		10.4	ns
t <sub>PHL</sub>	SRCLR	QH'	C <sub>L</sub> = 15pF	5V ± 0.5V		4.5	8	1		10.1	ns
F <sub>MAX</sub>	-	-	C <sub>L</sub> = 50pF	5V ± 0.5V	120	140		95			MHz
t <sub>PZL</sub>	$\overline{OE}$	Q	C <sub>L</sub> = 50pF	5V ± 0.5V		6.8	10.6			14.4	ns
t <sub>PZH</sub>	$\overline{OE}$	Q	C <sub>L</sub> = 50pF	5V ± 0.5V		5.7	10.6			14.4	ns
t <sub>PLZ</sub>	$\overline{OE}$	Q	C <sub>L</sub> = 50pF	5V ± 0.5V		3.4	10.3			13.2	ns
t <sub>PHZ</sub>	$\overline{OE}$	Q	C <sub>L</sub> = 50pF	5V ± 0.5V		3.5	10.3			13.2	ns
t <sub>PLH</sub>	RCLK	QA-QH	C <sub>L</sub> = 50pF	5V ± 0.5V		5.6	9.4	1		11.5	ns
t <sub>PHL</sub>	RCLK	QA-QH	C <sub>L</sub> = 50pF	5V ± 0.5V		5.6	9.4	1		11.5	ns
t <sub>PLH</sub>	SRCLK	QH'	C <sub>L</sub> = 50pF	5V ± 0.5V		6.4	10.2	1		12.4	ns
t <sub>PHL</sub>	SRCLK	QH'	C <sub>L</sub> = 50pF	5V ± 0.5V		6.4	10.2	1		12.4	ns
t <sub>PHL</sub>	SRCLR	QH'	C <sub>L</sub> = 50pF	5V ± 0.5V		6.4	10	1		12.1	ns

## 5.8 Noise Characteristics

V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>		0.2	0.8	V
V <sub>OL(V)</sub>	Quiet output, minimum dynamic V <sub>OL</sub>	-0.9	-0.2		V
V <sub>OH(V)</sub>	Quiet output, minimum dynamic V <sub>OH</sub>	4.4	4.7		V
V <sub>IH(D)</sub>	High-level dynamic input voltage	2			V
V <sub>IL(D)</sub>	Low-level dynamic input voltage			0.8	V

## 5.9 Typical Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

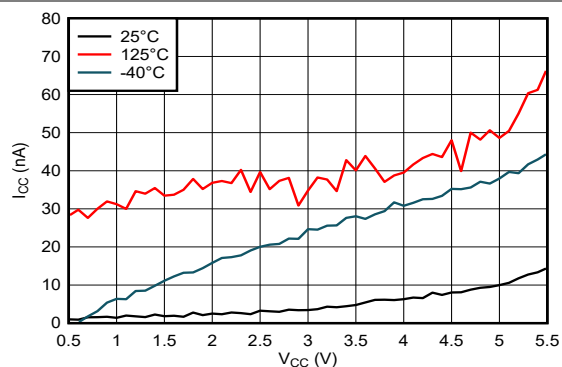


Figure 5-1. Supply Current Across Supply Voltage

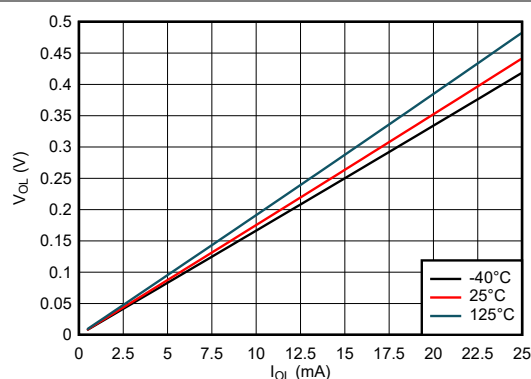
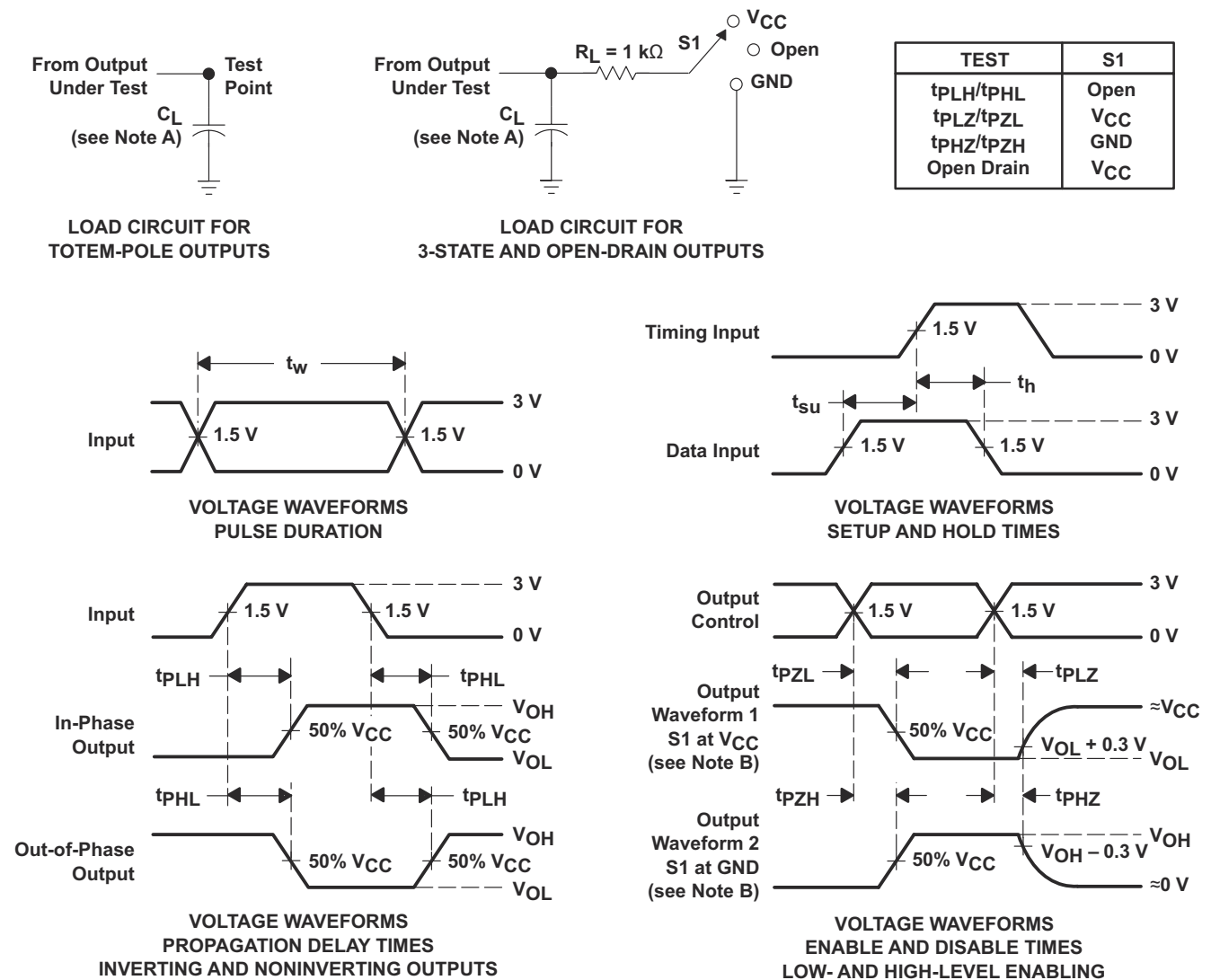


Figure 5-2. Output Voltage vs Current in LOW State; 5V Supply

## 6 Parameter Measurement Information



- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

**Figure 6-1. Load Circuit and Voltage Waveforms**

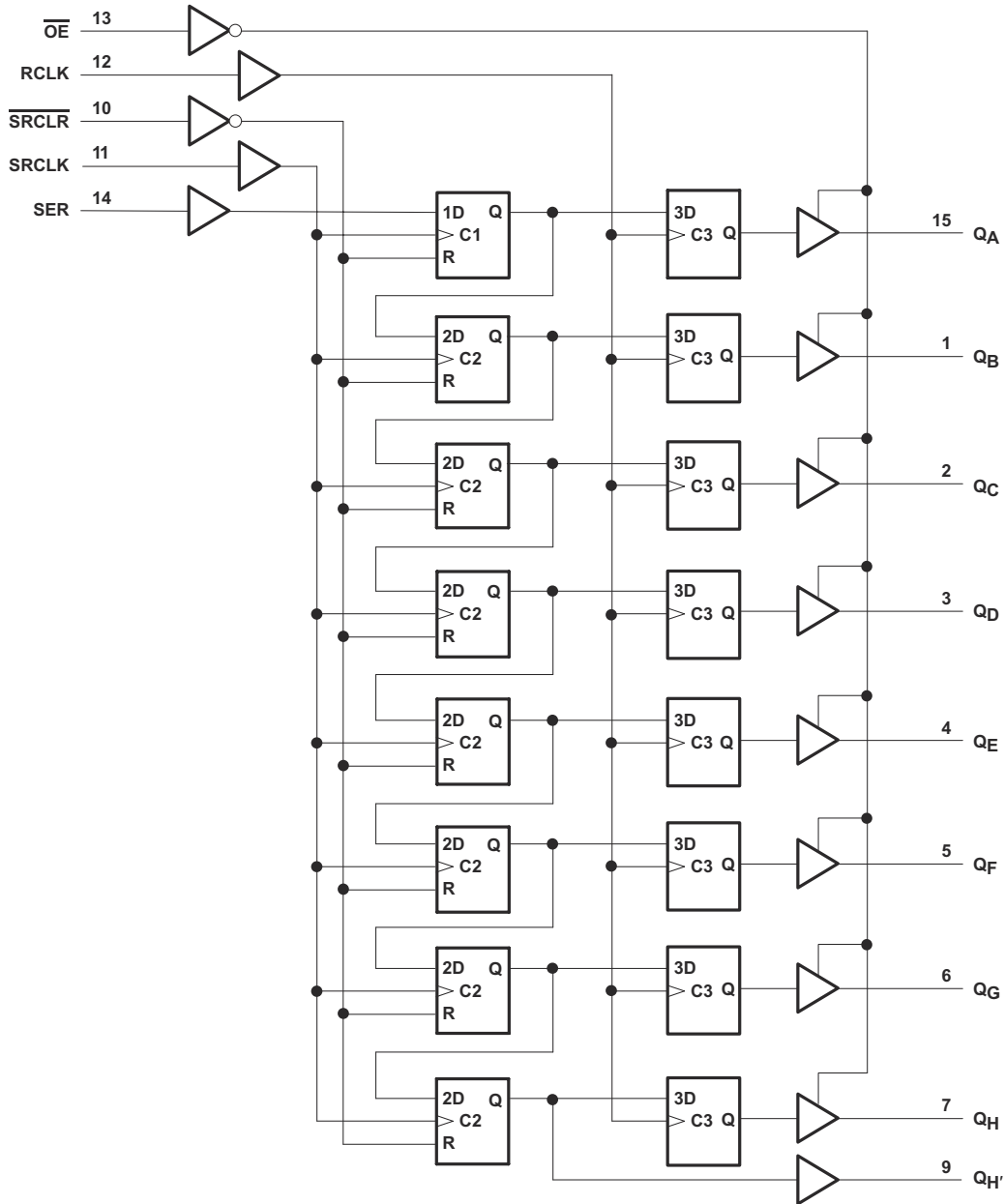


## 7 Detailed Description

### 7.1 Overview

The SNx4AHCT595 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for the shift and storage registers. The shift register has a direct overriding clear ( $\overline{\text{SRCLR}}$ ) input, serial (SER) input, and serial outputs for cascading. When the output-enable ( $\overline{\text{OE}}$ ) input is high, the outputs are in the high-impedance state. Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, then the shift register always is one clock pulse ahead of the storage register.

### 7.2 Functional Block Diagram



Pin numbers shown are for the PW and BQB packages.

### 7.3 Feature Description

## 7.4 Device Functional Modes

**Table 7-1. Function Table**

INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	$\overline{OE}$	
X	X	X	X	H	Outputs $Q_A - Q_H$ are disabled.
X	X	X	X	L	Outputs $Q_A - Q_H$ are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored in the storage register.

## 8 Application and Implementation

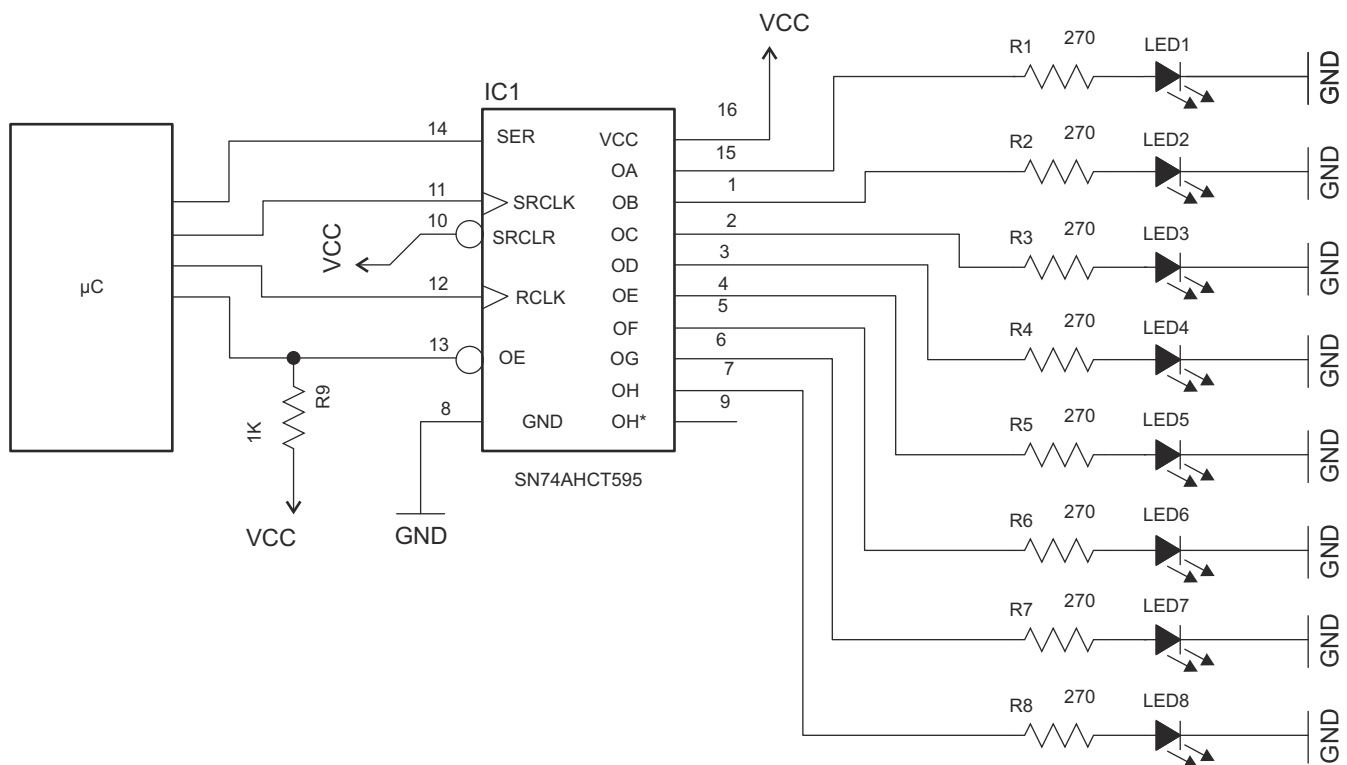
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The SNx4AHCT595 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8V  $V_{IL}$  and 2V  $V_{IH}$ . This feature makes it an excellent choice for translating up from 3.3V to 5V. Figure 8-1 shows this type of translation.

### 8.2 Typical Application



**Figure 8-1. Specific Application Schematic**

#### 8.2.1 Design Requirements

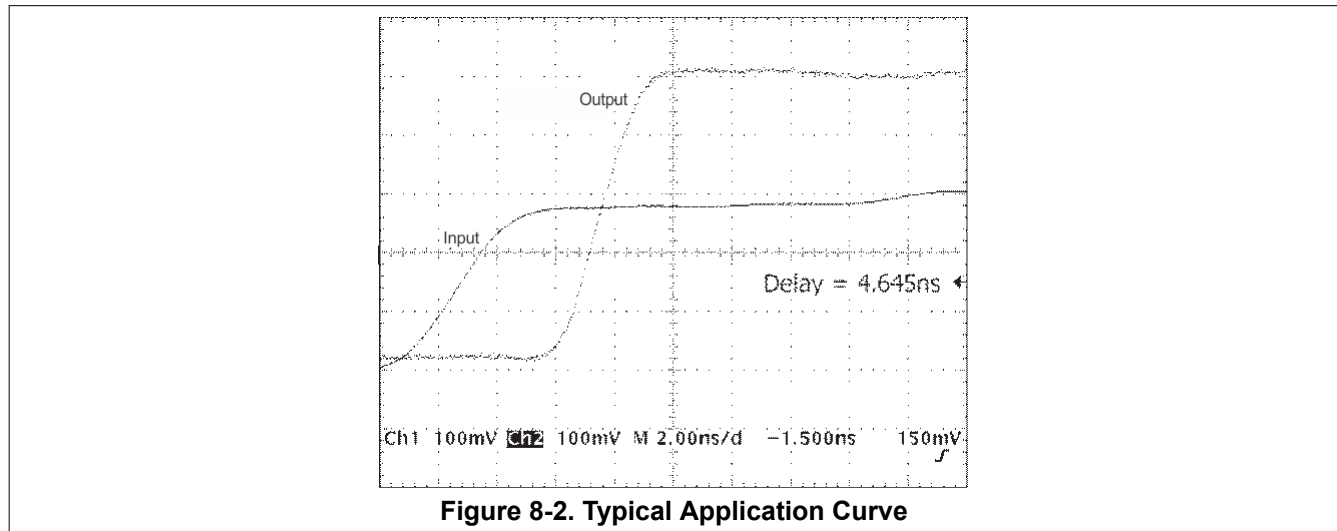
This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 8.2.2 Detailed Design Procedure

- Recommended input conditions
  - Specified high and low levels. See ( $V_{IH}$  and  $V_{IL}$ ) in the [Recommended Operating Conditions](#) table.
  - Specified high and low levels. See ( $V_{IH}$  and  $V_{IL}$ ) in the [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5V at any valid  $V_{CC}$

- Recommend output conditions
  - Load currents should not exceed 25mA per output and 50mA total for the part
  - Outputs should not be pulled above  $V_{CC}$

### 8.2.3 Application Curves



## 8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 $\mu$ F is recommended; if there are multiple  $V_{CC}$  pins, then 0.01 $\mu$ F or 0.022 $\mu$ F is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 $\mu$ F and a 1 $\mu$ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

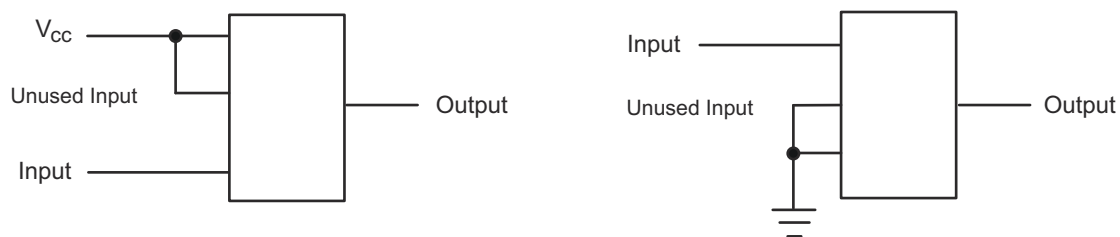
## 8.4 Layout

### 8.4.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 8-3](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

### 8.4.2 Layout Example



**Figure 8-3. Layout Diagram**

## 9 Device and Documentation Support

### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision P (April 2024) to Revision Q (August 2024)	Page
• Updated thermal values for D package from RθJA = 80.2 to 93.8, RθJC(top) = 39.1 to 54.7, RθJB = 27.7 to 50.9, ΨJT = 9.9 to 20.8, ΨJB = 37.4 to 50.7, RθJC(bot) = N/A, all values in °C/W .....	5

Changes from Revision O (March 2024) to Revision P (April 2024)	Page
• Updated thermal values for PW package from RθJA = 105.7 to 135.9, RθJC(top) = 40.4 to 70.3, RθJB = 50.7 to 81.3, ΨJT = 3.7 to 22.5, ΨJB = 50.1 to 80.8, all values in °C/W.....	5

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74AHCT595BQBR</a>	Active	Production	WQFN (BQB)   16	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHT595
SN74AHCT595BQBR.A	Active	Production	WQFN (BQB)   16	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHT595
<a href="#">SN74AHCT595D</a>	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	-40 to 125	AHCT595
<a href="#">SN74AHCT595DBR</a>	Active	Production	SSOP (DB)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB595
SN74AHCT595DBR.A	Active	Production	SSOP (DB)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB595
SN74AHCT595DBR.B	Active	Production	SSOP (DB)   16	2000   LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB595
<a href="#">SN74AHCT595DR</a>	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT595
SN74AHCT595DR.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT595
<a href="#">SN74AHCT595N</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHCT595N
SN74AHCT595N.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHCT595N
SN74AHCT595NE4	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHCT595N
<a href="#">SN74AHCT595PW</a>	Obsolete	Production	TSSOP (PW)   16	-	-	Call TI	Call TI	-40 to 125	HB595
<a href="#">SN74AHCT595PWR</a>	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	HB595
SN74AHCT595PWR.A	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB595
SN74AHCT595PWR.B	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB595
<a href="#">SN74AHCT595PWRG3</a>	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	HB595
SN74AHCT595PWRG3.A	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	HB595

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74AHCT595 :**

- Automotive : [SN74AHCT595-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT595BQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
SN74AHCT595DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHCT595DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHCT595DR	SOIC	D	16	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AHCT595DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHCT595PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT595PWRG3	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT595BQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
SN74AHCT595DBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN74AHCT595DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74AHCT595DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74AHCT595DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74AHCT595PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74AHCT595PWG3	TSSOP	PW	16	2000	364.0	364.0	27.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AHCT595N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHCT595N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHCT595N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHCT595N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHCT595NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHCT595NE4	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

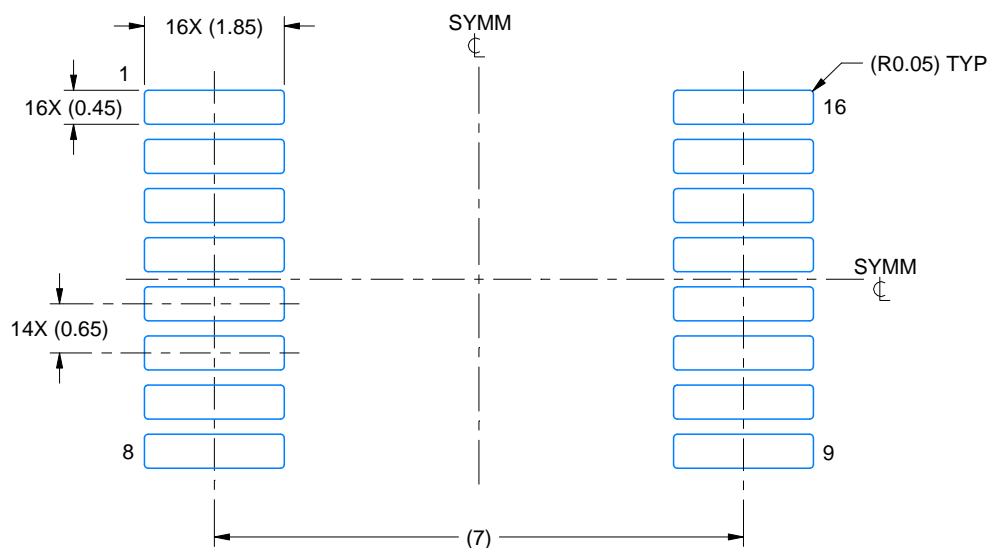


# EXAMPLE BOARD LAYOUT

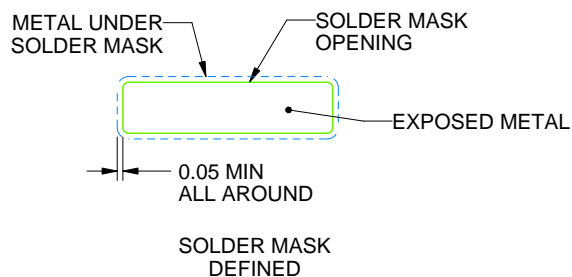
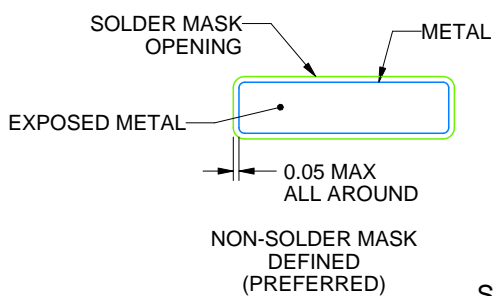
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**BQB 16**

**WQFN - 0.8 mm max height**

2.5 x 3.5, 0.5 mm pitch

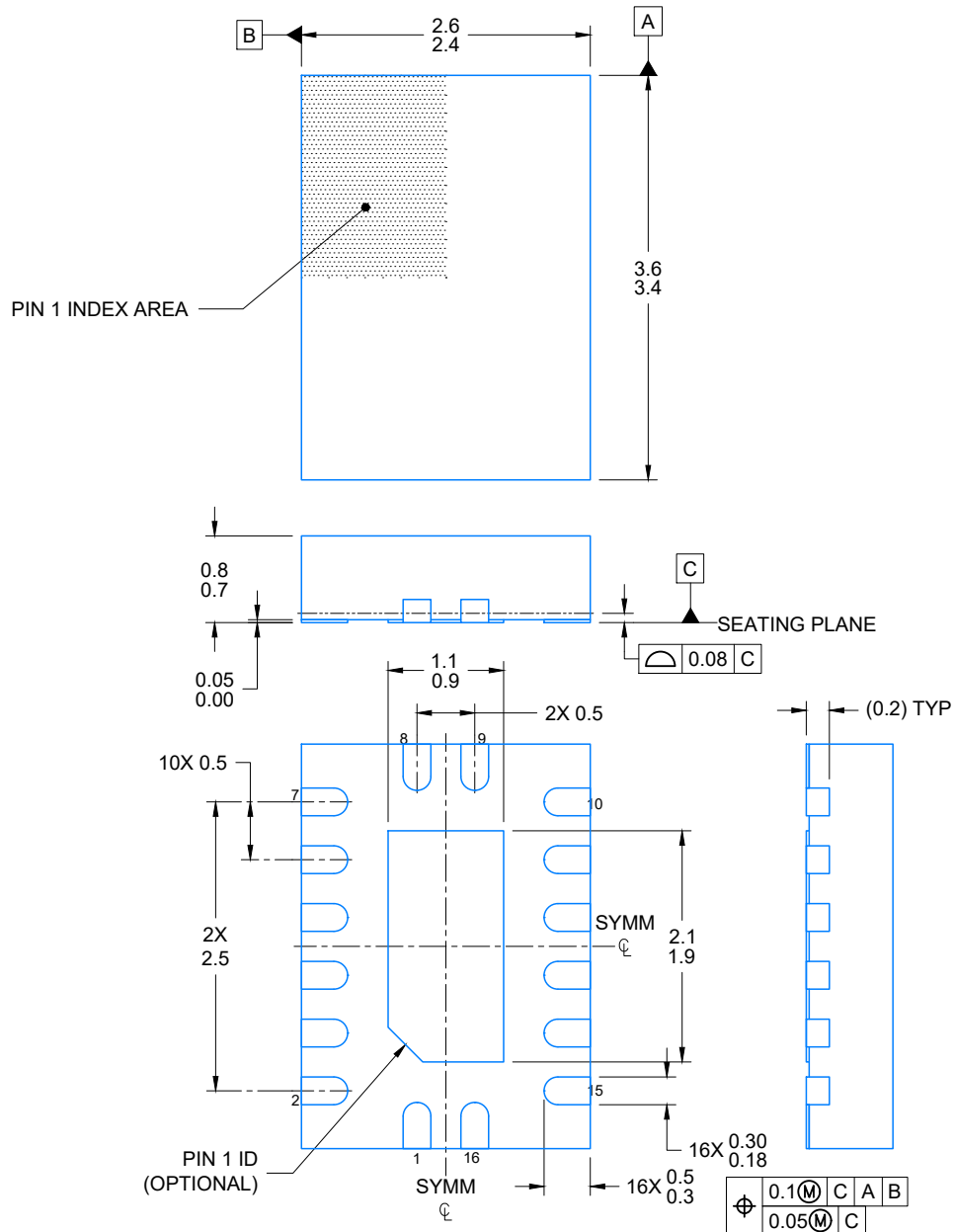
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4226161/A

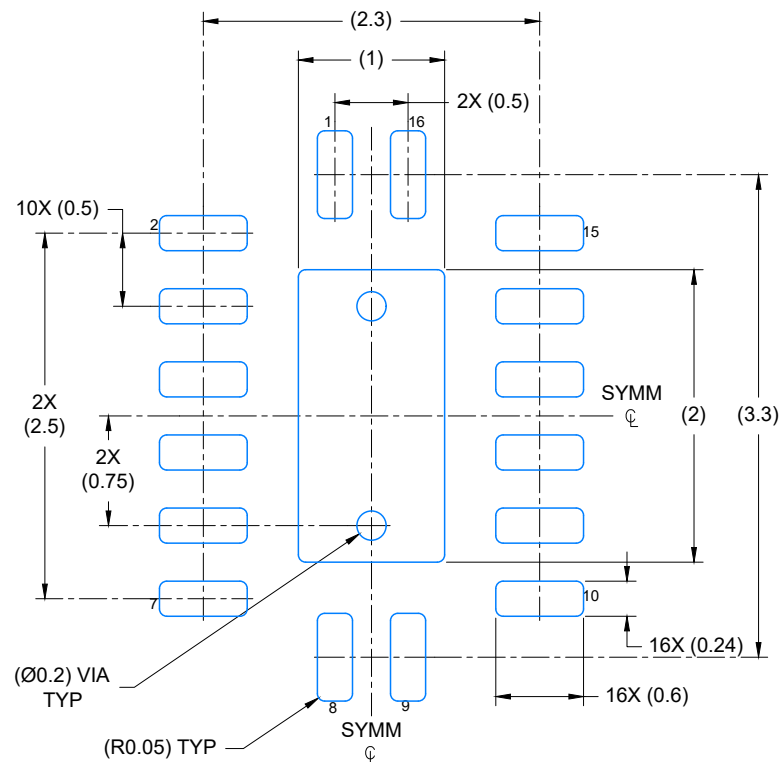




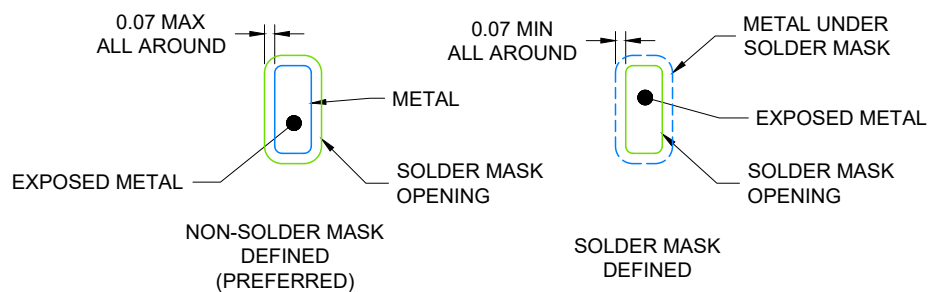
4224640/A 11/2018

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



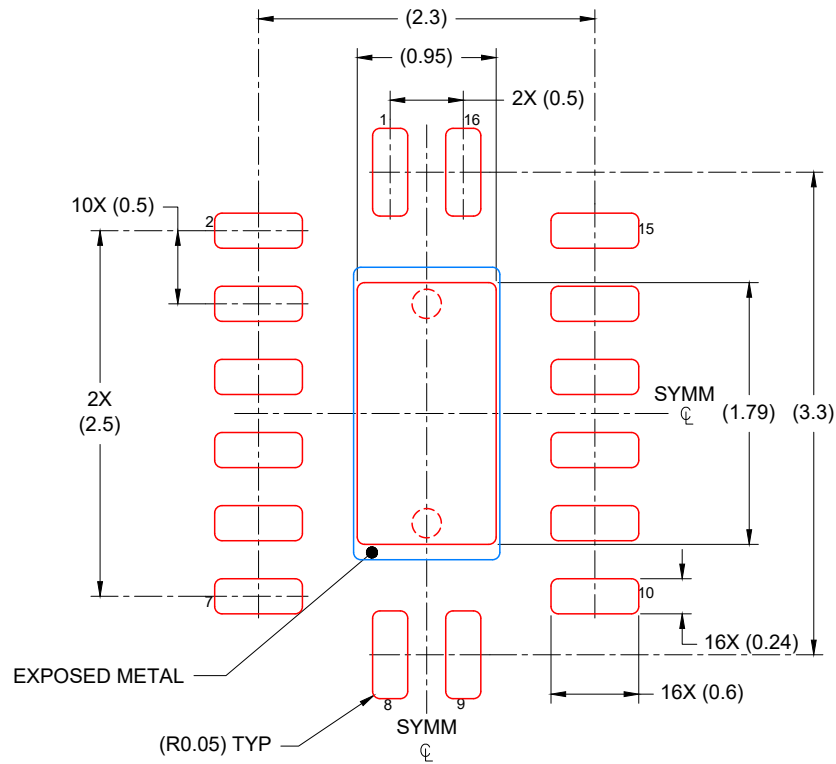
LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224640/A 11/2018

## NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 85% PRINTED COVERAGE BY AREA  
 SCALE: 20X

4224640/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4220204/B 12/2023

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

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