

# ADM8511/X

USB/Fast Ethernet/HomePNA Controller

Communications



Never stop thinking.

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## USB/Fast Ethernet/HomePNA Controller

**Revision History: 2005-11-30, Rev. 2.03**

### Previous Version:

| Page/Date          | Subjects (major changes since last revision)                                |
|--------------------|-----------------------------------------------------------------------------|
| 2000-06            | Rev. 0.1: Draft product spec for review                                     |
| 2000-09            | Rev. 1.0: Rearrange                                                         |
| 2000-10            | Rev. 2.0: Add appendix                                                      |
| Page62/<br>2000-12 | Rev. 2.01: Appendix 5/item 7/item b/item iii/ TXER change to RXER           |
| 2000-12            | Rev. 2.02: Add max. power consumption P.1 I <sup>2</sup> C change to serial |
| 2005-09-12         | Rev. 2.03: when changed to the new Infineon format                          |
| 2005-11-30         | Minor change. Included Green package information                            |
|                    |                                                                             |
|                    |                                                                             |

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## 1 General Description

The ADM8511/X, USB based chip set, provides desktop, notebook and computer peripheral with greater connectivity to ethernet and home network. In the meantime, the ADM8511/X also combines a low power and small package design which is ideal for power and space constrained by the environment. Then, it can reduce the external component BOM cost to a minimum. The ADM8511X is the environmentally friendly “green” package version.

The ADM8511/X device combines a on-chip USB command&EP decoder used for USB interface through SIE (Series Interface Engine), FIFO controller with 24 K SRAM, 64 byte and 2 K byte buffers, 10/100 Mbit/s ethernet physical layer (PHY) and 1M / 10M HomePNA interface 1M8 / 10M8. The 10M HomePNA interface is MII which is the same as the ethernet MAC interface. The ADM8511/X is fully compliant with the IEEE 802.3 u and HomePNA (Home Phoneline Network Alliance) specification revision 1.0.

The ADM8511/X is capable of providing an easy, universal connectivity to computer peripherals with USB. The transfer rate of USB interface is 12 Mbit/s belonging to a high speed USB device. The ADM8511/X supports all USB commands, 4 endpoints and suspend/resume function.

The ADM8511/X's LAN PHY supports 100 Base TX (100 Mbit/s mode) and 10 Base T (10 Mbit/s mode) full-duplex operations. It uses the auto-negotiation function to optimize the network traffic and the built-in 24M SRAM for receiving buffer, especially for 100 Mbit/s. Through FIFO controller, data cannot communicate fluently between buffers and external device. To obtain the better signal quality, the PHY provides wave-shaper, filter and adaptive equalizer to reach. By using diagnostic mechanism (loop-back mode), the data correctness will be increased. The Lan PHY supports external transmit/receive transformer turn ratio 1:1. The ADM8511/X chip set can be programmed MAC analysis and it provides MII interface for external PHY, such as 10M8 interface for 1 Mbit/s HomePNA. In the system application, it is essential that the EEPROM loads device ID and vendor ID automatically. So for ADM8511/X, serial interface is applied for EEPROM communication including read/write function. Furthermore, different system status are reported by some LED pins including transfer speed LEDSP (100 Mbit/s or 10 Mbit/s), Link status (LEDL) on network and transfer type LEDFD/COL) full- duplex or half-duplex or collision on network.

ADM8511/X is ideally suited for USB adapter and intelligent networked peripheral design. By fiber media, ADM8511/X can associate with fiber transceiver & PHY through MII interface to network in fiber network. In HomePAN application, ADM8511/X can provide 1M8 interface and 10M8 (MII interface) associated with external 1M&10M Home PHY for 1 Mbit/s & 10 Mbit/s network. ADM8511/X can't apply only in LAN (Local Area Network) but also in WAN (Wide Area Network), such as xDSL, Cable Modem, and router, etc. In IA (Information Appliance) application, Set-Top box is an example of ADM8511/X application. ADM8511/X also provides serial interface for EEPROM storing default values, e.g. vendor ID, Product ID, etc.(EEPROM Access Program). Specially, ADM8511/X can be tested by test program (MFG) in the less time for mass productions of system board level. This chip provides low power 0.35  $\mu$ m, 3.3 V/5 V I/Otolerance, and 100 pin LQFP package

In software, ADM8511/X provides a fully software support, NDIS 5 driver, Linux driver, EEPROM burn-in program and MFG program. The NDIS 5 and Linux drivers are windows netware drivers. EEPROM burn-in program is convenient for customers to implement. The MFG program is a powerful tool in mass – production.

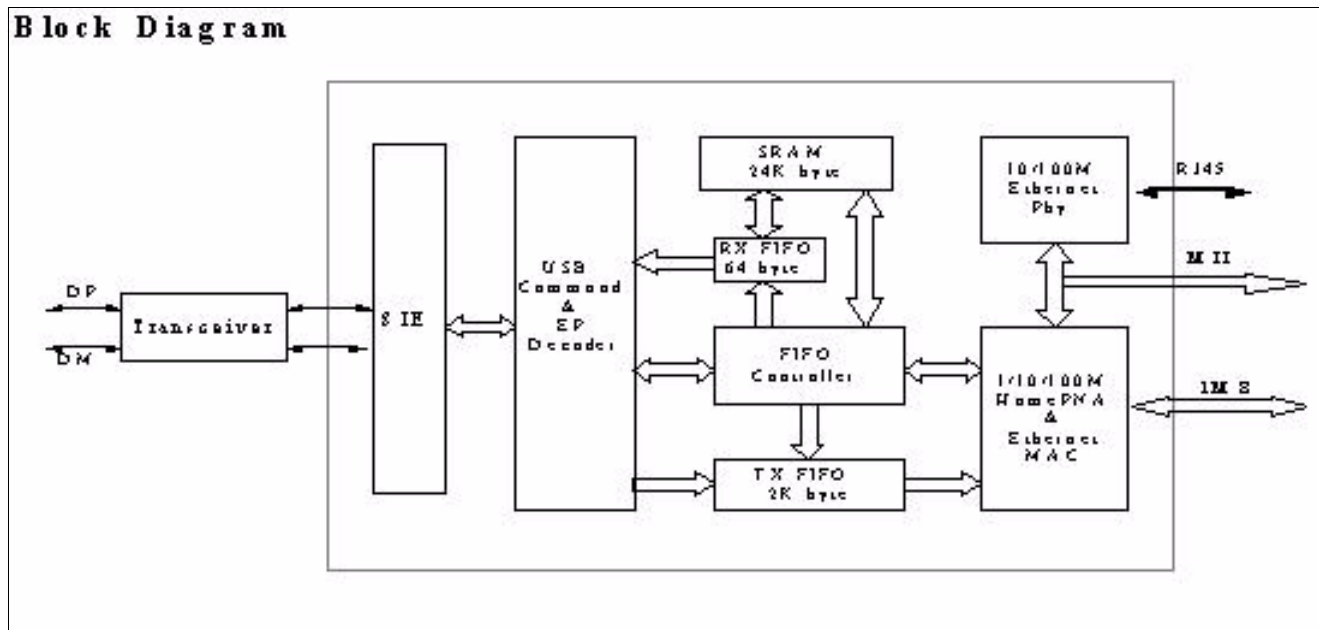


Figure 1 Block Diagram

## 1.1 Package Information

| Product Name | Product Type     | Package      | Ordering Number |
|--------------|------------------|--------------|-----------------|
| ADM8511/X    | ADM8511/X-CC-T-1 | P-LQFP-100-1 | Q67801H 26A101  |

## 1.2 Features

### 1.2.1 Industry Standard

- IEEE802.3 u 100BASE-TX and IEEE802.3 10BASE-T compliant
- Supports for IEEE 802.3x flow control
- IEEE802.3 u Auto-Negotiation support for 10BASE-T and 100BASE-TX
- USB specification 1.0 and 1.1 compliant

### 1.2.2 USB I/F

- Full-Speed USB Device
- Supports 1 USB configuration and 1 interface
- Supports all USB standard commands
- Supports two vendor specific commands
- Supports USB Suspend/Resume detection logic
- Supports 4 endpoints: 1 control endpoint with maximum 8-byte packet, 1 bulk IN endpoint with maximum 64-byte packet, 1 bulk OUT endpoint with maximum 64-byte packet and 1 interrupt IN endpoint with maximum 8-byte packet

### 1.2.3 MAC/Phy

- Integrates the whole physical layer functions of 100BASE-TX and 10BASE-T by using phy address 1
- Be programmed to isolate the internal PHY, the I/F to external PHY could be either IEEE 802.3 MII (10M8 for HomePNA 2.0). Supports configurable threshold for transmitting PAUSE frame
- Supports wakeup frame, link status change and magic packet wake-up
- Provides full-duplex operation on both 100 Mbit/s and 10 Mbit/s Ethernet modes
- Provides Auto-negotiation (NWAY) function of full/half duplex operation for both 10/100 Mbit/s
- Provides transmit wave-shaper, receive filters, and adaptive equalizer
- Provides MLT-3 transceiver with DC restoration for Base-Line Wander compensation
- Provides MAC and Transceiver loop-back modes for diagnostic
- Supports external transmit transformer with turn ratio 1:1
- Supports external receive transformer with turn ratio 1:1

### 1.2.4 EEPROM I/F

- Provides serial interface for read/write 93C46 EEPROM
- Automatically load device ID, vendor ID from EEPROM after power-on reset

### 1.2.5 FIFO

- Supports internal 2 Kbytes SRAM for transmission
- Supports external 32 Kbytes SRAM or internal 24 Kbytes synchronous SRAM for receiving.
- Supports "receive 32 packets" or "receive 16 packets" queue in the receive buffer

### 1.2.6 LED Display

- Provides LED display
- LEDSP: Speed - 100 Mbit/s(on) or 10 Mbit/s(off)
- LEDL: Link (keeps on when link ok) or Active (will be blinking with 10 Hz)
- LEDFD/COL: FD (keeps on when in Full duplex mode) or Collision (will be blinking with 20 Hz when colliding)

### 1.2.7 Miscellaneous

- Supports 6 GPIO pins
- Provides 100-pin LQFP package
- 3.3 V power supply with 5 V/3.3 V I/O tolerance

### 1.2.8 LAN Driver Support

- Windows Networks: NDIS 5.0
- Linux

### 1.2.9 Utility

- EEPROM burn-in program

- MFG testing program

## 2 Interface Description

### 2.1 Pin Diagram

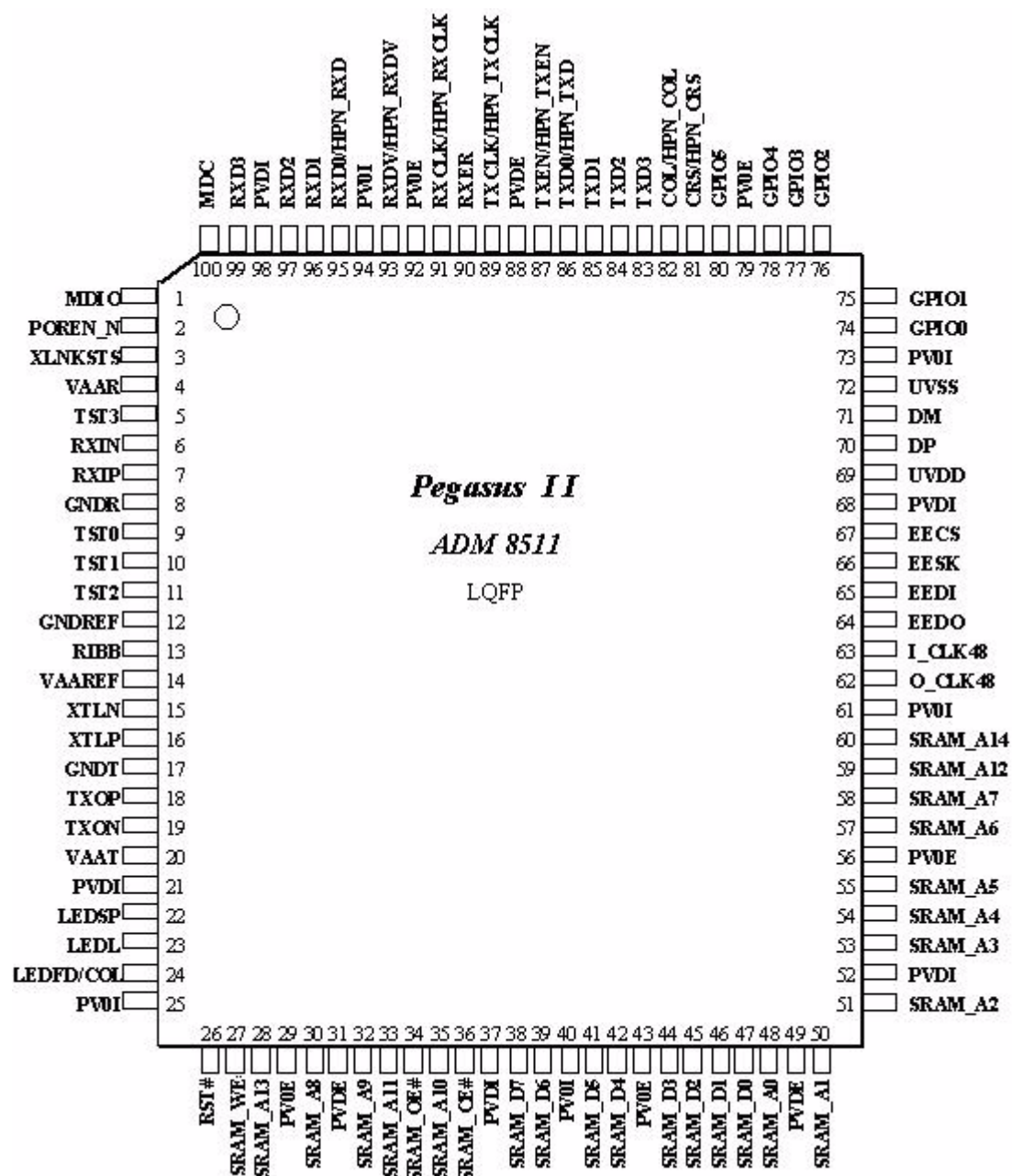


Figure 2 Pin Diagram

## 2.2 Pin Description

**Table 1 Abbreviations for Pin Type**

| Abbreviations | Description                                 |
|---------------|---------------------------------------------|
| I             | Standard input-only pin. Digital levels.    |
| O             | Output. Digital levels.                     |
| I/O           | I/O is a bidirectional input/output signal. |
| AI            | Input. Analog levels.                       |
| AO            | Output. Analog levels.                      |
| AI/O          | Input or Output. Analog levels.             |
| PWR           | Power                                       |
| GND           | Ground                                      |
| MCL           | Must be connected to Low (JEDEC Standard)   |
| MCH           | Must be connected to High (JEDEC Standard)  |
| NU            | Not Usable (JEDEC Standard)                 |
| NC            | Not Connected (JEDEC Standard)              |

**Table 2 Abbreviations for Buffer Type**

| Abbreviations | Description                                                                                                                                                                                                                                                                        |
|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Z             | High impedance                                                                                                                                                                                                                                                                     |
| PU1           | Pull up, 10 k $\Omega$                                                                                                                                                                                                                                                             |
| PD1           | Pull down, 10 k $\Omega$                                                                                                                                                                                                                                                           |
| PD2           | Pull down, 20 k $\Omega$                                                                                                                                                                                                                                                           |
| TS            | Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.                                                                                                                                                                                 |
| OD            | Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource. |
| OC            | Open Collector                                                                                                                                                                                                                                                                     |
| PP            | Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).                                                                                                                                                |
| OD/PP         | Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute.                                                                                                                                  |
| ST            | Schmitt-Trigger characteristics                                                                                                                                                                                                                                                    |
| TTL           | TTL characteristics                                                                                                                                                                                                                                                                |

## 2.2.1 Host Interface

**Table 3 Host Interface**

| Pin or Ball No. | Name    | Pin Type | Buffer Type | Function                                             |
|-----------------|---------|----------|-------------|------------------------------------------------------|
| 63              | I_CLK48 | I        |             | <b>48 MHz Clock Input from Crystal or Oscillator</b> |
| 62              | O_CLK48 | O        |             | <b>Output for Crystal</b>                            |
| 26              | RST#    | I        |             | <b>External Hardware Reset Input</b>                 |
| 71              | DM      | I/O      |             | <b>USB Data Minus Pin</b>                            |
| 70              | DP      | I/O      |             | <b>USB Data Plus Pin</b>                             |

## 2.2.2 MII Interface

Program ADM8511/X as MAC-only mode, set 81<sub>H</sub>[4:2]=001<sub>B</sub> and 01<sub>H</sub> bit 2 = 0

**Table 4 MII Interface**

| Pin or Ball No. | Name  | Pin Type | Buffer Type | Function                                                                                                                                                                                                                                 |
|-----------------|-------|----------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 82              | COL   | I        |             | <b>Collision Detected</b><br>This signal is asserted high asynchronously by the external physical unit upon detection of a collision on the medium. It will remain asserted as long as the collision condition persists.                 |
| 81              | CRS   | I        |             | <b>Carrier Sense</b><br>This signal is asserted high asynchronously by the external physical unit upon detection of a non-idle medium.                                                                                                   |
| 100             | MDC   | O        |             | <b>Management Data Clock</b><br>Clock signal with a maximum rate of 2.5 MHz used to transfer management data for the external PMD on the MDIO pin.                                                                                       |
| 1               | MDIO  | I/O      |             | <b>Management Data I/O</b><br>Bi-directional signal used to transfer management information for the external PMD. Requires external 1.5 kΩ pull-up resistor.                                                                             |
| 91              | RXCLK | I        |             | <b>Receive Clock</b><br>A continuous clock that is recovered from the incoming data. During 100 Mbit/s operation RXCLK is 25 MHz, during 10 Mbit/s this is 2.5 MHz and during 1 Mbit/s operation this is 0.25 MHz.                       |
| 95              | RXD3  | I        |             | <b>Receive Data</b><br>This is a group of 4 data signals aligned on nibble boundary which are driven synchronous to the RXCLK by the external physical unit. RXD[3] is the most significant bit and RXD[0] is the least significant bit. |
| 96              | RXD2  |          |             |                                                                                                                                                                                                                                          |
| 97              | RXD1  |          |             |                                                                                                                                                                                                                                          |
| 99              | RXD0  |          |             |                                                                                                                                                                                                                                          |

## Interface Description

Table 4 MII Interface (cont'd)

| Pin or Ball No. | Name    | Pin Type | Buffer Type | Function                                                                                                                                                                                                                                                                                                                                                          |
|-----------------|---------|----------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 93              | RXDV    | I        |             | <b>Receive Data Valid</b><br>This indicates that the external physical unit is presenting recovered and decoded nibbles on the RXD[3:0] and that RXCLK is synchronous to the recovered data.                                                                                                                                                                      |
| 90              | RXER    | I        |             | <b>Receive Error</b><br>This signal is asserted high synchronously by the external physical unit whenever it detects a media error and RXDV is asserted.<br>If not used, it should be grounded, e.g. isolate internal phy and use external phy. However, if the external phy has RXER pin, the RXER of ADM8511/X should connect to this RXER of the external phy. |
| 89              | TXCLK   | I        |             | <b>Transmit Clock</b><br>A continuous clock sourced in the physical layer. During 100 Mbit/s operation this is 25 MHz $\pm$ 100 ppm. During 10 Mbit/s operation this clock is 2.5 MHz $\pm$ 100 ppm. During 1 Mbit/s operation this clock is 0.25 MHz $\pm$ 100 ppm.                                                                                              |
| 83              | TXD3    | O        |             | <b>Transmit Data</b><br>This is a group of 4 data signals which are driven synchronously to the TXCLK for transmission to the external physical unit. TXD[3] is the most significant bit and TXD[0] is the least significant bit.                                                                                                                                 |
| 84              | TXD2    |          |             |                                                                                                                                                                                                                                                                                                                                                                   |
| 85              | TXD1    |          |             |                                                                                                                                                                                                                                                                                                                                                                   |
| 86              | TXD0    |          |             |                                                                                                                                                                                                                                                                                                                                                                   |
| 87              | TXEN    | O        |             | <b>Transmit Enable</b><br>This signal is synchronous to TXCLK and provides precise framing for data carried on TXD[3:0]. It is asserted when TX[3:0] contains valid data to be transmitted. Requires external pull-down resistor 4.7 k $\Omega$ if external phy is used                                                                                           |
| 3               | XLNKSTS | I        |             | <b>Link Status Indication</b><br>External PHY reports link status information to system and level change trigger. Pull-down to low if external phy is used.                                                                                                                                                                                                       |

### 2.2.3 1M8 Interface

Program ADM8511/X as MAC-only mode, set 81<sub>H</sub>[4:2]=001<sub>B</sub> and 01<sub>H</sub> bit 2 = 1

Table 5 1M8 Interface

| Pin or Ball No. | Name    | Pin Type | Buffer Type | Function                                                                                               |
|-----------------|---------|----------|-------------|--------------------------------------------------------------------------------------------------------|
| 82              | HPN_COL | I        |             | <b>Collision</b><br>Indicates a collision was detected by the 1M8 PHY on the 1M8 wiring network.       |
| 81              | HPN_CRS | I        |             | <b>Carrier Sense</b><br>Indicates the 1M8 PHY is receiving a valid 1M8 signal from the wiring network. |

## Interface Description

Table 5 1M8 Interface (cont'd)

| Pin or Ball No. | Name      | Pin Type | Buffer Type | Function                                                                                                                                                                                        |
|-----------------|-----------|----------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 91              | HPN_RXCLK | I        |             | <b>Receive Clock</b><br>Clock for RX_D.                                                                                                                                                         |
| 95              | HPN_RXD   | I        |             | <b>Receive Data</b><br>Data to the MAC is synchronously clocked by HPN_RXCLK.                                                                                                                   |
| 93              | HPN_RXDV  | I        |             | <b>Receive Data Valid</b><br>This indicates that the external physical unit is presenting recovered and decoded nibbles on the HPN_RXD and that HPN_RXCLK is synchronous to the recovered data. |
| 89              | HPN_TXCLK | I        |             | <b>Transmit Clock</b><br>Clock for HPN_TXD.                                                                                                                                                     |
| 86              | HPN_TXD   | O        |             | <b>Transmit Data</b><br>Data to the PHY is synchronously clocked by HPN_TXCLK.                                                                                                                  |
| 87              | HPN_TXEN  | O        |             | <b>Transmit Enable</b><br>Transmits enable request from the MAC to begin sending data to the PHY.                                                                                               |

## 2.2.4 Physical Interface

Table 6 Physical Interface

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function                                                                                                                                         |
|-----------------|------|----------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 16              | XTLP | I        |             | <b>Crystal inputs</b><br>To be connected to a 25 MHz crystal.                                                                                    |
| 15              | XTLN |          |             |                                                                                                                                                  |
| 6               | RXIN | I        |             | The differential receives inputs of 100Base-TX or 10Base-T, these pins directly input from Magnetic.                                             |
| 7               | RXIP |          |             |                                                                                                                                                  |
| 18              | TXOP | O        |             | The differential Transmit outputs of 100Base-TX or 10Base-T, these pins directly output to Magnetic.                                             |
| 19              | TXON |          |             |                                                                                                                                                  |
| 13              | RIBB | I        |             | <b>Reference Bias Resistor</b><br>To be tied to an external 10.0K (1%) resistor which should be connected to the analog ground at the other end. |
| 9               | TST0 | I        |             | <b>Test pin</b>                                                                                                                                  |
| 10              | TST1 |          |             |                                                                                                                                                  |
| 11              | TST2 |          |             |                                                                                                                                                  |
| 5               | TST3 |          |             |                                                                                                                                                  |

## 2.2.5 LED Display

**Table 7 LED Display**

| Pin or Ball No. | Name      | Pin Type | Buffer Type | Function                                                                                                                             |
|-----------------|-----------|----------|-------------|--------------------------------------------------------------------------------------------------------------------------------------|
| 22              | LEDSP     | O        |             | <b>LED Display for 100 Mbit/s or 10 Mbit/s Speed</b><br>Active low indicates 100Base-TX, active high indicates 10 BaseT.             |
| 23              | LEDL      | O        |             | <b>LED Display for Link and Activity Status</b><br>Active low when link is established.                                              |
| 24              | LEDFD/COL | O        |             | <b>LED Display for Full Duplex or Collision Status</b><br>Active low indicates full duplex, high indicates collision in half duplex. |

## 2.2.6 SRAM Interface

**Table 8 SRAM Interface**

| Pin or Ball No. | Name     | Pin Type | Buffer Type | Function                                            |
|-----------------|----------|----------|-------------|-----------------------------------------------------|
| 48              | SRAM_A14 | O        |             | <b>External SRAM Address Bus</b>                    |
| 50              | SRAM_A13 |          |             |                                                     |
| 51              | SRAM_A12 |          |             |                                                     |
| 53              | SRAM_A11 |          |             |                                                     |
| 54              | SRAM_A10 |          |             |                                                     |
| 55              | SRAM_A9  |          |             |                                                     |
| 57              | SRAM_A8  |          |             |                                                     |
| 58              | SRAM_A7  |          |             |                                                     |
| 30              | SRAM_A6  |          |             |                                                     |
| 32              | SRAM_A5  |          |             |                                                     |
| 35              | SRAM_A4  |          |             |                                                     |
| 33              | SRAM_A3  |          |             |                                                     |
| 59              | SRAM_A2  |          |             |                                                     |
| 28              | SRAM_A1  |          |             |                                                     |
| 60              | SRAM_A0  |          |             |                                                     |
| 47              | SRAM_D7  | I/O      | PD          | <b>External SRAM Data Bus</b><br>Internal pull down |
| 46              | SRAM_D6  |          |             |                                                     |
| 45              | SRAM_D5  |          |             |                                                     |
| 44              | SRAM_D4  |          |             |                                                     |
| 42              | SRAM_D3  |          |             |                                                     |
| 41              | SRAM_D2  |          |             |                                                     |
| 39              | SRAM_D1  |          |             |                                                     |
| 38              | SRAM_D0  |          |             |                                                     |

## Interface Description

Table 8 SRAM Interface (cont'd)

| Pin or Ball No. | Name     | Pin Type | Buffer Type | Function                           |
|-----------------|----------|----------|-------------|------------------------------------|
| 36              | SRAM_CE# | O        |             | <b>External SRAM Chip Enable</b>   |
| 34              | SRAM_OE# | O        |             | <b>External SRAM Output Enable</b> |
| 27              | SRAM_WE# | O        |             | <b>External SRAM Write Enable</b>  |

## 2.2.7 EEPROM Interface

Table 9 EEPROM Interface

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function                                                                                                                                                                |
|-----------------|------|----------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 67              | EECS | O        |             | <b>EEPROM Chip Select</b><br>This enables the EEPROM during loading of the Ethernet configuration data.                                                                 |
| 65              | EEDI | O        |             | <b>EEPROM Data In</b><br>The MAC will use this pin to serially write opcodes, addresses and data into the serial EEPROM.                                                |
| 64              | EEDO | I        |             | <b>EEPROM Data Out</b><br>The MAC will read the contents of the EEPROM serially through this pin.                                                                       |
| 66              | EESK | O        |             | <b>EEPROM Clock</b><br>After reset, the MAC if configured, will read the contents of the EEPROM using EESK, EEDO, and EEDI. This pin provides the clock for the EEPROM. |

## 2.2.8 Miscellaneous

Table 10 Miscellaneous

| Pin or Ball No. | Name    | Pin Type | Buffer Type | Function                                                                                                                                                                                                  |
|-----------------|---------|----------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 80              | GPIO5   | I/O      |             | These pins are used as general purpose Input/Output pins and offset 0A[1] = 0 in EEPROM.<br>Default is internal pull-low                                                                                  |
| 78              | GPIO4   |          |             |                                                                                                                                                                                                           |
| 77              | GPIO3   |          |             |                                                                                                                                                                                                           |
| 76              | GPIO2   |          |             |                                                                                                                                                                                                           |
| 75              | GPIO1   |          |             |                                                                                                                                                                                                           |
| 74              | GPIO0   |          |             |                                                                                                                                                                                                           |
| 2               | POREN_N | I        |             | <b>Internal Power On Reset Logic Enable</b><br>Default is enabled and internal pull - low.<br>When external hardware reset is used, this pin should be connected to $V_{cc}$ via 4.7 k $\Omega$ resistor. |

## 2.2.9 Power Pins

**Table 11 Power Pins**

| Pin or Ball No.    | Name   | Pin Type | Buffer Type | Function                               |
|--------------------|--------|----------|-------------|----------------------------------------|
| 21, 37, 52, 68, 98 | PVDI   | P        |             | 3.3 V Power Supply for Core            |
| 31, 49, 88         | PVDE   | P        |             | 3.3 V Power Supply for Pads            |
| 25, 40, 61, 73, 94 | PV0I   | P        |             | Ground for PVDI                        |
| 29, 43, 56, 79, 92 | PV0E   | P        |             | Ground for PVDE                        |
| 69                 | UVDD   | P        |             | 3.3 V Power Supply for USB Transceiver |
| 72                 | UVSS   | P        |             | Ground for UVDD                        |
| 4                  | VAAR   | P        | P           | Analog Power Pins, 3.3 V               |
| 14                 | VAAREF |          |             |                                        |
| 20                 | VAAT   |          |             |                                        |
| 8                  | GNDR   | P        |             | Analog Ground Pins                     |
| 12                 | GNDREF |          |             |                                        |
| 17                 | GNDT   |          |             |                                        |

## 3 Function Description

### 3.1 USB Interface

USB is a likely solution when you want to use a computer to communicate with devices outside the computer. The interface is suitable for one-of-kind and small-scale designs as well as mass-produced and standard peripheral. The benefits to USB are easy to use, fast and reliable data transfers, flexibility, low cost and power conservation.

#### 3.1.1 SIE

SIE (Serial Interface Engine) is used to control USB communications and check USB protocol, and then transfer protocol to EP decoder. The SIE and USB transceivers, which provide the hardware interface to the USB cable, together comprise the USB engine

#### 3.1.2 USB Command & EP Decoder

The detail description is in Appendix 4.

### 3.2 MAC Interface

#### 3.2.1 MII

The Media Independent Interface (MII) is an 18 wire MAC/Phy interface described in 802.3 u. The purpose of the interface is to allow MAC layer devices to attach to a variety of Physical Layer devices through a common interface. MII operates at either 100 Mbit/s or 10 Mbit/s, dependant on the speed of the Physical Layer. With clocks running at either 25 MHz or 2.5 MHz, 4 bit data is clocked between the MAC and Phy, synchronous with Enable and Error signals.

On receipt of valid data from the wire interface, RX\_DV will go active signaling to the MAC that the valid data will be presented on the RXD[3:0] pins at the speed of the RX\_CLK.

On transmission of data from the MAC, TX\_EN is presented to the phy indicating the presence of valid data on TXD[3:0]. TXD[3:0] are sampled by the phy synchronous to TX\_CLK during the time that TX\_EN is valid.

#### 3.2.2 Adaptive Equalizer

The amplitude and phase distortions from cable cause inter-symbol interference (ISI) which makes clock and data recovery difficult. The adaptive equalizer is designed to closely match the inverse transfer function of the twisted-pairs cable. The equalizer has the ability to change its equalizer frequency response according to the cable length. The equalizer will tune itself automatically to any cable, compensating for the amplitude and phase distortion introduced by the cable.

#### 3.2.3 LEDs

Individual LED output is available to indicate Speed, Duplex, Collision, Transmit, and Link. These multi-function pins are inputs during reset and LED output pins thereafter. The level of these pins during reset determines their active output states. If a multi-function pin is pulled up during reset to select a particular function, the LED output would become active low, and the LED circuit must be designed accordingly, and vice versa.

### 3.2.4 Jabber and SQE

After the MAC transmitter exceeds the jabber timer, the transmit and loopback functions will be disabled and COL signal gets asserted. After TX\_EN goes low for more than 500 ms, the TP transmitter will reactivate and COL gets de-asserted. Setting Jabber Disable will disable the jabber function.

When the SQE test is enabled, a COL pulse is asserted after each transmitted packet. SQE is enabled in 10Base-T by default.

### 3.2.5 Auto Polarity

Certain cable plants have crossed wiring on the twisted pairs; the reversal of TXIN and TXIP. Under normal circumstances this would cause the receive circuitry to reject all data. When the Auto Polarity Disable bit is cleared, the Phy is able to detect the fact that either 8 NLPs (normal link pulse) or a burst of FLPs are inverted and automatically reverses the receiver's polarity. The polarity state is stored in the Reverse Polarity bit.

### 3.2.6 Auto-Negotiation

It provides a linked device with the capability to detect the abilities (modes of operation) supported by the device at the other end of the link, determines common abilities, and configures joint operations. Auto-Negotiation is performed out-of-band using a pulse code sequence that is compatible with the 10Base-T link integrity test sequence.

### 3.2.7 Baseline Wander Compensation

The 100BASE-TX data stream is not always DC balanced. The transformer blocks the DC components of the incoming signal, thus the DC offset of the differential receive inputs can drift. The shifting of the signal level, coupled with non-zero rise, and fall times of the serial stream, can cause pulse-width distortion. This creates jitter and possibly increases in the bit error rates. Therefore, a DC restoration circuit is needed to compensate the attenuation of the DC component. Unlike the traditional implementation, the circuit does not need the feedback information from the slicer or the clock recovery circuit. The design simplifies the circuit design. In 10Base-T, the baseline wander correction circuit is not required.

## 3.3 FIFO Controller

FIFO Controller in receive path is in charge of:

- Store received Ethernet packets to SRAM (internal 24 Kbyte or external 32 Kbyte) and total 32 (or 16) packets can be stored to SRAM. If more than maximum packet counts are received or total packet size is more than 32 K (or 24 K for internal SRAM) bytes, the subsequent coming Ethernet packet will be discarded.
- FIFO controller will load data from SRAM to internal RX FIFO then inform EP Decoder that 64-byte data or a packet is ready in RX FIFO. Before FIFO controller informs this, any USB access to bulk IN endpoint will return NAK. To maintain the data transfer on USB bus via bulk IN transfer must be continuously, thus a 64-byte internal RX FIFO is needed.
- If an Ethernet packet is being received and loading into SRAM while FIFO Controller is moving data from SRAM to internal RX FIFO, writing the Ethernet packet to SRAM will get the higher priority.

FIFO Controller in transmit path is in charge of:

- Store each individual USB packet to internal TX FIFO. When EP decoder informs end of packet, a complete Ethernet packet is stored in TX FIFO. FIFO Controller then informs MAC to transmit this packet.
- Total 4 Ethernet packets can be stored in TX FIFO. If all 4 Ethernet packets are stored in TX FIFO or total packet size is more than 2 K bytes, FIFO Controller will inform EP Decoder that TX FIFO is full and EP Decoder will return NAK if accessing bulk OUT endpoint is invoked. Thus additional USB packet won't be written into TX FIFO until TX FIFO has free space.

### 3.4 TX FIFO and RX FIFO

RX FIFO is a one-port 64-byte FIFO and TX FIFO is a two-port 2 Kbyte FIFO.

### 3.5 1/10/100 Ethernet/HomePNA MAC

The MAC controller takes in charge of:

- Generate CRC then transmit Ethernet packet.
- Check CRC for received packet CRC, filter the received packets.
- Polling PHY status.
- Magic packet detection.
- Automatically transmit PAUSE frame when received status meets the flow control criteria.
- Late collision transmit packets will be discarded.

### 3.6 10/100M Ethernet PHY

The internal Ethernet PHY is compliant to IEEE 802.3u 100Base-TX and IEEE802.3 10Base-T. It provides the whole physical layer functions for both 10M and 100M Ethernet speed. The internal PHY can be isolated by programming register offset 7B<sub>H</sub>, bit 1.

## **4        Registers Description**

System Registers and Transceiver Registers.

## 4.1 System Registers

**Table 12 Registers Address Space**

| Module           | Base Address           | End Address            | Note |
|------------------|------------------------|------------------------|------|
| System Registers | 0000 0000 <sub>H</sub> | 0000 0081 <sub>H</sub> |      |

**Table 13 Registers Overview**

| Register Short Name | Register Long Name                       | Offset Address  | Page Number        |
|---------------------|------------------------------------------|-----------------|--------------------|
| <b>EC0</b>          | Ethernet Control 0                       | 00 <sub>H</sub> | <a href="#">29</a> |
| <b>EC1</b>          | Ethernet Control 1                       | 01 <sub>H</sub> | <a href="#">30</a> |
| <b>EC2</b>          | Ethernet Control 2                       | 02 <sub>H</sub> | <a href="#">31</a> |
| <b>Res0</b>         | Reserved 0                               | 03 <sub>H</sub> | <a href="#">32</a> |
| Res1                | Reserved 1                               | 04 <sub>H</sub> | <a href="#">32</a> |
| Res2                | Reserved 2                               | 05 <sub>H</sub> | <a href="#">32</a> |
| Res3                | Reserved 3                               | 06 <sub>H</sub> | <a href="#">32</a> |
| Res4                | Reserved 4                               | 07 <sub>H</sub> | <a href="#">32</a> |
| <b>MC0</b>          | Multicast 0                              | 08 <sub>H</sub> | <a href="#">32</a> |
| <b>MC1</b>          | Multicast 1                              | 09 <sub>H</sub> | <a href="#">33</a> |
| <b>MC2</b>          | Multicast 2                              | 0A <sub>H</sub> | <a href="#">33</a> |
| <b>MC3</b>          | Multicast 3                              | 0B <sub>H</sub> | <a href="#">33</a> |
| <b>MC4</b>          | Multicast 4                              | 0C <sub>H</sub> | <a href="#">34</a> |
| <b>MC5</b>          | Multicast 5                              | 0D <sub>H</sub> | <a href="#">34</a> |
| <b>MC6</b>          | Multicast 6                              | 0E <sub>H</sub> | <a href="#">34</a> |
| <b>MC7</b>          | Multicast 7                              | 0F <sub>H</sub> | <a href="#">35</a> |
| <b>EID0</b>         | Ethernet ID 0                            | 10 <sub>H</sub> | <a href="#">35</a> |
| <b>EID1</b>         | Ethernet ID 1                            | 11 <sub>H</sub> | <a href="#">36</a> |
| <b>EID2</b>         | Ethernet ID 2                            | 12 <sub>H</sub> | <a href="#">36</a> |
| <b>EID3</b>         | Ethernet ID 3                            | 13 <sub>H</sub> | <a href="#">37</a> |
| <b>EID4</b>         | Ethernet ID 4                            | 14 <sub>H</sub> | <a href="#">37</a> |
| <b>EID5</b>         | Ethernet ID 5                            | 15 <sub>H</sub> | <a href="#">38</a> |
| <b>Res5</b>         | Reserved 5                               | 16 <sub>H</sub> | <a href="#">38</a> |
| <b>Res6</b>         | Reserved 6                               | 17 <sub>H</sub> | <a href="#">38</a> |
| <b>PTL</b>          | Pause Timer Low                          | 18 <sub>H</sub> | <a href="#">39</a> |
| <b>Res7</b>         | Reserved 7                               | 19 <sub>H</sub> | <a href="#">39</a> |
| <b>RPNBFC</b>       | Receive Packet Number Based Flow Control | 1A <sub>H</sub> | <a href="#">40</a> |
| <b>ORFBFC</b>       | Occupied Receive FIFO Based Flow Control | 1B <sub>H</sub> | <a href="#">40</a> |
| <b>EP1C</b>         | EP1 Control                              | 1C <sub>H</sub> | <a href="#">40</a> |
| <b>RXFC</b>         | RX FIFO Control                          | 1D <sub>H</sub> | <a href="#">41</a> |
| <b>BISTC</b>        | BIST Control                             | 1E <sub>H</sub> | <a href="#">41</a> |
| <b>Res8</b>         | Reserved 8                               | 1F <sub>H</sub> | <a href="#">42</a> |
| <b>EEPROMO</b>      | EEPROM Offset                            | 20 <sub>H</sub> | <a href="#">42</a> |
| <b>EEPROMDL</b>     | EEPROM Data Low                          | 21 <sub>H</sub> | <a href="#">43</a> |

## Registers DescriptionSystem Registers

Table 13 Registers Overview (cont'd)

| Register Short Name | Register Long Name             | Offset Address  | Page Number |
|---------------------|--------------------------------|-----------------|-------------|
| <b>EEPROMDH</b>     | EEPROM Data High               | 22 <sub>H</sub> | <b>44</b>   |
| <b>EEPROMAC</b>     | EEPROM Access Control          | 23 <sub>H</sub> | <b>44</b>   |
| <b>Res9</b>         | Reserved 9                     | 24 <sub>H</sub> | <b>45</b>   |
| <b>PHYA</b>         | PHY Address                    | 25 <sub>H</sub> | <b>45</b>   |
| <b>PHYDL</b>        | PHY Data Low                   | 26 <sub>H</sub> | <b>46</b>   |
| <b>PHYDH</b>        | PHY Data High                  | 27 <sub>H</sub> | <b>46</b>   |
| <b>PHYAC</b>        | PHY Access Control             | 28 <sub>H</sub> | <b>47</b>   |
| <b>Res10</b>        | Reserved 10                    | 29 <sub>H</sub> | <b>47</b>   |
| <b>USBBS</b>        | USB Bus Status                 | 2A <sub>H</sub> | <b>48</b>   |
| <b>TS1</b>          | Transmit Status 1              | 2B <sub>H</sub> | <b>48</b>   |
| <b>TS2</b>          | Transmit Status 2              | 2C <sub>H</sub> | <b>49</b>   |
| <b>RS</b>           | Receive Status                 | 2D <sub>H</sub> | <b>50</b>   |
| <b>RLPCH</b>        | Receive Lost Packet Count High | 2E <sub>H</sub> | <b>50</b>   |
| <b>RLPCL</b>        | Receive Lost Packet Count Low  | 2F <sub>H</sub> | <b>51</b>   |
| <b>WUF0_M0</b>      | Wake-Up Frame 0 Mask 0         | 30 <sub>H</sub> | <b>51</b>   |
| WUF0_M1             | Wake-Up Frame 0 Mask 1         | 31 <sub>H</sub> | <b>51</b>   |
| WUF0_M2             | Wake-Up Frame 0 Mask 2         | 32 <sub>H</sub> | <b>51</b>   |
| WUF0_M3             | Wake-Up Frame 0 Mask 3         | 33 <sub>H</sub> | <b>51</b>   |
| WUF0_M4             | Wake-Up Frame 0 Mask 4         | 34 <sub>H</sub> | <b>51</b>   |
| WUF0_M5             | Wake-Up Frame 0 Mask 5         | 35 <sub>H</sub> | <b>51</b>   |
| WUF0_M6             | Wake-Up Frame 0 Mask 6         | 36 <sub>H</sub> | <b>51</b>   |
| WUF0_M7             | Wake-Up Frame 0 Mask 7         | 37 <sub>H</sub> | <b>51</b>   |
| WUF0_M8             | Wake-Up Frame 0 Mask 8         | 38 <sub>H</sub> | <b>51</b>   |
| WUF0_M9             | Wake-Up Frame 0 Mask 9         | 39 <sub>H</sub> | <b>51</b>   |
| WUF0_M10            | Wake-Up Frame 0 Mask 10        | 3A <sub>H</sub> | <b>52</b>   |
| WUF0_M11            | Wake-Up Frame 0 Mask 11        | 3B <sub>H</sub> | <b>52</b>   |
| WUF0_M12            | Wake-Up Frame 0 Mask 12        | 3C <sub>H</sub> | <b>52</b>   |
| WUF0_M13            | Wake-Up Frame 0 Mask 13        | 3D <sub>H</sub> | <b>52</b>   |
| WUF0_M14            | Wake-Up Frame 0 Mask 14        | 3E <sub>H</sub> | <b>52</b>   |
| WUF0_M15            | Wake-Up Frame 0 Mask 15        | 3F <sub>H</sub> | <b>52</b>   |
| <b>WUF0_O</b>       | Wake-Up Frame 0 Offset         | 40 <sub>H</sub> | <b>52</b>   |
| <b>WUF0_CRCL</b>    | Wake-Up Frame 0 CRC Low        | 41 <sub>H</sub> | <b>52</b>   |
| <b>WUF0_CRCH</b>    | Wake-Up Frame 0 CRC High       | 42 <sub>H</sub> | <b>53</b>   |
| <b>Res11</b>        | Reserved 11                    | 43 <sub>H</sub> | <b>53</b>   |
| Res12               | Reserved12                     | 44 <sub>H</sub> | <b>53</b>   |
| Res13               | Reserved13                     | 45 <sub>H</sub> | <b>53</b>   |
| Res14               | Reserved14                     | 46 <sub>H</sub> | <b>53</b>   |
| Res15               | Reserved15                     | 47 <sub>H</sub> | <b>53</b>   |
| <b>WUF1_M0</b>      | Wake-Up Frame 1 Mask 0         | 48 <sub>H</sub> | <b>54</b>   |
| WUF1_M1             | Wake-Up Frame 1 Mask 1         | 49 <sub>H</sub> | <b>54</b>   |
| WUF1_M2             | Wake-Up Frame 1 Mask 2         | 50 <sub>H</sub> | <b>54</b>   |

Table 13 Registers Overview (cont'd)

| Register Short Name | Register Long Name       | Offset Address  | Page Number |
|---------------------|--------------------------|-----------------|-------------|
| WUF1_M3             | Wake-Up Frame 1 Mask 3   | 51 <sub>H</sub> | 54          |
| WUF1_M4             | Wake-Up Frame 1 Mask 4   | 52 <sub>H</sub> | 54          |
| WUF1_M5             | Wake-Up Frame 1 Mask 5   | 53 <sub>H</sub> | 54          |
| WUF1_M6             | Wake-Up Frame 1 Mask 6   | 54 <sub>H</sub> | 54          |
| WUF1_M7             | Wake-Up Frame 1 Mask 7   | 55 <sub>H</sub> | 54          |
| WUF1_M8             | Wake-Up Frame 1 Mask 8   | 56 <sub>H</sub> | 54          |
| WUF1_M9             | Wake-Up Frame 1 Mask 9   | 57 <sub>H</sub> | 54          |
| WUF1_O              | Wake-Up Frame 1 Offset   | 58 <sub>H</sub> | 54          |
| WUF1_CRCL           | Wake-Up Frame 1 CRC Low  | 59 <sub>H</sub> | 55          |
| WUF1_CRCH           | Wake-Up Frame 1 CRC High | 5A <sub>H</sub> | 55          |
| Res16               | Reserved 16              | 5B <sub>H</sub> | 56          |
| Res17               | Reserved 17              | 5C <sub>H</sub> | 56          |
| Res18               | Reserved 18              | 5D <sub>H</sub> | 56          |
| Res19               | Reserved 19              | 5E <sub>H</sub> | 56          |
| Res20               | Reserved 20              | 5F <sub>H</sub> | 56          |
| WUF2_M0             | Wake-Up Frame 2 Mask 0   | 60 <sub>H</sub> | 56          |
| WUF2_M1             | Wake-Up Frame 2 Mask 1   | 61 <sub>H</sub> | 56          |
| WUF2_M2             | Wake-Up Frame 2 Mask 2   | 62 <sub>H</sub> | 56          |
| WUF2_M3             | Wake-Up Frame 2 Mask 3   | 63 <sub>H</sub> | 57          |
| WUF2_M4             | Wake-Up Frame 2 Mask 4   | 64 <sub>H</sub> | 57          |
| WUF2_M5             | Wake-Up Frame 2 Mask 5   | 65 <sub>H</sub> | 57          |
| WUF2_M6             | Wake-Up Frame 2 Mask 6   | 66 <sub>H</sub> | 57          |
| WUF2_M7             | Wake-Up Frame 2 Mask 7   | 67 <sub>H</sub> | 57          |
| WUF2_M8             | Wake-Up Frame 2 Mask 8   | 68 <sub>H</sub> | 57          |
| WUF2_M9             | Wake-Up Frame 2 Mask 9   | 69 <sub>H</sub> | 57          |
| WUF2_M10            | Wake-Up Frame 2 Mask 10  | 6A <sub>H</sub> | 57          |
| WUF2_M11            | Wake-Up Frame 2 Mask 11  | 6B <sub>H</sub> | 57          |
| WUF2_M12            | Wake-Up Frame 2 Mask 12  | 6C <sub>H</sub> | 57          |
| WUF2_M13            | Wake-Up Frame 2 Mask 13  | 6D <sub>H</sub> | 57          |
| WUF2_M14            | Wake-Up Frame 2 Mask 14  | 6E <sub>H</sub> | 57          |
| WUF2_M15            | Wake-Up Frame 2 Mask 15  | 6F <sub>H</sub> | 57          |
| WUF2_O              | Wake-Up Frame 2 Offset   | 70 <sub>H</sub> | 57          |
| WUF2_CRCL           | Wake-Up Frame 2 CRC Low  | 71 <sub>H</sub> | 57          |
| WUF2_CRCH           | Wake-Up Frame 2 CRC High | 72 <sub>H</sub> | 58          |
| Res21               | Reserved 21              | 73 <sub>H</sub> | 58          |
| Res22               | Reserved 22              | 74 <sub>H</sub> | 58          |
| Res23               | Reserved 23              | 75 <sub>H</sub> | 58          |
| Res24               | Reserved 24              | 76 <sub>H</sub> | 58          |
| Res25               | Reserved 25              | 77 <sub>H</sub> | 58          |
| WUC                 | Wake-Up Control          | 78 <sub>H</sub> | 59          |
| Res26               | Reserved 26              | 79 <sub>H</sub> | 59          |

## Registers DescriptionSystem Registers

Table 13 Registers Overview (cont'd)

| Register Short Name | Register Long Name   | Offset Address  | Page Number |
|---------------------|----------------------|-----------------|-------------|
| <b>WUS</b>          | Wake-Up Status       | 7A <sub>H</sub> | <b>60</b>   |
| <b>IPHYC</b>        | Internal PHY Control | 7B <sub>H</sub> | <b>60</b>   |
| <b>GPIO54</b>       | GPIO 5:4             | 7C <sub>H</sub> | <b>61</b>   |
| <b>Res27</b>        | Reserved 27          | 7D <sub>H</sub> | <b>61</b>   |
| <b>GPIO10</b>       | GPIO 1:0             | 7E <sub>H</sub> | <b>62</b>   |
| <b>GPIO32</b>       | GPIO 3:2             | 7F <sub>H</sub> | <b>62</b>   |
| <b>TR</b>           | TEST Register        | 80 <sub>H</sub> | <b>63</b>   |
| <b>TM</b>           | Test Mode            | 81 <sub>H</sub> | <b>64</b>   |

The register is addressed wordwise.

Table 14 Registers Access Types

| Mode                          | Symbol | Description Hardware (HW)                                                                                       | Description Software (SW)                                                                                                                                             |
|-------------------------------|--------|-----------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| read/write                    | rw     | Register is used as input for the HW                                                                            | Register is read and writable by SW                                                                                                                                   |
| read                          | r      | Register is written by HW (register between input and output -> one cycle delay)                                | Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.) |
| write                         | w      |                                                                                                                 | Register is writable by SW                                                                                                                                            |
| read/write hardware affected  | rwh    | Register can be modified by HW                                                                                  | Register can be modified by HW, but the priority SW versus HW has to be specified                                                                                     |
|                               | rwv    |                                                                                                                 |                                                                                                                                                                       |
| Read only                     | ro     | Register is set by HW (register between input and output -> one cycle delay)                                    | SW can only read this register                                                                                                                                        |
| Read virtual                  | rv     | Physically, there is no new register, the input of the signal is connected directly to the address multiplexer. | SW can only read this register                                                                                                                                        |
| Latch high, self clearing     | lhsc   | Latch high signal at high level, clear on read                                                                  | SW can read the register                                                                                                                                              |
| Latch low, self clearing      | llsc   | Latch high signal at low-level, clear on read                                                                   | SW can read the register                                                                                                                                              |
| Latch high, mask clearing     | lhmk   | Latch high signal at high level, register cleared with written mask                                             | SW can read the register, with write mask the register can be cleared (1 clears)                                                                                      |
| Latch low, mask clearing      | llmk   | Latch high signal at low-level, register cleared on read                                                        | SW can read the register, with write mask the register can be cleared (1 clears)                                                                                      |
| Interrupt high, self clearing | ihsc   | Differentiates the input signal (low->high) register cleared on read                                            | SW can read the register                                                                                                                                              |
| Interrupt low, self clearing  | ilsc   | Differentiates the input signal (high->low) register cleared on read                                            | SW can read the register                                                                                                                                              |
| Interrupt high, mask clearing | ihmk   | Differentiates the input signal (high->low) register cleared with written mask                                  | SW can read the register, with write mask the register can be cleared                                                                                                 |

## Registers DescriptionSystem Registers

**Table 14 Registers Access Types (cont'd)**

| Mode                         | Symbol | Description Hardware (HW)                                                                 | Description Software (SW)                                                                                                    |
|------------------------------|--------|-------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------|
| Interrupt low, mask clearing | ilmk   | Differentiates the input signal (low->high) register cleared with written mask            | SW can read the register, with write mask the register can be cleared                                                        |
| Interrupt enable register    | ien    | Enables the interrupt source for interrupt generation                                     | SW can read and write this register                                                                                          |
| latch_on_reset               | lor    | rw register, value is latched after first clock cycle after reset                         | Register is readable and writable by SW                                                                                      |
| Read/write self clearing     | rwsc   | Register is used as input for the hw, the register will be cleared due to a HW mechanism. | Writing to the register generates a strobe signal for the HW (1 pdi clock cycle)<br>Register is readable and writable by SW. |

**Table 15 Registers Clock Domains**

| Clock Short Name | Description |
|------------------|-------------|
|                  |             |

### 4.1.1

#### Ethernet Control 0

| EC0                | Offset          | Reset Value     |
|--------------------|-----------------|-----------------|
| Ethernet Control 0 | 00 <sub>H</sub> | 09 <sub>H</sub> |

| 7          | 6          | 5            | 4          | 3           | 2          | 1           | 0           |
|------------|------------|--------------|------------|-------------|------------|-------------|-------------|
| <b>TXE</b> | <b>RXE</b> | <b>RXFCE</b> | <b>WOE</b> | <b>RXSA</b> | <b>SBO</b> | <b>RXMA</b> | <b>RXCS</b> |
| rw         | rw         | rw           | rw         | rw          | rw         | rw          | rw          |

| Field | Bits | Type | Description                                                                  |
|-------|------|------|------------------------------------------------------------------------------|
| TXE   | 7    | rw   | <b>Enable Ethernet Transmission</b><br>tx_en                                 |
| RXE   | 6    |      | <b>Enable Ethernet Receive</b><br>rx_en                                      |
| RXFCE | 5    |      | <b>Enable Receive Pause Frame</b><br>rx_flowctl_en                           |
| WOE   | 4    |      | <b>Enable Wake-On-LAN Mode</b><br>wakeon_en                                  |
| RXSA  | 3    |      | <b>Enable Status Append at the End of Received Packet</b><br>rxstatus_append |

## Registers DescriptionSystem Registers

| Field | Bits | Type | Description                                                                                                                                                                                 |
|-------|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SBO   | 2    | rw   | <b>Stop Back Off</b><br>0 <sub>B</sub> , back-off counter isn't affected by carrier.<br>1 <sub>B</sub> , back-off counter stops when carrier is active and resumes when carrier is dropped. |
| RXMA  | 1    |      | <b>Receive All Multicast Packet</b><br>rx_multicast_all                                                                                                                                     |
| RXCS  | 0    |      | <b>Include CRC in Receive Packet</b><br>rx_crc_sent                                                                                                                                         |

## Ethernet Control 1

|                           |                       |                       |
|---------------------------|-----------------------|-----------------------|
| <b>EC1</b>                | <b>Offset</b>         | <b>Reset Value</b>    |
| <b>Ethernet Control 1</b> | <b>01<sub>H</sub></b> | <b>00<sub>H</sub></b> |

|     |    |    |     |    |    |     |   |
|-----|----|----|-----|----|----|-----|---|
| 7   | 6  | 5  | 4   | 3  | 2  | 1   | 0 |
| Res | DH | FD | 10M | RM | HM | Res |   |
| ro  | rw | rw | rw  | rw | rw | ro  |   |

| Field | Bits | Type | Description                                                                                                                                      |
|-------|------|------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| Res   | 7    | ro   | <b>Reserved</b>                                                                                                                                  |
| DH    | 6    | rw   | <b>Delay Home</b><br>0 <sub>B</sub> , all data is received after HPN_CRS asserts<br>1 <sub>B</sub> , 1 bit data is dropped after HPN_CRS asserts |
| FD    | 5    |      | <b>Full Duplex</b><br>0 <sub>B</sub> , half-duplex mode<br>1 <sub>B</sub> , full-duplex mode                                                     |
| 10M   | 4    |      | <b>10Mode</b><br>0 <sub>B</sub> , 10Base-T mode<br>1 <sub>B</sub> , 100Base-T mode                                                               |
| RM    | 3    |      | <b>Reset MAC</b><br>Reset MAC, After write 1, HW will clear this bit after MAC resets.                                                           |
| HM    | 2    |      | <b>Homelan Mode</b><br>0 <sub>B</sub> , MII I/F to external PHY<br>1 <sub>B</sub> , 1M8 I/F to external PHY                                      |
| Res   | 1:0  | ro   | <b>Reserved</b>                                                                                                                                  |

## Ethernet Control 2

EC2  
Ethernet Control 2

Offset  
02<sub>H</sub>

Reset Value  
00<sub>H</sub>

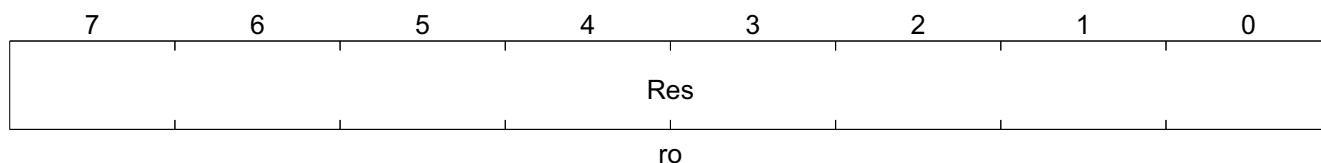
| 7   | 6   | 5    | 4  | 3  | 2   | 1    | 0  |
|-----|-----|------|----|----|-----|------|----|
| Res | LES | EWED | LB | PR | RBP | E3RC |    |
| ro  | rw  | rw   | rw | rw | rw  | rw   | rw |

| Field | Bits | Type | Description                                                                                                                                                     |
|-------|------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Res   | 7:6  | ro   | <b>Reserved</b>                                                                                                                                                 |
| LES   | 5    | rw   | <b>Load EEPROM Start</b><br>When this bit is written with 1, HW will start to load EEPROM.                                                                      |
| EWED  | 4    |      | <b>EEPROM Write Enable/Disable</b><br>0 <sub>B</sub> , EEPROM writes enable/disable command<br>1 <sub>B</sub> , EEPROM writes command                           |
| LB    | 3    |      | <b>Loop Back</b><br>Enables MAC in a loop back mode                                                                                                             |
| PR    | 2    |      | <b>Promiscuous</b><br>0 <sub>B</sub> , receives packets which pass the address filter<br>1 <sub>B</sub> , receives any packet                                   |
| RBP   | 1    |      | rx_bad_pkt<br>0 <sub>B</sub> , filters all bad packets<br>1 <sub>B</sub> , receives bad packets which pass the address filter                                   |
| E3RC  | 0    |      | Ep3_rd_clr/<br>0 <sub>B</sub> , Access EP3, no effect to those registers.<br>1 <sub>B</sub> , Once EP3 is accessed those registers (2B-2F, 7A) will be cleared. |

## Registers DescriptionSystem Registers

## Reserved 0

Res0 Offset Reset Value  
Reserved 0 03<sub>H</sub> 00<sub>H</sub>



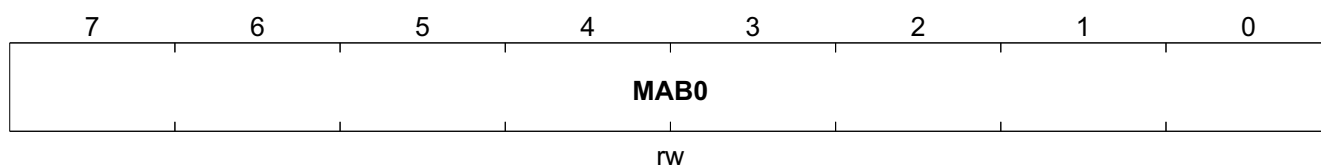
| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res   | 7:0  | ro   | Reserved    |

Table 16 Reserved Registers

| Register Short Name | Register Long Name | Offset Address  | Page Number |
|---------------------|--------------------|-----------------|-------------|
| Res1                | Reserved 1         | 04 <sub>H</sub> |             |
| Res2                | Reserved 2         | 05 <sub>H</sub> |             |
| Res3                | Reserved 3         | 06 <sub>H</sub> |             |
| Res4                | Reserved 4         | 07 <sub>H</sub> |             |

## Multicast 0

MC0 Offset Reset Value  
Multicast 0 08<sub>H</sub> 00<sub>H</sub>



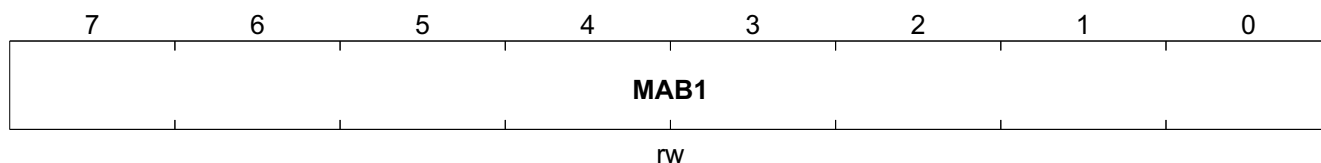
| Field | Bits | Type | Description                |
|-------|------|------|----------------------------|
| MAB0  | 7:0  | rw   | Multicast Address Byte 7:0 |

### Multicast 1

MC1  
Multicast 1

Offset  
09<sub>H</sub>

Reset Value  
00<sub>H</sub>



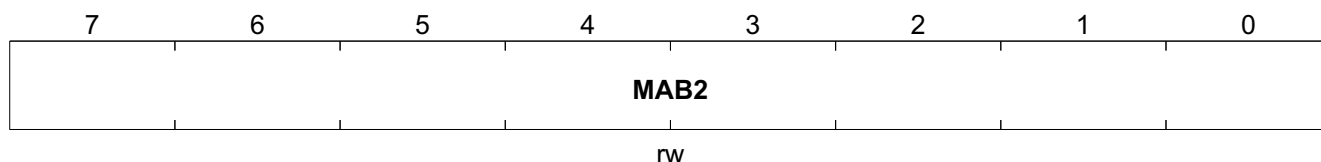
| Field | Bits | Type | Description                 |
|-------|------|------|-----------------------------|
| MAB1  | 7:0  | rw   | Multicast Address Byte 15:8 |

### Multicast 2

MC2  
Multicast 2

Offset  
0A<sub>H</sub>

Reset Value  
00<sub>H</sub>



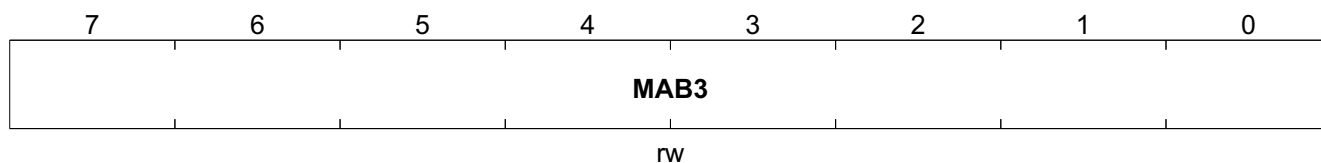
| Field | Bits | Type | Description                  |
|-------|------|------|------------------------------|
| MAB2  | 7:0  | rw   | Multicast Address Byte 23:16 |

### Multicast 3

MC3  
Multicast 3

Offset  
0B<sub>H</sub>

Reset Value  
00<sub>H</sub>



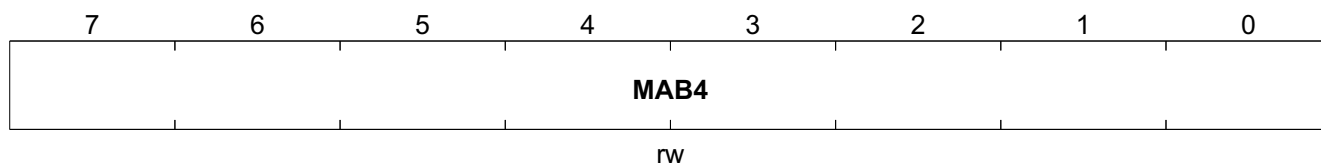
| Field | Bits | Type | Description                  |
|-------|------|------|------------------------------|
| MAB3  | 7:0  | rw   | Multicast Address Byte 31:24 |

### Multicast 4

MC4  
Multicast 4

Offset  
0C<sub>H</sub>

Reset Value  
00<sub>H</sub>



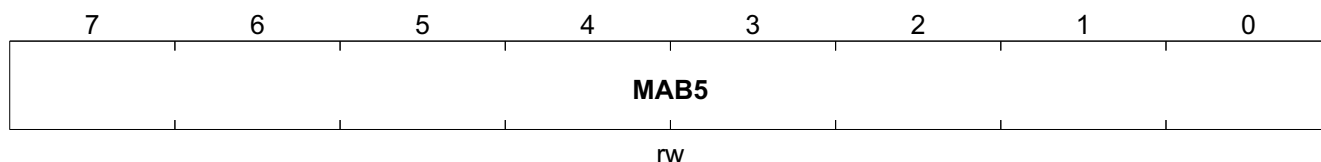
| Field | Bits | Type | Description                  |
|-------|------|------|------------------------------|
| MAB4  | 7:0  | rw   | Multicast Address Byte 39:32 |

### Multicast 5

MC5  
Multicast 5

Offset  
0D<sub>H</sub>

Reset Value  
00<sub>H</sub>



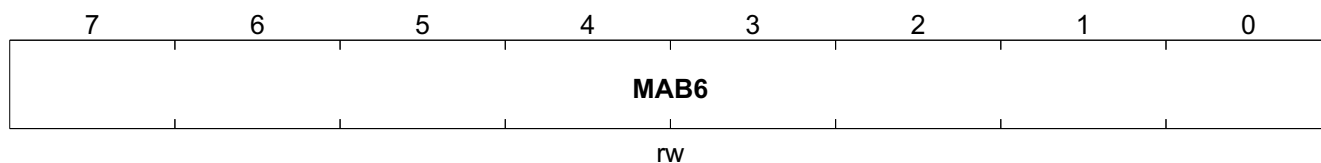
| Field | Bits | Type | Description                  |
|-------|------|------|------------------------------|
| MAB5  | 7:0  | rw   | Multicast Address Byte 47:40 |

### Multicast 6

MC6  
Multicast 6

Offset  
0E<sub>H</sub>

Reset Value  
00<sub>H</sub>



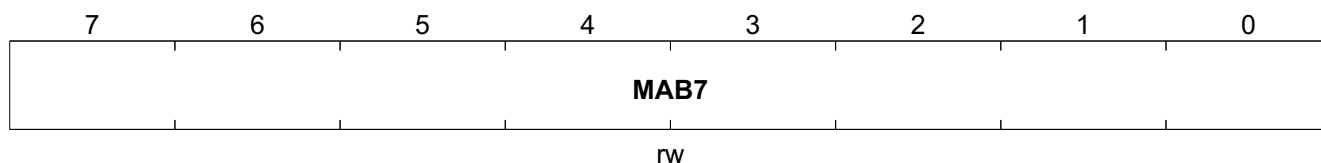
| Field | Bits | Type | Description                  |
|-------|------|------|------------------------------|
| MAB6  | 7:0  | rw   | Multicast Address Byte 55:48 |

## Multicast 7

MC7  
Multicast 7

Offset  
0F<sub>H</sub>

Reset Value  
00<sub>H</sub>



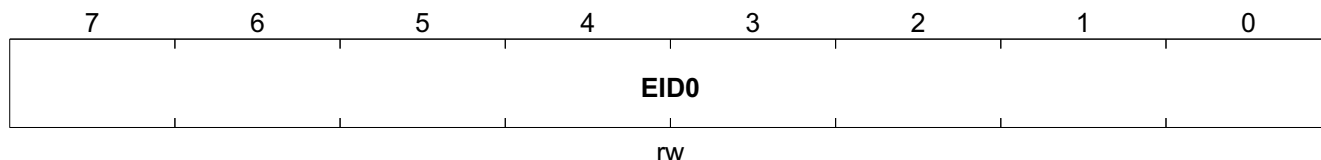
| Field | Bits | Type | Description                  |
|-------|------|------|------------------------------|
| MAB7  | 7:0  | rw   | Multicast Address Byte 63:56 |

## Ethernet ID 0

EID0  
Ethernet ID 0

Offset  
10<sub>H</sub>

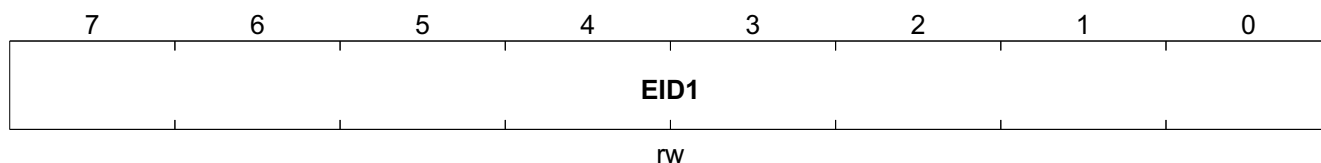
Reset Value  
00<sub>H</sub>



| Field | Bits | Type | Description                                                                                             |
|-------|------|------|---------------------------------------------------------------------------------------------------------|
| EID0  | 7:0  | rw   | <b>Ethernet ID 0</b><br>The 1st byte of ethernet ID is automatically loaded from EEPROM after HW reset. |

## Ethernet ID 1

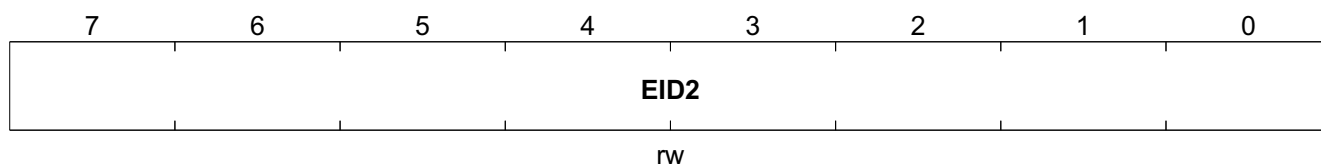
|               |                 |                    |
|---------------|-----------------|--------------------|
| <b>EID1</b>   | <b>Offset</b>   | <b>Reset Value</b> |
| Ethernet ID 1 | 11 <sub>H</sub> | 00 <sub>H</sub>    |



| Field | Bits | Type | Description                                          |
|-------|------|------|------------------------------------------------------|
| EID1  | 7:0  | rw   | <b>Ethernet ID 1</b><br>The 2nd byte of ethernet ID. |

## Ethernet ID 2

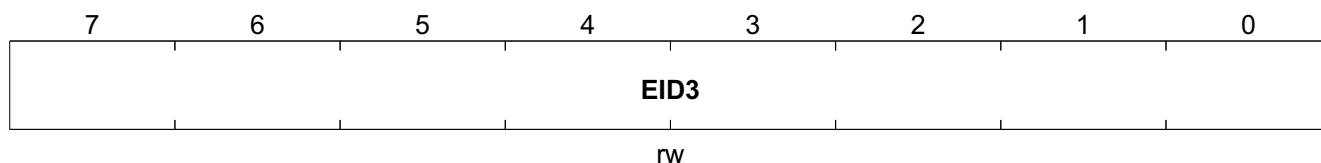
|               |                 |                    |
|---------------|-----------------|--------------------|
| <b>EID2</b>   | <b>Offset</b>   | <b>Reset Value</b> |
| Ethernet ID 2 | 12 <sub>H</sub> | 00 <sub>H</sub>    |



| Field | Bits | Type | Description                                          |
|-------|------|------|------------------------------------------------------|
| EID2  | 7:0  | rw   | <b>Ethernet ID 2</b><br>The 3rd byte of ethernet ID. |

### Ethernet ID 3

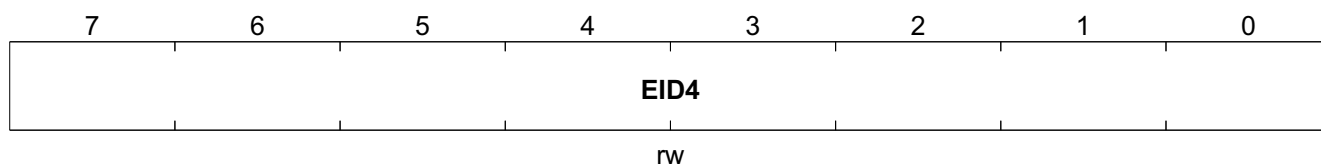
**EID3** **Offset** **Reset Value**  
**Ethernet ID 3** **13<sub>H</sub>** **00<sub>H</sub>**



| Field | Bits | Type | Description                                          |
|-------|------|------|------------------------------------------------------|
| EID3  | 7:0  | rw   | <b>Ethernet ID 3</b><br>The 4th byte of ethernet ID. |

### Ethernet ID 4

**EID4** **Offset** **Reset Value**  
**Ethernet ID 4** **14<sub>H</sub>** **00<sub>H</sub>**

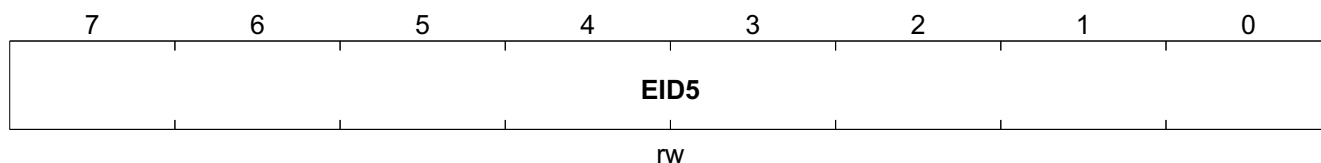


| Field | Bits | Type | Description                                          |
|-------|------|------|------------------------------------------------------|
| EID4  | 7:0  | rw   | <b>Ethernet ID 4</b><br>The 5th byte of ethernet ID. |

## Registers DescriptionSystem Registers

## Ethernet ID 5

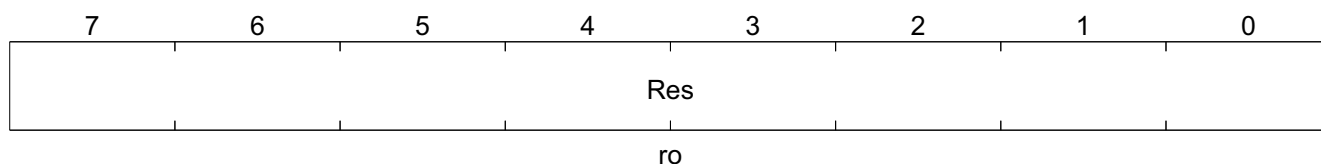
|               |                 |                    |
|---------------|-----------------|--------------------|
| <b>EID5</b>   | <b>Offset</b>   | <b>Reset Value</b> |
| Ethernet ID 5 | 15 <sub>H</sub> | 00 <sub>H</sub>    |



| Field | Bits | Type | Description                                          |
|-------|------|------|------------------------------------------------------|
| EID5  | 7:0  | rw   | <b>Ethernet ID 5</b><br>The 6th byte of ethernet ID. |

## Reserved 5

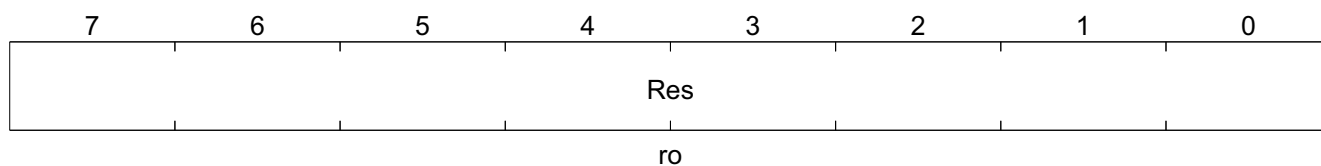
|             |                 |                    |
|-------------|-----------------|--------------------|
| <b>Res5</b> | <b>Offset</b>   | <b>Reset Value</b> |
| Reserved 5  | 16 <sub>H</sub> | 00 <sub>H</sub>    |



| Field | Bits | Type | Description     |
|-------|------|------|-----------------|
| Res   | 7:0  | ro   | <b>Reserved</b> |

## Reserved 6

|             |                 |                    |
|-------------|-----------------|--------------------|
| <b>Res6</b> | <b>Offset</b>   | <b>Reset Value</b> |
| Reserved 6  | 17 <sub>H</sub> | 00 <sub>H</sub>    |

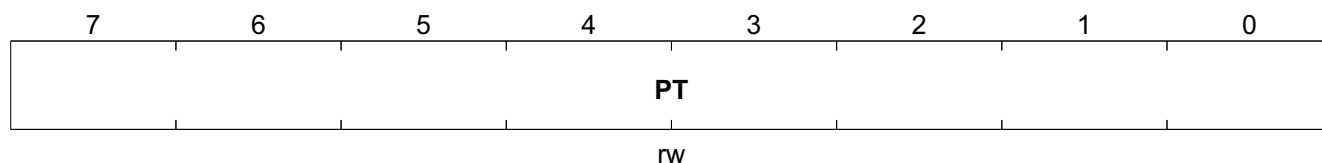


| Field | Bits | Type | Description     |
|-------|------|------|-----------------|
| Res   | 7:0  | ro   | <b>Reserved</b> |

## Registers DescriptionSystem Registers

## Pause Timer Low

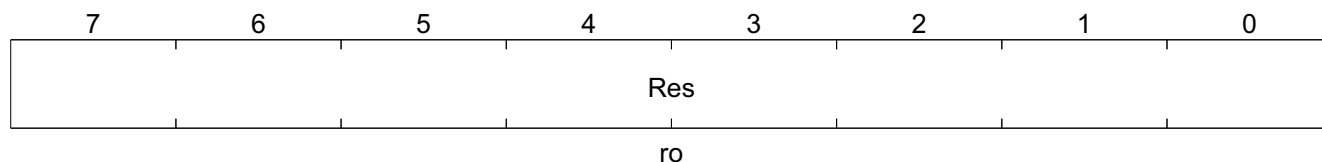
PTL Offset Reset Value  
Pause Timer Low 18<sub>H</sub> 00<sub>H</sub>



| Field | Bits | Type | Description                                                        |
|-------|------|------|--------------------------------------------------------------------|
| PT    | 7:0  | rw   | <b>Pause Timer</b><br>The [11:4] of pause time in the PAUSE frame. |

## Reserved 7

Res7 Offset Reset Value  
Reserved 7 19<sub>H</sub> 00<sub>H</sub>



| Field | Bits | Type | Description     |
|-------|------|------|-----------------|
| Res   | 7:0  | ro   | <b>Reserved</b> |

## Receive Packet Number Based Flow Control

**RPNBFC** **Offset**  
**Receive Packet Number Based Flow Control** **1A<sub>H</sub>** **Reset Value**  
**00<sub>H</sub>**

| 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0  |
|-----|---|---|---|---|---|---|----|
| Res |   |   |   |   |   |   | FP |
| ro  |   |   |   |   |   |   | rw |

| Field | Bits | Type | Description                                                                                                                                                                                                  |
|-------|------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Res   | 7    | ro   | <b>Reserved</b>                                                                                                                                                                                              |
| PN    | 6:1  | rw   | <b>Packet Number</b><br>This field specifies the threshold for transmitting the PAUSE frame. As the received packet number is more than or equal to this field, the PAUSE frame is sent automatically by HW. |
| FP    | 0    | rw   | <b>Flow Control Packet</b><br>Enabled pause frame transmission bases on received packet number.                                                                                                              |

## Occupied Receive FIFO Based Flow Control

**ORFBFC** **Offset**  
**Occupied Receive FIFO Based Flow Control** **1B<sub>H</sub>** **Reset Value**  
**00<sub>H</sub>**

| 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0    |
|-----|---|---|---|---|---|---|------|
| Res |   |   |   |   |   |   | FRXS |
| ro  |   |   |   |   |   |   | rw   |

| Field | Bits | Type | Description                                                                                                                                                                                                                                                                                                          |
|-------|------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Res   | 7    | ro   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                      |
| RXS   | 6:1  | rw   | <b>RX Size</b><br>This field specifies the Kbyte threshold for transmitting the PAUSE frame. As the received FIFO is occupied than or equal to this field, the PAUSE frame is sent automatically by HW. If this field =2, as receive FIFO is occupied more than or equal to 2 Kbyte, the PAUSE frame is transmitted. |
| FRXS  | 0    |      | <b>Flow Control RX Size</b><br>Enabled pause frame transmission bases on occupied receive FIFO size.                                                                                                                                                                                                                 |

## EP1 Control

## Registers DescriptionSystem Registers

**EP1C** **Offset** **Reset Value**  
**EP1 Control** **1C<sub>H</sub>** **00<sub>H</sub>**

|             |            |   |            |   |   |   |   |
|-------------|------------|---|------------|---|---|---|---|
| 7           | 6          | 5 | 4          | 3 | 2 | 1 | 0 |
| <b>EPSE</b> | <b>TIA</b> |   | <b>TIB</b> |   |   |   |   |
| rw          | rw         |   | rw         |   |   |   |   |

| Field | Bits | Type | Description                                                                                                                                                                     |
|-------|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EPSE  | 7    | rw   | <b>EP1 Send0 Enable</b><br>0 <sub>B</sub> , Disables EP1 send 1-byte 00 function<br>1 <sub>B</sub> , Enables EP1 send 1-byte 00 when more than frame_interval's NAK is received |
| TIA   | 6:5  | rw   | <b>Test Interval A</b><br>This value is used for internal test mode.                                                                                                            |
| TIB   | 4:0  | rw   | <b>Test Interval B</b><br>This value is used for internal test mode.                                                                                                            |

## RX FIFO Control

**RXFC** **Offset** **Reset Value**  
**RX FIFO Control** **1D<sub>H</sub>** **00<sub>H</sub>**

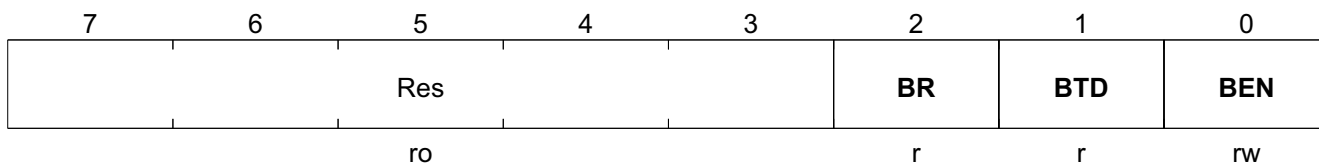
|     |   |   |   |   |   |            |             |
|-----|---|---|---|---|---|------------|-------------|
| 7   | 6 | 5 | 4 | 3 | 2 | 1          | 0           |
| Res |   |   |   |   |   | <b>ESE</b> | <b>R32P</b> |
| ro  |   |   |   |   |   | rw         | rw          |

| Field | Bits | Type | Description                                                                                                                                               |
|-------|------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| Res   | 7:2  | ro   | <b>Reserved</b>                                                                                                                                           |
| ESE   | 1    | rw   | <b>External SRAM Enable</b><br>0 <sub>B</sub> , Supports internal 24 Kbyte SRAM<br>1 <sub>B</sub> , Supports external 32 Kbyte SRAM                       |
| R32P  | 0    |      | <b>Receive 32 Packets</b><br>0 <sub>B</sub> , Supports maximum 16 packets in receive FIFO<br>1 <sub>B</sub> , Supports maximum 32 packets in receive FIFO |

## BIST Control

**BISTC** **Offset** **Reset Value**  
**BIST Control** **1E<sub>H</sub>** **01<sub>H</sub>**

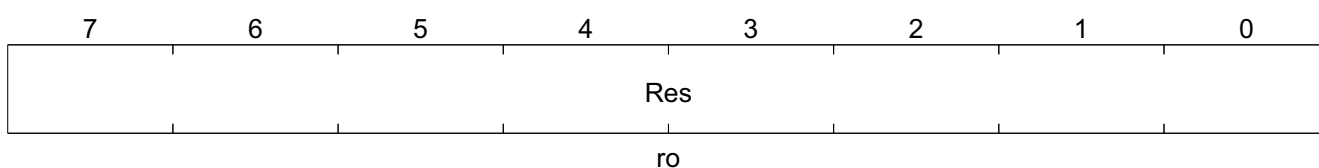
## Registers DescriptionSystem Registers



| Field | Bits | Type | Description                                                                                                                                                                                                                        |
|-------|------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Res   | 7:3  | ro   | <b>Reserved</b>                                                                                                                                                                                                                    |
| BR    | 2    | r    | <b>BIST Result</b><br>This bit indicates the bist result and is valid when “bist_test_done” is ‘1’.<br>This bit also reflects the value of “pass_or_fail” signal in BIST module.<br>0 <sub>B</sub> , Fail<br>1 <sub>B</sub> , Pass |
| BTD   | 1    | r    | <b>BIST Test Done</b><br>This bit indicates the completion of bist. The bist completes if this bit is ‘1’.<br>This bit also reflects the value of “test_done” signal in BIST module.                                               |
| BEN   | 0    | rw   | <b>BIST Enable</b><br>This bit enables the BIST function and also drives the “reset” signal in BIST module.<br>0 <sub>B</sub> , Enable BIST function<br>1 <sub>B</sub> , Disable BIST function                                     |

## Reserved 8

|                   |                       |                       |
|-------------------|-----------------------|-----------------------|
| <b>Res8</b>       | <b>Offset</b>         | <b>Reset Value</b>    |
| <b>Reserved 8</b> | <b>1F<sub>H</sub></b> | <b>00<sub>H</sub></b> |

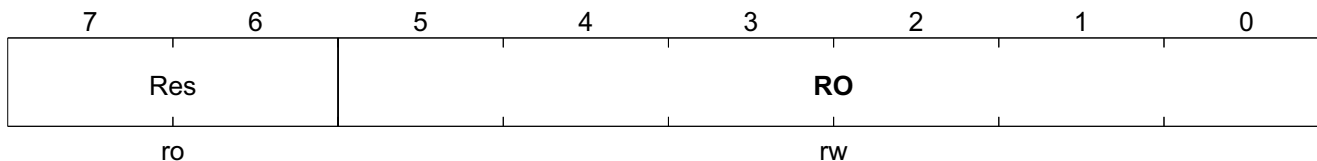


| Field | Bits | Type | Description     |
|-------|------|------|-----------------|
| Res   | 7:0  | ro   | <b>Reserved</b> |

## EEPROM Offset

|                      |                       |                       |
|----------------------|-----------------------|-----------------------|
| <b>EEPROMO</b>       | <b>Offset</b>         | <b>Reset Value</b>    |
| <b>EEPROM Offset</b> | <b>20<sub>H</sub></b> | <b>00<sub>H</sub></b> |

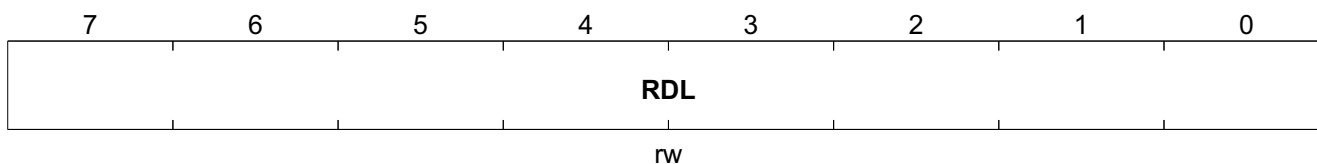
## Registers DescriptionSystem Registers



| Field | Bits | Type | Description                                                       |
|-------|------|------|-------------------------------------------------------------------|
| Res   | 7:6  | ro   | Reserved                                                          |
| RO    | 5:0  | rw   | <b>ROM Offset</b><br>SW sets this register when access to EEPROM. |

## EEPROM Data Low

|                 |                 |                    |
|-----------------|-----------------|--------------------|
| <b>EEPROMDL</b> | <b>Offset</b>   | <b>Reset Value</b> |
| EEPROM Data Low | 21 <sub>H</sub> | 00 <sub>H</sub>    |



| Field | Bits | Type | Description                                                                                                           |
|-------|------|------|-----------------------------------------------------------------------------------------------------------------------|
| RDL   | 7:0  | rw   | <b>ROM Data Low</b><br>SW sets this register when writes to EEPROM. HW sets this register when read data from EEPROM. |



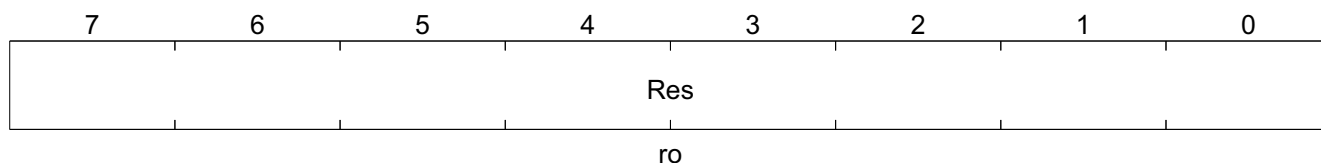
## Registers DescriptionSystem Registers

## Reserved 9

Res9  
Reserved 9

Offset  
24<sub>H</sub>

Reset Value  
00<sub>H</sub>



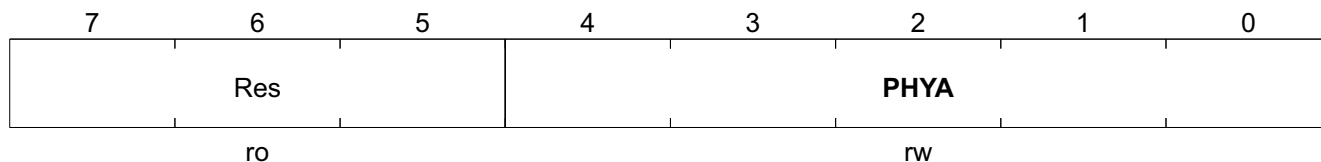
| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res   | 7:0  | ro   | Reserved    |

## PHY Address

PHYA  
PHY Address

Offset  
25<sub>H</sub>

Reset Value  
00<sub>H</sub>

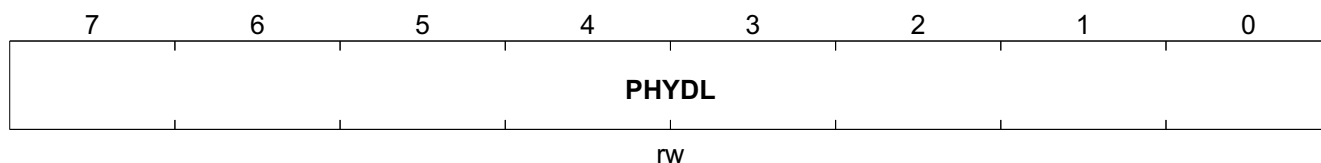


| Field | Bits | Type | Description     |
|-------|------|------|-----------------|
| Res   | 7:5  | ro   | Reserved        |
| PHYA  | 4:0  | rw   | MII PHY Address |

## Registers DescriptionSystem Registers

## PHY Data Low

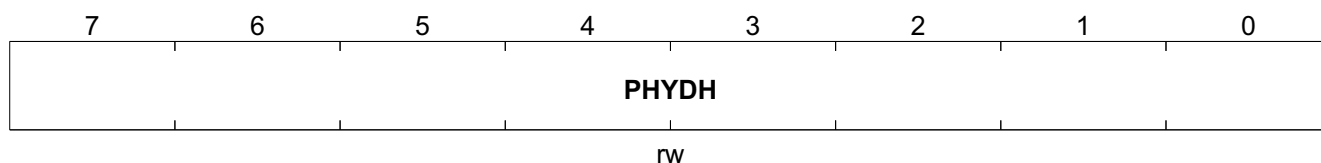
|              |                 |                    |
|--------------|-----------------|--------------------|
| <b>PHYDL</b> | <b>Offset</b>   | <b>Reset Value</b> |
| PHY Data Low | 26 <sub>H</sub> | 00 <sub>H</sub>    |



| Field | Bits | Type | Description                                                                                                                     |
|-------|------|------|---------------------------------------------------------------------------------------------------------------------------------|
| PHYDL | 7:0  | rw   | <b>PHY Data Low</b><br>SW set this register when write to phy registers. HW set this register when read data from PHY register. |

## PHY Data High

|               |                 |                    |
|---------------|-----------------|--------------------|
| <b>PHYDH</b>  | <b>Offset</b>   | <b>Reset Value</b> |
| PHY Data High | 27 <sub>H</sub> | 00 <sub>H</sub>    |



| Field | Bits | Type | Description                                                                                                                      |
|-------|------|------|----------------------------------------------------------------------------------------------------------------------------------|
| PHYDH | 7:0  | rw   | <b>PHY Data High</b><br>SW set this register when write to phy registers. HW set this register when read data from PHY register. |

## Registers DescriptionSystem Registers

## PHY Access Control

|                           |                       |                       |
|---------------------------|-----------------------|-----------------------|
| <b>PHYAC</b>              | <b>Offset</b>         | <b>Reset Value</b>    |
| <b>PHY Access Control</b> | <b>28<sub>H</sub></b> | <b>00<sub>H</sub></b> |

|           |            |            |            |   |   |   |   |
|-----------|------------|------------|------------|---|---|---|---|
| 7         | 6          | 5          | 4          | 3 | 2 | 1 | 0 |
| <b>DO</b> | <b>RDP</b> | <b>WRP</b> | <b>PRA</b> |   |   |   |   |
| rw        | rw         | rw         | rw         |   |   |   |   |

| Field | Bits | Type | Description                                                                                                                                                                   |
|-------|------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DO    | 7    | rw   | <b>Done</b><br>Set by HW to indicate successful completion of PHY access. Clear by SW when initiate a new access to PHY.                                                      |
| RDP   | 6    |      | <b>Read Access to PHY Register</b><br>Set by SW to initiate a read access to PHY register. SW set this bit after it well setting the phy_addr and phyreg_addr.                |
| WRP   | 5    |      | <b>Write Access to PHY Register</b><br>Set by SW to initiate a write access to PHY register. SW set this bit after it well setting the phy_addr, phyreg_addr and phyreg_data. |
| PRA   | 4:0  |      | <b>PHY Register Address</b>                                                                                                                                                   |

## Reserved 10

|                    |                       |                       |
|--------------------|-----------------------|-----------------------|
| <b>Res10</b>       | <b>Offset</b>         | <b>Reset Value</b>    |
| <b>Reserved 10</b> | <b>29<sub>H</sub></b> | <b>00<sub>H</sub></b> |

|            |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|
| 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Res</b> |   |   |   |   |   |   |   |
| ro         |   |   |   |   |   |   |   |

| Field | Bits | Type | Description     |
|-------|------|------|-----------------|
| Res   | 7:0  | ro   | <b>Reserved</b> |

## Registers DescriptionSystem Registers

## USB Bus Status

**USBBS**  
**USB Bus Status**

**Offset**  
**2A<sub>H</sub>**

**Reset Value**  
**00<sub>H</sub>**

| 7   | 6 | 5 | 4 | 3 | 2 | 1  | 0  |
|-----|---|---|---|---|---|----|----|
| Res |   |   |   |   |   | UR | US |
| ro  |   |   |   |   |   | rw | rw |

| Field | Bits | Type | Description                                                                                                          |
|-------|------|------|----------------------------------------------------------------------------------------------------------------------|
| Res   | 7:2  | ro   | <b>Reserved</b>                                                                                                      |
| UR    | 1    | rw   | <b>USB Bus in Resume State</b><br>Set by HW to indicate usb bus in resumed state. Clear by SW read this register.    |
| US    | 0    |      | <b>USB Bus in Suspend State</b><br>Set by HW to indicate usb bus in suspended state. Clear by SW read this register. |

## Transmit Status 1

**TS1**  
**Transmit Status 1**

**Offset**  
**2B<sub>H</sub>**

**Reset Value**  
**00<sub>H</sub>**

| 7   | 6  | 5   | 4  | 3  | 2   | 1   | 0 |
|-----|----|-----|----|----|-----|-----|---|
| TXU | EC | LCE | NC | LC | JTO | Res |   |
| r   | r  | r   | r  | r  | r   | ro  |   |

| Field | Bits | Type | Description                                                                                                                         |
|-------|------|------|-------------------------------------------------------------------------------------------------------------------------------------|
| TXU   | 7    | r    | <b>TX Underrun Error</b><br>Set by HW to indicate tx underrun error. Clear this register by SW Read or after EP3 is accessed.       |
| EC    | 6    |      | <b>Excessive Collision</b><br>Set by HW to indicate excessive collision. Clear this register by SW Read or after EP3 is accessed.   |
| LCE   | 5    |      | <b>Late Collision Error</b><br>Set by HW to indicate late collision error. Clear this register by SW Read or after EP3 is accessed. |
| NC    | 4    | r    | <b>No Carrier</b><br>Set by HW to indicate no carrier. Clear this register by SW Read or after EP3 is accessed.                     |

## Registers DescriptionSystem Registers

| Field | Bits | Type | Description                                                                                                               |
|-------|------|------|---------------------------------------------------------------------------------------------------------------------------|
| LC    | 3    | r    | <b>Loss Carrier</b><br>Set by HW to indicate carrier loss. Clear this register by SW Read or after EP3 is accessed.       |
| JTO   | 2    | r    | <b>Jabber Time Out</b><br>Set by HW to indicate jabber time out. Clear this register by SW Read or after EP3 is accessed. |
| Res   | 1:0  | ro   | <b>Reserved</b>                                                                                                           |

## Transmit Status 2

| TS2               | Offset          | Reset Value     |
|-------------------|-----------------|-----------------|
| Transmit Status 2 | 2C <sub>H</sub> | 00 <sub>H</sub> |

|             |             |     |   |   |   |             |   |
|-------------|-------------|-----|---|---|---|-------------|---|
| 7           | 6           | 5   | 4 | 3 | 2 | 1           | 0 |
| <b>TXFF</b> | <b>TXFE</b> | Res |   |   |   | <b>TXPC</b> |   |
| r           | r           | ro  |   |   |   | r           |   |

| Field | Bits | Type | Description                                                                                                                                                                                                                                    |
|-------|------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TXFF  | 7    | r    | <b>TX Fifo Full</b><br>Set by HW to indicate tx fifo full. Clear this register by SW Read or after EP3 is accessed.                                                                                                                            |
| TXFE  | 6    |      | <b>TX Fifo Empty</b><br>Set by HW to indicate tx fifo empty. Clear this register by SW Read or after EP3 is accessed.                                                                                                                          |
| Res   | 5:4  | ro   | <b>Reserved</b>                                                                                                                                                                                                                                |
| TXPC  | 3:0  | r    | <b>TX Packet Count</b><br>Set by HW to indicate Ethernet transmit packet count every interrupt EP polling. If more than 15 packets have been transmitted, this value will keep as 15. Clear this register by SW Read or after EP3 is accessed. |

## Registers DescriptionSystem Registers

## Receive Status

RS  
Receive Status

Offset  
2D<sub>H</sub>

Reset Value  
00<sub>H</sub>

|     |   |   |   |   |   |     |     |
|-----|---|---|---|---|---|-----|-----|
| 7   | 6 | 5 | 4 | 3 | 2 | 1   | 0   |
| Res |   |   |   |   |   | RXP | RXO |
| ro  |   |   |   |   |   | rw  | r   |

| Field | Bits | Type | Description                                                                                                                  |
|-------|------|------|------------------------------------------------------------------------------------------------------------------------------|
| Res   | 7:2  | ro   | <b>Reserved</b>                                                                                                              |
| RXP   | 1    | rw   | <b>RX Pause</b><br>Set by HW to indicate a PAUSE frame is received. Clear this register by SW Read or after EP3 is accessed. |
| RXO   | 0    | r    | <b>RX Overflow</b><br>Set by HW to indicate external SRAM overflow. Clear this register by SW Read or after EP3 is accessed. |

## Receive Lost Packet Count High

RLPCH  
Receive Lost Packet Count High

Offset  
2E<sub>H</sub>

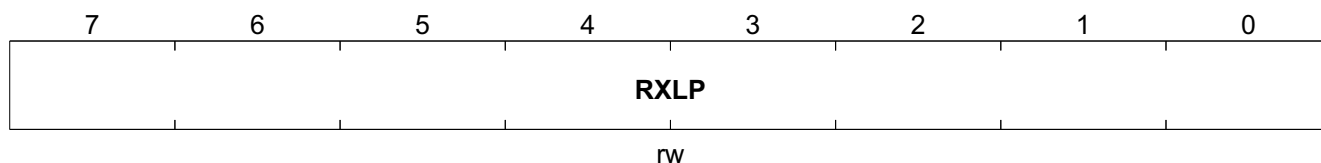
Reset Value  
00<sub>H</sub>

|    |     |   |   |   |   |   |   |
|----|-----|---|---|---|---|---|---|
| 7  | 6   | 5 | 4 | 3 | 2 | 1 | 0 |
| LP | RXL |   |   |   |   |   |   |
| rw | rw  |   |   |   |   |   |   |

| Field | Bits | Type | Description                                                                                                                                            |
|-------|------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| LP    | 7    | rw   | <b>Received Packet Lost</b>                                                                                                                            |
| RXL   | 6:0  |      | <b>RX Lost Packet Count</b><br>The [14:8] of lost packet counts due to receive FIFO overflow. Clear this register by SW Read or after EP3 is accessed. |

## Receive Lost Packet Count Low

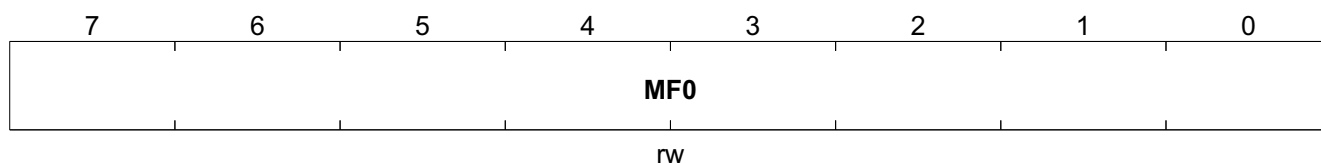
**RLPCL** **Offset** **Reset Value**  
**Receive Lost Packet Count Low** **2F<sub>H</sub>** **00<sub>H</sub>**



| Field | Bits | Type | Description                                                                                                                                     |
|-------|------|------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| RXLP  | 7:0  | rw   | <b>RX Lost Packet</b><br>The [7:0] of lost packet counts due to receive FIFO overflow. Clear this register by SW Read or after EP3 is accessed. |

## Wake-Up Frame 0 Mask 0

**WUF0\_M0** **Offset** **Reset Value**  
**Wake-Up Frame 0 Mask 0** **30<sub>H</sub>** **00<sub>H</sub>**



| Field | Bits | Type | Description                          |
|-------|------|------|--------------------------------------|
| MF0   | 7:0  | rw   | <b>The 128 Mask Bits for Frame 0</b> |

**Table 17 Wake-Up Frame 0 Mask Registers**

| Register Short Name | Register Long Name     | Offset Address  | Page Number |
|---------------------|------------------------|-----------------|-------------|
| WUF0_M1             | Wake-Up Frame 0 Mask 1 | 31 <sub>H</sub> |             |
| WUF0_M2             | Wake-Up Frame 0 Mask 2 | 32 <sub>H</sub> |             |
| WUF0_M3             | Wake-Up Frame 0 Mask 3 | 33 <sub>H</sub> |             |
| WUF0_M4             | Wake-Up Frame 0 Mask 4 | 34 <sub>H</sub> |             |
| WUF0_M5             | Wake-Up Frame 0 Mask 5 | 35 <sub>H</sub> |             |
| WUF0_M6             | Wake-Up Frame 0 Mask 6 | 36 <sub>H</sub> |             |
| WUF0_M7             | Wake-Up Frame 0 Mask 7 | 37 <sub>H</sub> |             |
| WUF0_M8             | Wake-Up Frame 0 Mask 8 | 38 <sub>H</sub> |             |
| WUF0_M9             | Wake-Up Frame 0 Mask 9 | 39 <sub>H</sub> |             |



WUF0\_CRCH

### Wake-Up Frame 0 CRC High

## Offset

 $42_{\text{H}}$ 

### Reset Value

00<sub>H</sub>

Reserved 11

**Res11**

Reserved 11

## Offset

43<sub>H</sub>

### Reset Value

00<sub>H</sub>

### Table 18 Reserved Registers

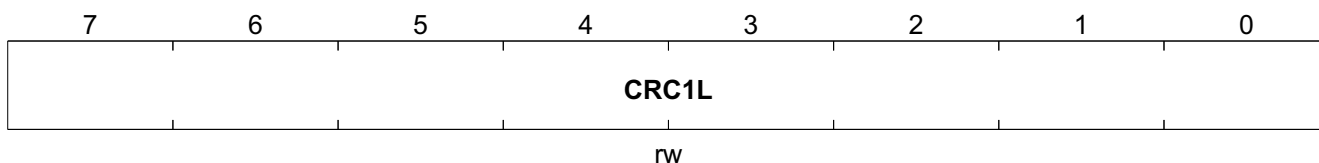


## Wake-Up Frame 1 CRC Low

**WUF1\_CRCL**  
 Wake-Up Frame 1 CRC Low

**Offset**  
 59<sub>H</sub>

**Reset Value**  
 00<sub>H</sub>



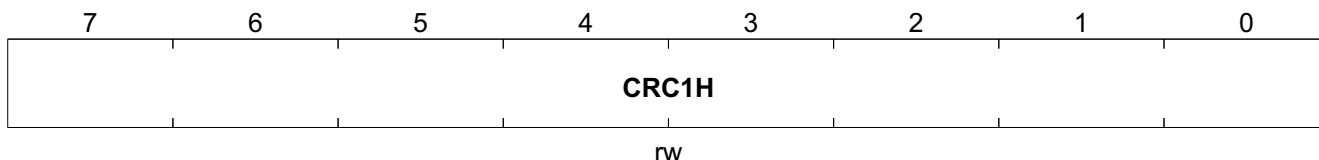
| Field | Bits | Type | Description                              |
|-------|------|------|------------------------------------------|
| CRC1L | 7:0  | rw   | The Low Byte of CRC 16 Match for Frame 1 |

## Wake-Up Frame 1 CRC High

**WUF1\_CRCH**  
 Wake-Up Frame 1 CRC High

**Offset**  
 5A<sub>H</sub>

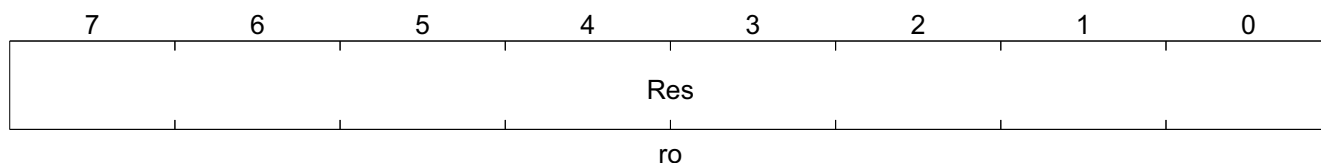
**Reset Value**  
 00<sub>H</sub>



| Field | Bits | Type | Description                               |
|-------|------|------|-------------------------------------------|
| CRC1H | 7:0  | rw   | The High Byte of CRC 16 Match for Frame 1 |

## Reserved 16

**Res16** **Offset** **Reset Value**  
**Reserved 16** **5B<sub>H</sub>** **00<sub>H</sub>**



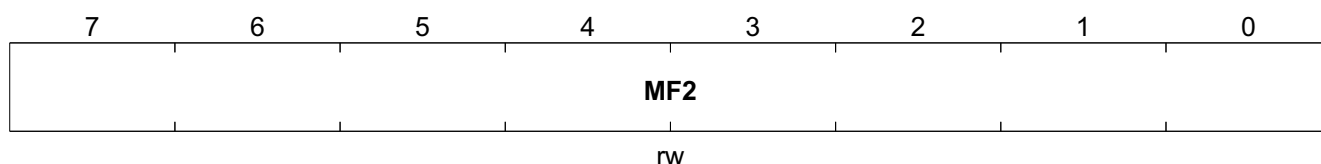
| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res   | 7:0  | ro   | Reserved    |

**Table 20** Reserved Registers

| Register Short Name | Register Long Name | Offset Address  | Page Number |
|---------------------|--------------------|-----------------|-------------|
| Res17               | Reserved 17        | 5C <sub>H</sub> |             |
| Res18               | Reserved 18        | 5D <sub>H</sub> |             |
| Res19               | Reserved 19        | 5E <sub>H</sub> |             |
| Res20               | Reserved 20        | 5F <sub>H</sub> |             |

## Wake-Up Frame 2 Mask 0

**WUF2\_M0** **Offset** **Reset Value**  
**Wake-Up Frame 2 Mask 0** **60<sub>H</sub>** **00<sub>H</sub>**



| Field | Bits | Type | Description                   |
|-------|------|------|-------------------------------|
| MF2   | 7:0  | rw   | The 128 Mask Bits for Frame 2 |

**Table 21** Wake-Up Frame 2 Mask Registers

| Register Short Name | Register Long Name     | Offset Address  | Page Number |
|---------------------|------------------------|-----------------|-------------|
| WUF2_M1             | Wake-Up Frame 2 Mask 1 | 61 <sub>H</sub> |             |
| WUF2_M2             | Wake-Up Frame 2 Mask 2 | 62 <sub>H</sub> |             |



## Wake-Up Frame 2 CRC High

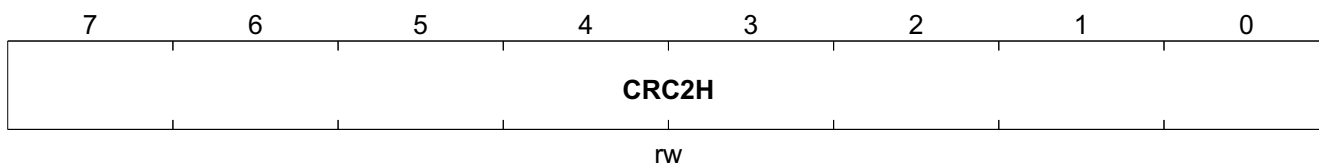
**WUF2\_CRCH**  
**Wake-Up Frame 2 CRC High**

Offset

72<sub>H</sub>

Reset Value

00<sub>H</sub>



| Field | Bits | Type | Description                               |
|-------|------|------|-------------------------------------------|
| CRC2H | 7:0  | rw   | The High Byte of CRC 16 Match for Frame 2 |

## Reserved 21

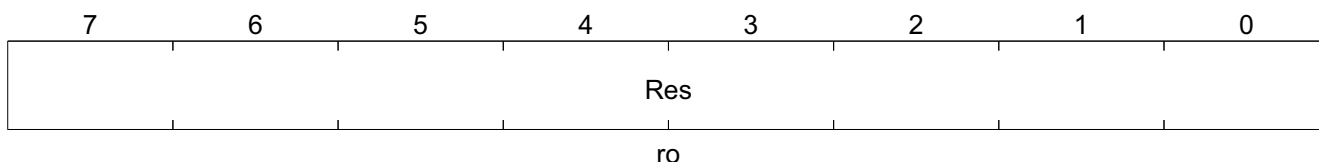
**Res21**  
**Reserved 21**

Offset

73<sub>H</sub>

Reset Value

00<sub>H</sub>



| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res   | 7:0  | ro   | Reserved    |

**Table 22** Reserved Registers

| Register Short Name | Register Long Name | Offset Address  | Page Number |
|---------------------|--------------------|-----------------|-------------|
| Res22               | Reserved 22        | 74 <sub>H</sub> |             |
| Res23               | Reserved 23        | 75 <sub>H</sub> |             |
| Res24               | Reserved 24        | 76 <sub>H</sub> |             |
| Res25               | Reserved 25        | 77 <sub>H</sub> |             |

## Wake-Up Control

**WUC** **Offset** **Reset Value**  
**Wake-Up Control** **78<sub>H</sub>** **04<sub>H</sub>**

|            |           |             |             |             |             |            |   |
|------------|-----------|-------------|-------------|-------------|-------------|------------|---|
| 7          | 6         | 5           | 4           | 3           | 2           | 1          | 0 |
| <b>MPE</b> | <b>LE</b> | <b>WF0E</b> | <b>WF1E</b> | <b>WF2E</b> | <b>C16T</b> | <b>Res</b> |   |
| rw         | rw        | rw          | rw          | rw          | rw          | ro         |   |

| Field | Bits | Type | Description                                                                                                                                       |
|-------|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| MPE   | 7    | rw   | Set by SW to Enable Magic Packet Wake-up Function                                                                                                 |
| LE    | 6    |      | Set by SW to Enable link Status Wake-up Function                                                                                                  |
| WF0E  | 5    |      | Set by SW to Enable Wakeup Frame 0 Wakeup Function                                                                                                |
| WF1E  | 4    |      | Set by SW to Enable Wakeup Frame 1 Wakeup Function                                                                                                |
| WF2E  | 3    |      | Set by SW to Enable Wakeup Frame 2 Wakeup Function                                                                                                |
| C16T  | 2    | ro   | <b>CRC16 Type</b><br>0 <sub>B</sub> , CRC-16 initial contents = 0000 <sub>H</sub><br>1 <sub>B</sub> , CRC-16 initial contents = ffff <sub>H</sub> |
| Res   | 1:0  |      | <b>Reserved</b>                                                                                                                                   |

## Reserved 26

**Res26** **Offset** **Reset Value**  
**Reserved 26** **79<sub>H</sub>** **00<sub>H</sub>**

|            |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|
| 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Res</b> |   |   |   |   |   |   |   |
| ro         |   |   |   |   |   |   |   |

| Field | Bits | Type | Description     |
|-------|------|------|-----------------|
| Res   | 7:0  | ro   | <b>Reserved</b> |

## Registers DescriptionSystem Registers

## Wake-Up Status

WUS  
Wake-Up Status

Offset  
7A<sub>H</sub>

Reset Value  
00<sub>H</sub>

| 7    | 6  | 5    | 4   | 3 | 2 | 1 | 0  |
|------|----|------|-----|---|---|---|----|
| RXMP | LW | RXWF | Res |   |   |   | LS |
| r    | r  | r    | ro  |   |   |   | r  |

| Field | Bits | Type | Description                                                                      |
|-------|------|------|----------------------------------------------------------------------------------|
| RXMP  | 7    | r    | <b>Set by HW when Receive a Magic Packet</b><br>Clear by SW read this register.  |
| LW    | 6    |      | <b>Set by HW when Link Status Change</b><br>Clear by SW read this register.      |
| RXWF  | 5    |      | <b>Set by HW when Receive a Wake-up Frame</b><br>Clear by SW read this register. |
| Res   | 4:1  | ro   | <b>Reserved</b>                                                                  |
| LS    | 0    | r    | <b>Indicate the Current Link Status</b><br>1 for link on, 0 for link off.        |

## Internal PHY Control

IPHYC  
Internal PHY Control

Offset  
7B<sub>H</sub>

Reset Value  
00<sub>H</sub>

| 7   | 6 | 5 | 4 | 3 | 2 | 1   | 0    |
|-----|---|---|---|---|---|-----|------|
| Res |   |   |   |   |   | PDP | PHYR |
| ro  |   |   |   |   |   | rw  | rw   |

| Field | Bits | Type | Description                                                                                                                                                           |
|-------|------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Res   | 7:2  | ro   | <b>Reserved</b>                                                                                                                                                       |
| PDP   | 1    | rw   | <b>Power Down PHY</b><br>0 <sub>B</sub> , Powers down internal 10/100 PHY<br>1 <sub>B</sub> , Enables internal 10/100 PHY                                             |
| PHYR  | 0    |      | <b>PHY Reset</b><br>The internal PHY is reset when this bit is written with 1 and stops reset when this bit is written with 0.<br>1 <sub>B</sub> , Reset internal PHY |

## GPIO 5:4

| GPIO54   | Offset          | Reset Value     |
|----------|-----------------|-----------------|
| GPIO 5:4 | 7C <sub>H</sub> | 00 <sub>H</sub> |

|     |   |      |      |      |      |      |      |
|-----|---|------|------|------|------|------|------|
| 7   | 6 | 5    | 4    | 3    | 2    | 1    | 0    |
| Res |   | G5OE | G5OV | G5IV | G4OE | G4OV | G4IV |
| ro  |   | rw   | rw   | r    | rw   | rw   | r    |

| Field | Bits | Type | Description                                                                                                                   |
|-------|------|------|-------------------------------------------------------------------------------------------------------------------------------|
| Res   | 7:6  | ro   | <b>Reserved</b>                                                                                                               |
| G5OE  | 5    | rw   | <b>GPIO5 Output Enable</b><br>0 <sub>B</sub> , GPIO5 is used for input<br>1 <sub>B</sub> , GPIO5 is used for output           |
| G5OV  | 4    |      | <b>GPIO5 Output Value</b><br>When GPIO5 is used for output, this value is driven to GPIO5 pin. Set by SW.                     |
| G5IV  | 3    | r    | <b>GPIO5 Input Value</b><br>When GPIO5 is used for input, this field reflects the status of GPIO5.<br>Default is pulled-down. |
| G4OE  | 2    | rw   | <b>GPIO4 Output Enable</b><br>0 <sub>B</sub> , GPIO4 is used for input<br>1 <sub>B</sub> , GPIO4 is used for output           |
| G4OV  | 1    |      | <b>GPIO4 Output Value</b><br>When GPIO4 is used for output, this value is driven to GPIO4 pin. Set by SW.                     |
| G4IV  | 0    | r    | <b>GPIO4 Input Value</b><br>When GPIO4 is used for input, this field reflects the status of GPIO4.<br>Default is pulled-down. |

## Reserved 27

| Res27       | Offset          | Reset Value     |
|-------------|-----------------|-----------------|
| Reserved 27 | 7D <sub>H</sub> | 00 <sub>H</sub> |

A horizontal bar representing a 16-bit register. Above the bar, bits are numbered from 7 on the left to 0 on the right. Below the bar, bit 3 is labeled 'Res' and bit 0 is labeled 'ro'.

## Registers DescriptionSystem Registers

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res   | 7:0  | ro   | Reserved    |

## GPIO 1:0

GPIO10  
GPIO 1:0

Offset  
7E<sub>H</sub>

Reset Value  
00<sub>H</sub>

|     |      |      |      |      |      |      |   |
|-----|------|------|------|------|------|------|---|
| 7   | 6    | 5    | 4    | 3    | 2    | 1    | 0 |
| Res | G1OE | G1OV | G1IV | G0OE | G0OV | G0IV |   |
| ro  | rw   | rw   | r    | rw   | rw   | r    |   |

| Field | Bits | Type | Description                                                                                                         |
|-------|------|------|---------------------------------------------------------------------------------------------------------------------|
| Res   | 7:6  | ro   | Reserved                                                                                                            |
| G1OE  | 5    | rw   | <b>GPIO1 Output Enable</b><br>1 <sub>D</sub> , GPIO1 is used for output<br>0 <sub>D</sub> , GPIO1 is used for input |
| G1OV  | 4    |      | <b>GPIO1 Output Value</b><br>When GPIO1 is used for output, this value is driven to GPIO1 pin. Set by SW.           |
| G1IV  | 3    | r    | <b>GPIO1 Input Value</b><br>When GPIO1 is used for input, this field reflects the status of GPIO1. Set by HW.       |
| G0OE  | 2    | rw   | <b>GPIO0 Output Enable</b><br>0 <sub>B</sub> , GPIO0 is used for input<br>1 <sub>B</sub> , GPIO0 is used for output |
| G0OV  | 1    |      | <b>GPIO0 Output Value</b><br>When GPIO0 is used for output, this value is driven to GPIO0 pin. Set by SW.           |
| G0IV  | 0    | r    | <b>GPIO0 Input Value</b><br>When GPIO0 is used for input, this field reflects the status of GPIO0. Set by HW.       |

## GPIO 3:2

GPIO32  
GPIO 3:2

Offset  
7F<sub>H</sub>

Reset Value  
00<sub>H</sub>

## Registers DescriptionSystem Registers

|     |      |      |      |      |      |      |   |
|-----|------|------|------|------|------|------|---|
| 7   | 6    | 5    | 4    | 3    | 2    | 1    | 0 |
| Res | G3OE | G3OV | G3IV | G2OE | G2OV | G2IV |   |
| ro  | rw   | rw   | r    | rw   | rw   | r    |   |

| Field | Bits | Type | Description                                                                                                         |
|-------|------|------|---------------------------------------------------------------------------------------------------------------------|
| Res   | 7:6  | ro   | <b>Reserved</b>                                                                                                     |
| G3OE  | 5    | rw   | <b>GPIO3 Output Enable</b><br>0 <sub>B</sub> , GPIO3 is used for input<br>1 <sub>B</sub> , GPIO3 is used for output |
| G3OV  | 4    |      | <b>GPIO3 Output Value</b><br>When GPIO3 is used for output, this value is driven to GPIO3 pin. Set by SW.           |
| G3IV  | 3    | r    | <b>GPIO3 Input Value</b><br>When GPIO3 is used for input, this field reflects the status of GPIO3. Set by HW.       |
| G2OE  | 2    | rw   | <b>GPIO2 Output Enable</b><br>0 <sub>B</sub> , GPIO2 is used for input<br>1 <sub>B</sub> , GPIO2 is used for output |
| G2OV  | 1    |      | <b>GPIO2 Output Value</b><br>When GPIO2 is used for output, this value is driven to GPIO2 pin. Set by SW.           |
| G2IV  | 0    | r    | <b>GPIO2 Input Value</b><br>When GPIO2 is used for input, this field reflects the status of GPIO2. Set by HW.       |

## TEST Register

|               |                 |                 |
|---------------|-----------------|-----------------|
| TR            | Offset          | Reset Value     |
| TEST Register | 80 <sub>H</sub> | 00 <sub>H</sub> |

|     |    |    |   |   |   |   |   |
|-----|----|----|---|---|---|---|---|
| 7   | 6  | 5  | 4 | 3 | 2 | 1 | 0 |
| Res | GS | UT |   |   |   |   |   |
| ro  | rw | rw |   |   |   |   |   |

| Field | Bits | Type | Description                                                                                                                                       |
|-------|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| Res   | 7:5  | ro   | <b>Reserved</b>                                                                                                                                   |
| GS    | 4:1  | rw   | <b>Internal Probing Signal Group Selection</b><br>group_sel                                                                                       |
| UT    | 0    |      | <b>USB Test</b><br>0 <sub>B</sub> , 6 test pins are used for USB transceiver<br>1 <sub>B</sub> , 6 test pins are used for internal signal probing |



## 4.2 Transceiver Registers

**Table 23 Registers Address Space**

| Module                | Base Address           | End Address            | Note |
|-----------------------|------------------------|------------------------|------|
| Transceiver Registers | 0000 0000 <sub>H</sub> | 0000 001F <sub>H</sub> |      |

**Table 24 Registers Overview**

| Register Short Name | Register Long Name                    | Offset Address  | Page Number |
|---------------------|---------------------------------------|-----------------|-------------|
| <b>CTL</b>          | Control                               | 00 <sub>H</sub> | <b>67</b>   |
| <b>STA</b>          | Status                                | 01 <sub>H</sub> | <b>68</b>   |
| <b>PHY11</b>        | PHY Identifier 1                      | 02 <sub>H</sub> | <b>69</b>   |
| <b>PHY12</b>        | PHY Identifier 2                      | 03 <sub>H</sub> | <b>70</b>   |
| <b>ANA</b>          | Auto-Negotiation Advertisement        | 04 <sub>H</sub> | <b>70</b>   |
| <b>ANLPA</b>        | Auto-Negotiation Link Partner Ability | 05 <sub>H</sub> | <b>71</b>   |
| <b>ANE</b>          | Auto Negotiation Expansion            | 06 <sub>H</sub> | <b>72</b>   |
| <b>ANNPT</b>        | Auto Negotiation Next Page Transmit   | 07 <sub>H</sub> | <b>73</b>   |
| <b>Res28</b>        | Reserved 28                           | 08 <sub>H</sub> | <b>75</b>   |
| Res29               | Reserved 29                           | 09 <sub>H</sub> | <b>75</b>   |
| Res30               | Reserved 30                           | 0A <sub>H</sub> | <b>75</b>   |
| Res31               | Reserved 31                           | 0B <sub>H</sub> | <b>75</b>   |
| Res32               | Reserved 32                           | 0C <sub>H</sub> | <b>75</b>   |
| Res33               | Reserved 33                           | 0D <sub>H</sub> | <b>75</b>   |
| Res34               | Reserved 34                           | 0E <sub>H</sub> | <b>75</b>   |
| Res35               | Reserved 35                           | 0F <sub>H</sub> | <b>75</b>   |
| <b>SPC</b>          | Specific                              | 10 <sub>H</sub> | <b>76</b>   |
| <b>ICS</b>          | Interrupt Control/Status              | 11 <sub>H</sub> | <b>77</b>   |
| <b>DGN</b>          | Diagnostic                            | 12 <sub>H</sub> | <b>78</b>   |
| <b>PWRLB</b>        | Power/Loopback                        | 13 <sub>H</sub> | <b>79</b>   |
| <b>LPM</b>          | Loopback and Power Management         | 14 <sub>H</sub> | <b>80</b>   |
| <b>MCTL</b>         | Mode Control                          | 15 <sub>H</sub> | <b>80</b>   |
| <b>Res36</b>        | Reserved 36                           | 16 <sub>H</sub> | <b>81</b>   |
| <b>PLLL</b>         | PLL Lock                              | 17 <sub>H</sub> | <b>82</b>   |
| <b>REC</b>          | Receive Error Counter                 | 18 <sub>H</sub> | <b>83</b>   |
| Res36               | Reserved 36                           | 19 <sub>H</sub> | <b>75</b>   |
| Res37               | Reserved 37                           | 1A <sub>H</sub> | <b>75</b>   |
| Res38               | Reserved 38                           | 1B <sub>H</sub> | <b>75</b>   |
| Res39               | Reserved 39                           | 1C <sub>H</sub> | <b>75</b>   |
| Res40               | Reserved 40                           | 1D <sub>H</sub> | <b>75</b>   |
| Res41               | Reserved 41                           | 1E <sub>H</sub> | <b>75</b>   |
| Res42               | Reserved 42                           | 1F <sub>H</sub> | <b>75</b>   |

The register is addressed wordwise.

## Registers Description Transceiver Registers

Table 25 Registers Access Types

| Mode                          | Symbol | Description Hardware (HW)                                                                                       | Description Software (SW)                                                                                                                                             |
|-------------------------------|--------|-----------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| read/write                    | rw     | Register is used as input for the HW                                                                            | Register is read and writable by SW                                                                                                                                   |
| read                          | r      | Register is written by HW (register between input and output -> one cycle delay)                                | Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.) |
| write                         | w      |                                                                                                                 | Register is writable by SW                                                                                                                                            |
| read/write hardware affected  | rwh    | Register can be modified by HW                                                                                  | Register can be modified by HW, but the priority SW versus HW has to be specified                                                                                     |
|                               | rwv    |                                                                                                                 |                                                                                                                                                                       |
| Read only                     | ro     | Register is set by HW (register between input and output -> one cycle delay)                                    | SW can only read this register                                                                                                                                        |
| Read virtual                  | rv     | Physically, there is no new register, the input of the signal is connected directly to the address multiplexer. | SW can only read this register                                                                                                                                        |
| Latch high, self clearing     | lhsc   | Latch high signal at high level, clear on read                                                                  | SW can read the register                                                                                                                                              |
| Latch low, self clearing      | llsc   | Latch high signal at low-level, clear on read                                                                   | SW can read the register                                                                                                                                              |
| Latch high, mask clearing     | lhmk   | Latch high signal at high level, register cleared with written mask                                             | SW can read the register, with write mask the register can be cleared (1 clears)                                                                                      |
| Latch low, mask clearing      | llmk   | Latch high signal at low-level, register cleared on read                                                        | SW can read the register, with write mask the register can be cleared (1 clears)                                                                                      |
| Interrupt high, self clearing | ihsc   | Differentiate the input signal (low->high) register cleared on read                                             | SW can read the register                                                                                                                                              |
| Interrupt low, self clearing  | ilsc   | Differentiate the input signal (high->low) register cleared on read                                             | SW can read the register                                                                                                                                              |
| Interrupt high, mask clearing | ihmk   | Differentiate the input signal (high->low) register cleared with written mask                                   | SW can read the register, with write mask the register can be cleared                                                                                                 |
| Interrupt low, mask clearing  | ilmk   | Differentiate the input signal (low->high) register cleared with written mask                                   | SW can read the register, with write mask the register can be cleared                                                                                                 |
| Interrupt enable register     | ien    | Enables the interrupt source for interrupt generation                                                           | SW can read and write this register                                                                                                                                   |
| latch_on_reset                | lor    | rw register, value is latched after first clock cycle after reset                                               | Register is readable and writable by SW                                                                                                                               |
| Read/write self clearing      | rwsc   | Register is used as input for the hw, the register will be cleared due to a HW mechanism.                       | Writing to the register generates a strobe signal for the HW (1 pdi clock cycle)<br>Register is readable and writable by SW.                                          |

Table 26 Registers Clock Domains

| Clock Short Name | Description |
|------------------|-------------|
|                  |             |

## 4.2.1

### Control

| CTL     |    |    |     |    |    |      |    |    | Offset          |   |   |     |   | Reset Value       |   |  |
|---------|----|----|-----|----|----|------|----|----|-----------------|---|---|-----|---|-------------------|---|--|
| Control |    |    |     |    |    |      |    |    | 00 <sub>H</sub> |   |   |     |   | 1000 <sub>H</sub> |   |  |
| 15      | 14 | 13 | 12  | 11 | 10 | 9    | 8  | 7  | 6               | 5 | 4 | 3   | 2 | 1                 | 0 |  |
| RE      | LB | SS | ANE | PD | IS | RAN  | DM | CT |                 |   |   | Res |   |                   |   |  |
| rwsc    | rw | rw | rw  | rw | rw | rwsc | rw | rw |                 |   |   | rw  |   |                   |   |  |

| Field | Bits | Type | Description                                                                                                                                                                             |
|-------|------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RE    | 15   | rwsc | <b>Reset</b><br>This bit is self-clearing.<br>1 <sub>B</sub> , PHY reset                                                                                                                |
| LB    | 14   | rw   | <b>Loopback</b><br>0 <sub>B</sub> , Normal operation<br>1 <sub>B</sub> , Enables loopback mode. This will loopback TXD to RXD, thus it will ignore all the activity on the cable media. |
| SS    | 13   |      | <b>Speed Select</b><br>This bit will be ignored if Auto Negotiation is enabled (0.12=1).<br>0 <sub>B</sub> , 10 Mbit/s<br>1 <sub>B</sub> , 100 Mbit/s                                   |
| ANE   | 12   |      | <b>Auto-Neg. Enable</b><br>0 <sub>B</sub> , Disables auto-negotiate process<br>1 <sub>B</sub> , Enables auto-negotiate process (overrides 0.13 and 0.8)                                 |
| PD    | 11   |      | <b>Power Down</b><br>0 <sub>B</sub> , Normal operation<br>1 <sub>B</sub> , Power down. ADM 8511 will shut off all blocks except for MDIO/MDC interface                                  |
| IS    | 10   |      | <b>Isolate</b><br>0 <sub>B</sub> , Normal operation<br>1 <sub>B</sub> , Electrically isolate the PHY from MII. However, PHY is still able to response to MDC/MDIO                       |
| RAN   | 9    | rwsc | <b>Restart Auto-Negotiation</b><br>0 <sub>B</sub> , Normal operation<br>1 <sub>B</sub> , Restart Auto-Negotiation process                                                               |

## Registers Description Transceiver Registers

| Field | Bits | Type | Description                                                                                                                                                                      |
|-------|------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DM    | 8    | rw   | <b>Dublex Mode</b><br>0 <sub>B</sub> , Half duplex<br>1 <sub>B</sub> , Full duplex                                                                                               |
| CT    | 7    |      | <b>Collision Test</b><br>0 <sub>B</sub> , Disables COL test<br>1 <sub>B</sub> , Enables collision test, which issues the COL signal in response to the assertion of TX_EN signal |
| Res   | 6:0  |      | <b>Reserved</b>                                                                                                                                                                  |

## Status

| STA       |           |           |      |      | Offset          |   |   |   |   | Reset Value       |       |     |       |       |    |
|-----------|-----------|-----------|------|------|-----------------|---|---|---|---|-------------------|-------|-----|-------|-------|----|
| Status    |           |           |      |      | 01 <sub>H</sub> |   |   |   |   | 7849 <sub>H</sub> |       |     |       |       |    |
| 15        | 14        | 13        | 12   | 11   | 10              | 9 | 8 | 7 | 6 | 5                 | 4     | 3   | 2     | 1     | 0  |
| 100T<br>4 | 100F<br>D | 100H<br>D | 10FD | 10HD | Res             |   |   |   |   | ANC               | RF    | ANA | LS    | JD    | EC |
| ro        | ro        | ro        | ro   | ro   | ro              |   |   |   |   | ro                | ro/lh | ro  | ro/ll | ro/lh | ro |

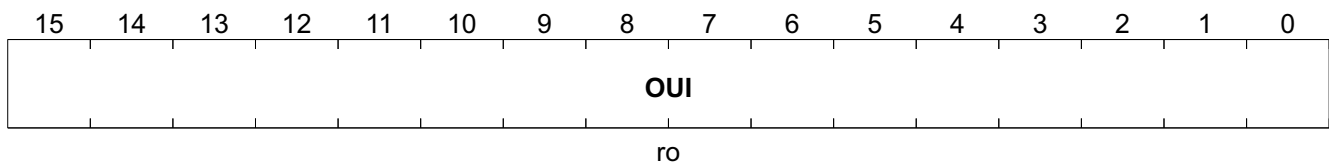
| Field | Bits | Type  | Description                                                                                                                                                                                                 |
|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 100T4 | 15   | ro    | <b>100Base-T4</b><br>Permanently tied to zero indicates no 100Base-T4 capability.                                                                                                                           |
| 100FD | 14   |       | <b>100Base-TX Full Duplex</b><br>0 <sub>B</sub> , No 100Base-TX full duplex ability<br>1 <sub>B</sub> , 100Base-TX with full duplex                                                                         |
| 100HD | 13   |       | <b>100Base-TX Half Duplex</b><br>0 <sub>B</sub> , No TX half-duplex ability<br>1 <sub>B</sub> , 100Base-TX with half duplex                                                                                 |
| 10FD  | 12   |       | <b>10Base-T Full Duplex</b><br>0 <sub>B</sub> , No 10BaseT full duplex ability<br>1 <sub>B</sub> , 10Base-T with full duplex                                                                                |
| 10HD  | 11   |       | <b>10Base-T Half Duplex</b><br>0 <sub>B</sub> , No 10Base-T half duplex ability<br>1 <sub>B</sub> , 10Base-T with half duplex                                                                               |
| Res   | 10:6 |       | <b>Reserved</b>                                                                                                                                                                                             |
| ANC   | 5    | ro/lh | <b>Auto-Negotiate Complete</b><br>0 <sub>B</sub> , Auto-negotiate process not completed<br>1 <sub>B</sub> , Auto-negotiate process completed. Reg. 4, 5, 6 are valid after this bit is set                  |
| RF    | 4    |       | <b>Remote Fault</b><br>This bit will remain set until it is cleared by reading register 1 via management interface.<br>0 <sub>B</sub> , No remote fault<br>1 <sub>B</sub> , Remote fault condition detected |

## Registers Description Transceiver Registers

| Field | Bits | Type  | Description                                                                                                                                                                                                                                          |
|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ANA   | 3    | ro    | <b>Auto-Negotiate Ability</b><br>0 <sub>B</sub> , Unable to perform Auto-Negotiation function<br>1 <sub>B</sub> , Able to perform Auto-Negotiation function                                                                                          |
| LS    | 2    | ro/lh | <b>Link Status</b><br>0 <sub>B</sub> , Link is down<br>1 <sub>B</sub> , Link is established. This is Latched bit. Therefore, if ADM8511/X link failed, this bit will be cleared and remain "0" until register is read again via management interface |
| JD    | 1    | ro/lh | <b>Jabber Detect</b><br>0 <sub>B</sub> , No Jabber condition detected<br>1 <sub>B</sub> , Jabber condition detect                                                                                                                                    |
| EC    | 0    | ro    | <b>Extended Capability</b><br>1 <sub>B</sub> , Extended register capable. This bit is tied permanently to one                                                                                                                                        |

## PHY Identifier 1

| PHYI1            | Offset          | Reset Value       |
|------------------|-----------------|-------------------|
| PHY Identifier 1 | 02 <sub>H</sub> | 0022 <sub>H</sub> |



| Field | Bits | Type | Description                                                                                                                                       |
|-------|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| OUI   | 15:0 | ro   | <b>Organizationally Unique Identifier</b><br>Composed of the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively. |

## Registers Description Transceiver Registers

## PHY Identifier 2

|                  |                 |                   |
|------------------|-----------------|-------------------|
| PHYI2            | Offset          | Reset Value       |
| PHY Identifier 2 | 03 <sub>H</sub> | 5513 <sub>H</sub> |

|     |    |    |    |    |    |    |   |   |   |   |   |    |   |   |   |
|-----|----|----|----|----|----|----|---|---|---|---|---|----|---|---|---|
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8 | 7 | 6 | 5 | 4 | 3  | 2 | 1 | 0 |
| OUI |    |    |    |    |    | MN |   |   |   |   |   | RN |   |   |   |
| ro  |    |    |    |    |    | ro |   |   |   |   |   | ro |   |   |   |

| Field | Bits  | Type | Description                                                                                     |
|-------|-------|------|-------------------------------------------------------------------------------------------------|
| OUI   | 15:10 | ro   | <b>Organizationally Unique Identifier</b><br>Assigned to the 19th through 24th bits of the OUI. |
| MN    | 9:4   |      | <b>Model Number</b><br>Six bit manufacturer's model number.                                     |
| RN    | 3:0   |      | <b>Revision Number</b><br>Four bit manufacturer's revision number.                              |

## Auto-Negotiation Advertisement

|                                |                 |                   |
|--------------------------------|-----------------|-------------------|
| ANA                            | Offset          | Reset Value       |
| Auto-Negotiation Advertisement | 04 <sub>H</sub> | 01E1 <sub>H</sub> |

|    |     |    |    |     |    |           |           |           |      |      |   |   |    |   |   |
|----|-----|----|----|-----|----|-----------|-----------|-----------|------|------|---|---|----|---|---|
| 15 | 14  | 13 | 12 | 11  | 10 | 9         | 8         | 7         | 6    | 5    | 4 | 3 | 2  | 1 | 0 |
| NP | ACK | RF |    | Res |    | 100T<br>4 | 100F<br>D | 100T<br>X | 10FD | 10BT |   |   | SF |   |   |
| rw | ro  | rw |    | rw  |    | ro        | rw        | rw        | rw   | rw   |   |   | rw |   |   |

| Field | Bits  | Type | Description                                                                                                                                  |
|-------|-------|------|----------------------------------------------------------------------------------------------------------------------------------------------|
| NP    | 15    | rw   | <b>Next Page</b><br>0 <sub>B</sub> , Next Page disabled<br>1 <sub>B</sub> , Next Page enabled                                                |
| ACK   | 14    | ro   | <b>Acknowledge</b><br>This bit will be set internally after receiving 3 consecutive and consistent FLP bursts.                               |
| RF    | 13    | rw   | <b>Remote Fault</b><br>0 <sub>B</sub> , No remote fault detected<br>1 <sub>B</sub> , Advertises that this device has detected a Remote Fault |
| Res   | 12:10 |      | <b>Reserved</b><br>For future technology.                                                                                                    |
| 100T4 | 9     | ro   | <b>100Base-T4</b><br>This bit ties to zero.                                                                                                  |

## Registers Description Transceiver Registers

| Field | Bits | Type | Description                                                                                                                                                                                                 |
|-------|------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 100FD | 8    | rw   | <b>100Base-TX Full Duplex</b><br>Default is set by Reg. 1.14.<br>0 <sub>B</sub> , 100Base-TX full duplex not supported by Local device<br>1 <sub>B</sub> , 100Base-TX full duplex supported by Local device |
| 100TX | 7    |      | <b>100Base-TX</b><br>Default is set by Reg. 1.13.<br>0 <sub>B</sub> , 100Base-TX not supported by Local device<br>1 <sub>B</sub> , 100Base-TX supported by Local device                                     |
| 10FD  | 6    |      | <b>10Base-T Full Duplex</b><br>Default is set by Reg. 1.12.<br>0 <sub>B</sub> , 10 Mbit/s full duplex not supported by Local device<br>1 <sub>B</sub> , 10 Mbit/s full duplex supported by Local device     |
| 10BT  | 5    |      | <b>10Base-T</b><br>Default is set by Reg. 1.11.<br>0 <sub>B</sub> , 10 Mbit/s not supported by Local device<br>1 <sub>B</sub> , 10 Mbit/s supported by Local device                                         |
| SF    | 4:0  |      | <b>Selector Field</b><br>Protocol Selection [00001] = IEEE 802.3.                                                                                                                                           |

## Auto-Negotiation Link Partner Ability

## ANLPA

Auto-Negotiation Link Partner Ability

## Offset

05<sub>H</sub>

## Reset Value

0001<sub>H</sub>

|     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |     |    |    |    |    |    |    |    |    |    |   |   |  |  |  |
|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----|----|----|----|----|----|----|----|----|----|---|---|--|--|--|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11  | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1 | 0 |  |  |  |
| Res |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | NP | AC | K  | RF | Res |    | 10 | 10 | 10 | 10 | 10 | SF |    |    |   |   |  |  |  |
|     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | ro | ro | ro |    | ro  |    | ro | ro | ro | ro | ro | ro | ro | ro |   |   |  |  |  |

## Registers Description Transceiver Registers

| Field | Bits  | Type | Description                                                                                                                                                                 |
|-------|-------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NP    | 15    | ro   | <b>Next Page</b><br>0 <sub>B</sub> , Link partner does not desire Next Page transfer<br>1 <sub>B</sub> , Link partner desires Next Page transfer                            |
| ACK   | 14    |      | <b>Acknowledge</b><br>0 <sub>B</sub> , Not acknowledged by Link Partner<br>1 <sub>B</sub> , Link Partner acknowledges reception of FLP words                                |
| RF    | 13    |      | <b>Remote Fault</b><br>0 <sub>B</sub> , No remote fault detected by Link Partner<br>1 <sub>B</sub> , Remote Fault indicated by Link Partner                                 |
| Res   | 12:10 |      | <b>Reserved</b><br>For future technology.                                                                                                                                   |
| 100T4 | 9     |      | <b>100Base-T4</b><br>0 <sub>B</sub> , 100Base-T4 not supported by Link Partner<br>1 <sub>B</sub> , 100Base-T4 supported by Link Partner                                     |
| 100FD | 8     |      | <b>100Base-TX Full Duplex</b><br>0 <sub>B</sub> , 100Base-TX full duplex not supported by Link Partner<br>1 <sub>B</sub> , 100Base-TX full duplex supported by Link Partner |
| 100TX | 7     |      | <b>100Base-TX</b><br>0 <sub>B</sub> , 100Base-TX not supported by Link Partner<br>1 <sub>B</sub> , 100Base-TX supported by Link Partner                                     |
| 10FD  | 6     |      | <b>10Base-T Full Duplex</b><br>0 <sub>B</sub> , 10 Mbit/s full duplex not supported by Link Partner<br>1 <sub>B</sub> , 10 Mbit/s full duplex supported by Link Partner     |
| 10T   | 5     |      | <b>10Base-T</b><br>0 <sub>B</sub> , 10 Mbit/s not supported by Link Partner<br>1 <sub>B</sub> , 10 Mbit/s supported by Link Partner                                         |
| SF    | 4:0   |      | <b>Selector Field</b><br>Protocol Selection [00001] = IEEE 802.3.                                                                                                           |

## Auto Negotiation Expansion

| ANE                                                                                                                                                                                                                                                             | Offset          | Reset Value       |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-------------------|
| Auto Negotiation Expansion                                                                                                                                                                                                                                      | 06 <sub>H</sub> | 0004 <sub>H</sub> |
| <div><div><div>1514131211109876543210</div><div><div>Res</div><div>PDF</div><div>LPNP<br/>A</div><div>NPA</div><div>PR</div><div>LPAN<br/>A</div></div></div><div><div>ro</div><div>ro/lh</div><div>ro</div><div>ro</div><div>ro</div><div>ro</div></div></div> |                 |                   |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res   | 15:5 | ro   | Reserved    |

## Registers Description Transceiver Registers

| Field | Bits | Type  | Description                                                                                                                                                                                                                                                                                                                    |
|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PDF   | 4    | ro/lh | <b>Parallel Detection Fault</b><br>$0_B$ , No fault detected by parallel detection logic<br>$1_B$ , Fault detected by parallel detection logic, this fault is due to more than one technology detecting concurrent link up condition. This bit can only be cleared by reading this register and using the management interface |
| LPNPA | 3    | ro    | <b>Link Partner Next Page Able</b><br>$0_B$ , Link partner does not support next page function<br>$1_B$ , Link partner support next page function                                                                                                                                                                              |
| NPA   | 2    |       | <b>Next Page Able</b><br>Next page is supported, i.e., this bit is permanently tied to 1.                                                                                                                                                                                                                                      |
| PR    | 1    |       | <b>Page Received</b><br>It is set when a new link code word has been received into the Auto-Negotiation Link Partner Ability Register. This bit is cleared upon a read of this register.                                                                                                                                       |
| LPANA | 0    |       | <b>Link Partner Auto-Negotiation Able</b><br>$0_B$ , Link partner is not Auto-Negotiation capable<br>$1_B$ , Link partner is Auto-Negotiation capable                                                                                                                                                                          |

## Auto Negotiation Next Page Transmit Register

|                                            |                       |                         |
|--------------------------------------------|-----------------------|-------------------------|
| <b>ANNPT</b>                               | <b>Offset</b>         | <b>Reset Value</b>      |
| <b>Auto Negotiation Next Page Transmit</b> | <b>07<sub>H</sub></b> | <b>2001<sub>H</sub></b> |

|            |            |           |             |            |    |   |   |   |   |           |   |   |   |   |   |
|------------|------------|-----------|-------------|------------|----|---|---|---|---|-----------|---|---|---|---|---|
| 15         | 14         | 13        | 12          | 11         | 10 | 9 | 8 | 7 | 6 | 5         | 4 | 3 | 2 | 1 | 0 |
| <b>NPI</b> | <b>Res</b> | <b>MP</b> | <b>ACK2</b> | <b>TTX</b> |    |   |   |   |   | <b>CO</b> |   |   |   |   |   |
| rw         | ro         | rw        | rw          | rw         |    |   |   |   |   | rw        |   |   |   |   |   |

| Field | Bits | Type | Description                                                                                                     |
|-------|------|------|-----------------------------------------------------------------------------------------------------------------|
| NPI   | 15   | rw   | <b>Next Page Indication</b><br>$0_B$ , No other Next Page Transfer desired<br>$1_B$ , Another Next Page desired |
| Res   | 14   | ro   | <b>Reserved</b>                                                                                                 |

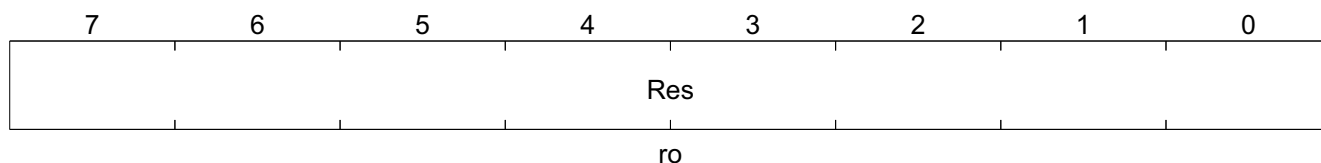
## Registers Description Transceiver Registers

| Field | Bits | Type | Description                                                                                                                                           |
|-------|------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| MP    | 13   | rw   | <b>Message Page</b><br>$0_B$ , Un-formatted page<br>$1_B$ , Message page                                                                              |
| ACK2  | 12   |      | <b>Acknowledge 2</b><br>$0_B$ , Cannot comply with message<br>$1_B$ , Will comply with message                                                        |
| TTX   | 11   |      | <b>Toggle</b><br>$0_B$ , Previous value of transmitted link code word equals to 1<br>$1_B$ , Previous value of transmitted link code word equals to 0 |
| CO    | 10:0 |      | <b>Code</b><br>Message/Un-formatted Code Field.                                                                                                       |

## Registers Description Transceiver Registers

## Reserved 28

| Res28       | Offset          | Reset Value       |
|-------------|-----------------|-------------------|
| Reserved 28 | 08 <sub>H</sub> | xxxx <sub>H</sub> |



| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res   | 7:0  | ro   | Reserved    |

Table 27 Reserved Registers

| Register Short Name | Register Long Name | Offset Address  | Page Number |
|---------------------|--------------------|-----------------|-------------|
| Res29               | Reserved 29        | 09 <sub>H</sub> |             |
| Res30               | Reserved 30        | 0A <sub>H</sub> |             |
| Res31               | Reserved 31        | 0B <sub>H</sub> |             |
| Res32               | Reserved 32        | 0C <sub>H</sub> |             |
| Res33               | Reserved 33        | 0D <sub>H</sub> |             |
| Res34               | Reserved 34        | 0E <sub>H</sub> |             |
| Res35               | Reserved 35        | 0F <sub>H</sub> |             |
| Res36               | Reserved 36        | 19 <sub>H</sub> |             |
| Res37               | Reserved 37        | 1A <sub>H</sub> |             |
| Res38               | Reserved 38        | 1B <sub>H</sub> |             |
| Res39               | Reserved 39        | 1C <sub>H</sub> |             |
| Res40               | Reserved 40        | 1D <sub>H</sub> |             |
| Res41               | Reserved 41        | 1E <sub>H</sub> |             |
| Res42               | Reserved 42        | 1F <sub>H</sub> |             |



## Registers Description Transceiver Registers

## Interrupt Control/Status

ICS Offset Reset Value  
Interrupt Control/Status 11<sub>H</sub> 0000<sub>H</sub>

| 15  | 14  | 13  | 12  | 11  | 10   | 9   | 8     | 7   | 6   | 5    | 4    | 3    | 2     | 1    | 0     |
|-----|-----|-----|-----|-----|------|-----|-------|-----|-----|------|------|------|-------|------|-------|
| JIE | REI | PRI | PFI | LAI | LNOI | RFI | ANCIE | JIN | REI | PRIN | PFIN | LAIN | LNOIN | RFIN | ANCIN |
| rw  | rw  | rw  | rw  | rw  | rw   | rw  | rw    | rc  | rc  | rc   | rc   | rc   | rc    | rc   | rc    |

| Field | Bits | Type | Description                                                       |
|-------|------|------|-------------------------------------------------------------------|
| JIE   | 15   | rw   | <b>Jabber Interrupt Enable</b><br>Jabber_IE                       |
| REI   | 14   |      | <b>Receive Error Interrupt Enable</b><br>Rx_Er_IE                 |
| PRI   | 13   |      | <b>Page Received Interrupt Enable</b><br>Page_Rx_IE               |
| PFI   | 12   | rw   | <b>Parallel Detection Fault Interrupt Enable</b><br>PD_Fault_IE   |
| LAI   | 11   |      | <b>Link Partner Acknowledge Interrupt Enable</b><br>LP_Ack_IE     |
| LNOI  | 10   |      | <b>Link Status Not OK Interrupt Enable</b><br>Link_Not_OK_IE      |
| RFI   | 9    |      | <b>Remote Fault Interrupt Enable</b><br>R_Fault_IE                |
| ANCIE | 8    |      | <b>Auto-Negotiation Complete Interrupt Enable</b><br>ANeg_Comp_IE |

## Registers Description Transceiver Registers

| Field | Bits | Type | Description                                                                                                         |
|-------|------|------|---------------------------------------------------------------------------------------------------------------------|
| JIN   | 7    | rc   | <b>This Bit is Set when a Jabber Event is Detected</b><br>Jabber_Int                                                |
| REI   | 6    |      | <b>This Bit is Set when RX_ER Transitions High</b><br>Rx_Er_Int                                                     |
| PRIN  | 5    |      | <b>This Bit is Set when a New Page is Received from Link Partner During Auto-Neg.</b><br>Page_Rx_Int                |
| PFIN  | 4    |      | <b>This Bit is Set when Parallel Detect Fault is Detected</b><br>PD_Fault_Int                                       |
| LAIN  | 3    |      | <b>This Bit is Set when the FLP with Acknowledge Bit Set is Received</b><br>LP_Ack_Int                              |
| LNOIN | 2    |      | <b>This Bit is Set when Link Status Switches from OK Status to Non-OK Status (Fail or Ready)</b><br>Link_Not_OK Int |
| RFIN  | 1    |      | <b>This Bit is Set when Remote Fault is Detected</b><br>R_Fault_Int                                                 |
| ANCIN | 0    |      | <b>This Bit is Set when Auto-Neg is Complete</b><br>A_Neg_Comp Int                                                  |

Note: See Interrupt Table for bit Assignments

## Diagnostic

| DGN        | Offset          | Reset Value       |
|------------|-----------------|-------------------|
| Diagnostic | 12 <sub>H</sub> | 0000 <sub>H</sub> |

|     |    |    |    |      |    |     |       |     |   |   |   |   |   |   |   |
|-----|----|----|----|------|----|-----|-------|-----|---|---|---|---|---|---|---|
| 15  | 14 | 13 | 12 | 11   | 10 | 9   | 8     | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Res |    |    |    | DPLX | SP | RXP | RXL   | Res |   |   |   |   |   |   |   |
| ro  |    |    |    | ro   | ro | ro  | ro/sc | ro  |   |   |   |   |   |   |   |

| Field | Bits  | Type | Description                                                                                                                                                                             |
|-------|-------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Res   | 15:12 | ro   | <b>Reserved</b>                                                                                                                                                                         |
| DPLX  | 11    |      | <b>Duplex</b><br>This bit indicates the result of the Auto-Neg for duplex arbitration.                                                                                                  |
| SP    | 10    |      | <b>Speed</b><br>This bit indicates the result of the Auto-Neg for data speed arbitration.                                                                                               |
| RXP   | 9     |      | <b>RX_PASS</b><br>In 10BT mode, this bit indicates that Manchester data has been detected. In 100BT mode, it indicates valid signal has been received but not necessarily locked on to. |

## Registers Description Transceiver Registers

| Field | Bits | Type  | Description                                                                                                                                                                                                                       |
|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RXL   | 8    | ro/sc | <b>RX_LOCK</b><br>Indicates the receive PLL has locked onto the received signal for the selected speed of operation (10Base-T or 100Base-TX). This bit is set whenever a cycle-slip occurs, and will remain set until it is read. |
| Res   | 7:0  | ro    | <b>Reserved</b>                                                                                                                                                                                                                   |

## Power/Loopback

|                       |                       |                         |
|-----------------------|-----------------------|-------------------------|
| <b>PWRLB</b>          | <b>Offset</b>         | <b>Reset Value</b>      |
| <b>Power/Loopback</b> | <b>13<sub>H</sub></b> | <b>0020<sub>H</sub></b> |

|     |    |    |    |    |     |   |   |   |      |     |     |     |      |      |    |
|-----|----|----|----|----|-----|---|---|---|------|-----|-----|-----|------|------|----|
| 15  | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6    | 5   | 4   | 3   | 2    | 1    | 0  |
| Res |    |    |    |    | Res |   |   |   | TTRS | LPM | TLB | DLP | LPBK | NLIT | RT |
|     |    |    |    |    |     |   |   |   | rw   | rw  | rw  | rw  | rw   | rw   | r  |

| Field | Bits | Type | Description                                                                                                                                                                                    |
|-------|------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Res   | 14:7 | ro   | <b>Reserved</b>                                                                                                                                                                                |
| TTRS  | 6    | rw   | <b>Transmit Transformer Ratio Selection</b><br>TP125<br>0 <sub>B</sub> , 1:1<br>1 <sub>B</sub> , 1.25:1                                                                                        |
| LPM   | 5    |      | <b>Low Power Mode</b><br>0 <sub>B</sub> , Disables advanced power saving mode<br>1 <sub>B</sub> , Enables advanced power saving mode                                                           |
| TLB   | 4    |      | <b>Test Loopback</b><br>1 <sub>B</sub> , Enables test loopback. Data will be transmitted from MII interface to clock recovery and loopback to MII received data                                |
| DLP   | 3    |      | <b>Digital Loopback</b><br>0 <sub>B</sub> , Normal operation<br>1 <sub>B</sub> , Enables loopback                                                                                              |
| LPBK  | 2    |      | LP_LPBK<br>0 <sub>B</sub> , Normal operation<br>1 <sub>B</sub> , Enables link pulse loopback                                                                                                   |
| NLIT  | 1    |      | <b>NLP Link Integrity Test</b><br>0 <sub>B</sub> , Sending FLP in Auto-Neg test mode<br>1 <sub>B</sub> , In Auto-Neg test mode, send NLP instead of FLP in order to test NLP receive integrity |
| RT    | 0    | r    | <b>Reduce Timer</b><br>0 <sub>B</sub> , Normal operation<br>1 <sub>B</sub> , Reduce time constant for Auto-Negotiation timer                                                                   |

## Registers Description Transceiver Registers

## Loopback and Power Management

**LPM** **Offset** **Reset Value**  
**Loopback and Power Management** **14<sub>H</sub>** **xxFx<sub>H</sub>**

| 15  | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7   | 6 | 5 | 4 | 3   | 2 | 1 | 0 |
|-----|----|----|----|----|----|---|---|-----|---|---|---|-----|---|---|---|
| Res |    |    |    |    |    |   |   | CMC |   |   |   | Res |   |   |   |
| ro  |    |    |    |    |    |   |   | ro  |   |   |   | ro  |   |   |   |

| Field | Bits | Type | Description                                                                                                                                                                                                                                                                                                                               |
|-------|------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Res   | 15:8 | ro   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                           |
| CMC   | 7:4  |      | <b>Cable Measurement Capability</b><br>These bits can be used as cable length indicator. The bits are incremented from 0000 to 1111, with an increment of approximately 10 meters. The equivalent is 0 to 32 dB with an increment of 2 dB @ 100 MHz. The value is a read back from the equalizer, and the measured value is not absolute. |
| Res   | 3:0  |      | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                           |

## Mode Control

**MCTL** **Offset** **Reset Value**  
**Mode Control** **15<sub>H</sub>** **0304<sub>H</sub>**

| 15  | 14   | 13  | 12  | 11        | 10  | 9 | 8   | 7   | 6     | 5    | 4    | 3             | 2   | 1 | 0   |
|-----|------|-----|-----|-----------|-----|---|-----|-----|-------|------|------|---------------|-----|---|-----|
| Res | NLPD | FLU | JDI | 10BT<br>S | Res |   | FDI | FFT | RECF  | DREC | DWDT | ERP<br>B<br>K | DSC |   | Res |
| ro  | rw   | rw  | rw  | rw        | ro  |   | rw  | rw  | ro/rc | rw   | rw   | rw            | rw  |   | ro  |

| Field | Bits | Type | Description     |
|-------|------|------|-----------------|
| Res   | 15   | ro   | <b>Reserved</b> |

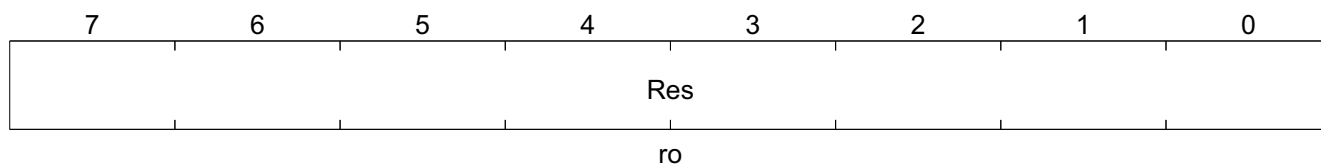
## Registers Description Transceiver Registers

| Field | Bits | Type  | Description                                                                                                                                                                        |
|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NLPD  | 14   | rw    | <b>NLP Disable</b><br>0 <sub>B</sub> , Normal Operation<br>1 <sub>B</sub> , Force 10B-T link up without checking NLP                                                               |
| FLU   | 13   |       | Force_link_up<br>1 <sub>B</sub> , Force link up, auto negotiation must be disabled at this time                                                                                    |
| JDI   | 12   |       | <b>Jabber Disable</b><br>0 <sub>B</sub> , Enables Jabber function in PHY<br>1 <sub>B</sub> , Disables Jabber function in PHY                                                       |
| 10BTS | 11   |       | 10BT_Sel<br>0 <sub>B</sub> , Normal operation<br>1 <sub>B</sub> , Enables 7-wire interface for 10Base-T operation. This bit is useful only when the chip is not in PCS bypass mode |
| Res   | 10:9 | ro    | <b>Reserved</b>                                                                                                                                                                    |
| FDI   | 8    | rw    | FEF_Disable<br>0 <sub>B</sub> , Disables far-end-fault<br>1 <sub>B</sub> , Enables far-end-fault generation and detection function                                                 |
| FFT   | 7    |       | <b>Force FEF Transmit</b><br>This bit is set to force to transmit Far End Fault (FEF) pattern.                                                                                     |
| RECF  | 6    | ro/rc | Rx_Er_Cnt Full<br>When Receive Error Counter is full, this bit will get set to one.                                                                                                |
| DREC  | 5    | rw    | Disable Rx_Er_Cnt<br>0 <sub>B</sub> , Enables Receive Error Counter<br>1 <sub>B</sub> , Disables Receive Error Counter                                                             |
| DWDT  | 4    |       | Dis_WDT<br>0 <sub>B</sub> , Enables watchdog timer<br>1 <sub>B</sub> , Disables the watchdog timer in the decipher                                                                 |
| ERPBK | 3    |       | En_RPBK<br>0 <sub>B</sub> , Disables remote loopback<br>1 <sub>B</sub> , Enables remote loopback                                                                                   |
| DSC   | 2    |       | Dis_Scrm<br>When FX mode is selected, this bit will be forced to one<br>0 <sub>B</sub> , Disables data scrambling<br>1 <sub>B</sub> , Enables data scrambling                      |
| Res   | 1:0  | ro    | <b>Reserved</b>                                                                                                                                                                    |

## Reserved 36

## Registers Description Transceiver Registers

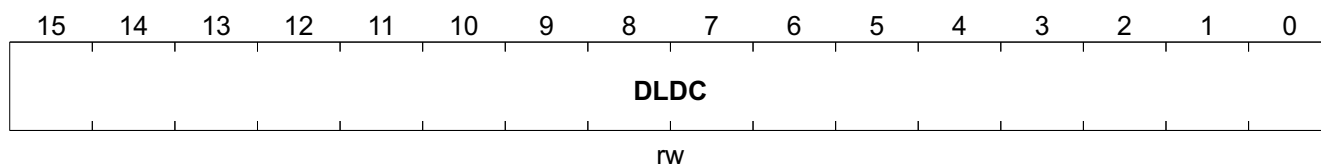
**Res36** **Offset** **Reset Value**  
**Reserved 36** **16<sub>H</sub>** **xxxx<sub>H</sub>**



| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res   | 7:0  | ro   | Reserved    |

## PLL Lock

**PLLL** **Offset** **Reset Value**  
**PLL Lock** **17<sub>H</sub>** **0000<sub>H</sub>**

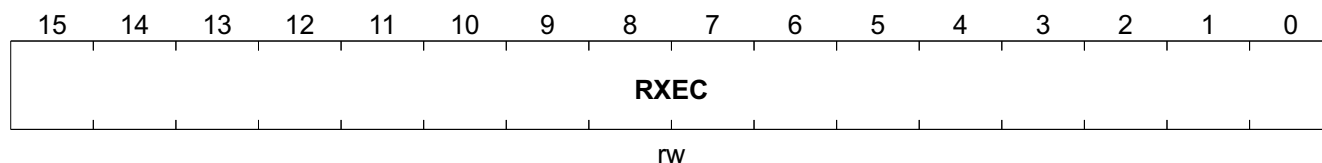


| Field | Bits | Type | Description                                              |
|-------|------|------|----------------------------------------------------------|
| DLDC  | 15:0 | rw   | <b>DLOCK Drop Counter</b><br>Count PLL lock drop events. |

## Registers Description Transceiver Registers

## Receive Error Counter

|                       |                 |                    |
|-----------------------|-----------------|--------------------|
| <b>REC</b>            | <b>Offset</b>   | <b>Reset Value</b> |
| Receive Error Counter | 18 <sub>H</sub> | 0000 <sub>H</sub>  |



| Field | Bits | Type | Description                                            |
|-------|------|------|--------------------------------------------------------|
| RXEC  | 15:0 | rw   | <b>RX Error Counter</b><br>Count receive error events. |

## 5 Electrical Characteristics

### 5.1 Absolute Maximum Ratings

**Table 28 Absolute Maximum Ratings**

| Parameter           | Symbol    | Values |      |      | Unit | Note / Test Condition |
|---------------------|-----------|--------|------|------|------|-----------------------|
|                     |           | Min.   | Typ. | Max. |      |                       |
| Supply Voltage      | $V_{DD}$  | –      | –    | 4.6  | V    | –                     |
| DC Input Voltage    | $V_{IN}$  | –      | –    | 6    | V    | –                     |
| DC Output Voltage   | $V_{OUT}$ | –      | –    | 4.6  | V    | –                     |
| Power Consumption   | $I_{PC}$  | –      | –    | 64   | mA   | Idle state            |
|                     |           | –      | –    | 120  | mA   | 10M Full Duplex Mode  |
|                     |           | –      | –    | 150  | mA   | 100M Full Duplex Mode |
| Storage Temperature | $T_S$     | -65    | –    | 150  | °C   | –                     |
| Ambient Temperature | $T_A$     | -40    | –    | 125  | °C   | –                     |
| ESD robustness      | $V_{ESD}$ | –      | –    | 2000 | V    | –                     |

**Attention:** Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

**Table 29 Operating Condition**

| Parameter      | Symbol   | Values |      |      | Unit | Note / Test Condition |
|----------------|----------|--------|------|------|------|-----------------------|
|                |          | Min.   | Typ. | Max. |      |                       |
| Supply Voltage | $V_{DD}$ | 3.0    | –    | 3.6  | V    | –                     |
| Supply Current | $I_{DD}$ | –      | –    | 150  | mA   | –                     |

### 5.2 DC Characteristics

**Table 30 USB Interface DC Characteristics**

| Parameter                      | Symbol   | Values |      |      | Unit | Note / Test Condition |
|--------------------------------|----------|--------|------|------|------|-----------------------|
|                                |          | Min.   | Typ. | Max. |      |                       |
| Input High Voltage             | $V_{IH}$ | 2.0    | –    | –    | V    | –                     |
| Input Low Voltage              | $V_{IL}$ | –      | –    | 0.8  | V    | –                     |
| Differential Input Sensitivity | $V_{DI}$ | 0.2    | –    | –    | V    | –                     |
| Differential Common Mode Range | $V_{CM}$ | 0.8    | –    | 2.5  | V    | –                     |
| Output Low Voltage             | $V_{OL}$ | 0.0    | –    | 0.3  | V    | –                     |

## Electrical Characteristics

Table 30 USB Interface DC Characteristics (cont'd)

| Parameter                       | Symbol    | Values |      |      | Unit | Note / Test Condition |
|---------------------------------|-----------|--------|------|------|------|-----------------------|
|                                 |           | Min.   | Typ. | Max. |      |                       |
| Output High Voltage             | $V_{OH}$  | 2.8    | –    | 3.6  | V    | –                     |
| Output Signal Crossover Voltage | $V_{CRS}$ | 1.3    | –    | 2.0  | V    | –                     |

Recommended Operating Conditions.

Table 31 EEPROM Interface DC Characteristics

| Parameter             | Symbol   | Values |      |      | Unit | Note / Test Condition                 |
|-----------------------|----------|--------|------|------|------|---------------------------------------|
|                       |          | Min.   | Typ. | Max. |      |                                       |
| Input High Voltage    | $V_{IH}$ | 1.8    | –    | 5.5  | V    | –                                     |
| Input Low Voltage     | $V_{IL}$ | -0.5   | –    | 1.0  | V    | –                                     |
| Input Leakage Current | $I_I$    | ±1     | –    | 1000 | nA   | $V_{IN} = 3.3\text{ V or }0\text{ V}$ |
| Output High Voltage   | $V_{CH}$ | 2.4    | –    | –    | V    | –                                     |
| Output Low Voltage    | $V_{OL}$ | –      | –    | 0.4  | V    | –                                     |
| Input Pin Capacitance | $C_{IN}$ | –      | –    | 5.66 | pF   | –                                     |

Table 32 Home PNA Interface DC Characteristics

| Parameter             | Symbol   | Values |      |      | Unit | Note / Test Condition                 |
|-----------------------|----------|--------|------|------|------|---------------------------------------|
|                       |          | Min.   | Typ. | Max. |      |                                       |
| Input High Voltage    | $V_{IH}$ | 1.8    | –    | 5.5  | V    | –                                     |
| Input Low Voltage     | $V_{IL}$ | -0.5   | –    | 1.0  | V    | –                                     |
| Input Leakage Current | $I_I$    | ±1     | –    | 1000 | nA   | $V_{IN} = 3.3\text{ V or }0\text{ V}$ |
| Output High Voltage   | $V_{OH}$ | 2.4    | –    | –    | V    | –                                     |
| Output Low Voltage    | $V_{OL}$ | –      | –    | 0.4  | V    | –                                     |
| Input Pin Capacitance | $C_{IN}$ | –      | –    | 5.63 | pF   | –                                     |

Table 33 GPIO Interface DC Characteristics

| Parameter             | Symbol   | Values |      |      | Unit | Note / Test Condition                 |
|-----------------------|----------|--------|------|------|------|---------------------------------------|
|                       |          | Min.   | Typ. | Max. |      |                                       |
| Input High Voltage    | $V_{IH}$ | 1.8    | –    | 5.5  | V    | –                                     |
| Input Low Voltage     | $V_{IL}$ | -0.5   | –    | 1.0  | V    | –                                     |
| Input Leakage Current | $I_I$    | ±1     | –    | 1000 | nA   | $V_{IN} = 3.3\text{ V or }0\text{ V}$ |
| Output High Voltage   | $V_{OH}$ | 2.4    | –    | –    | V    | –                                     |
| Output Low Voltage    | $V_{OL}$ | –      | –    | 0.4  | V    | –                                     |
| Input Pin Capacitance | $C_{IN}$ | –      | –    | 5.64 | pF   | –                                     |

### 5.3 Reset Timing

ADM8511/X can be reset either by hardware, software or USB reset.

- A hardware reset is accomplished by asserting the RST# pin after power up the device. It should have a duration of at least 100 ms to ensure the external 48 MHz crystal is in stable and correct frequency. All registers will be reset to default values.

## Electrical Characteristics

- A software reset is accomplished by setting the reset bit (bit 4) of the Ethernet Control Register (address 01<sub>H</sub>). This software reset will reset all registers to default values.
- When ADM8511/X sees an SE0 on USB bus for more than 2.5  $\mu$ s. This USB reset will reset all registers to default values.

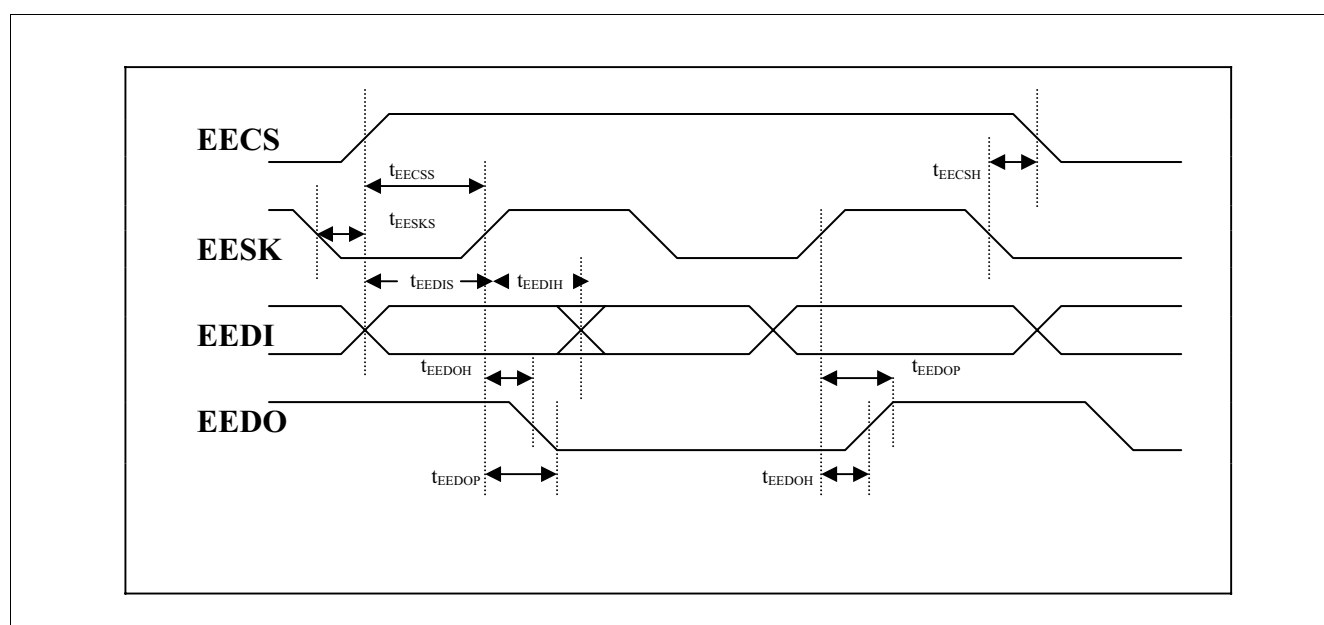
## 5.4 USB Interface Timing

**Table 34 EEPROM Interface Timing**

| Parameter                   | Symbol     | Values |      |        | Unit | Note / Test Condition        |
|-----------------------------|------------|--------|------|--------|------|------------------------------|
|                             |            | Min.   | Typ. | Max.   |      |                              |
| Rise time                   | $T_{FR}$   | 4      | –    | 20     | ns   | $C_L = 50$ pF                |
| Fall time                   | $T_{FF}$   | 4      | –    | 20     | ns   | $C_L = 50$ pF                |
| Rise and fall time matching | $T_{FRFF}$ | 90     | –    | 111.11 | %    | $T_{FRFF} = T_{FR} / T_{FF}$ |

**Table 35 EEPROM Interface Timing**

| Parameter                       | Symbol      | Values |      |      | Unit    | Note / Test Condition |
|---------------------------------|-------------|--------|------|------|---------|-----------------------|
|                                 |             | Min.   | Typ. | Max. |         |                       |
| EESK Clock Frequency            | $t_{EESK}$  | 0      | –    | 1    | MHz     | –                     |
| EECS Setup Time to EESK         | $T_{EECSS}$ | 0.2    | –    | –    | $\mu$ s | –                     |
| EECS Hold Time from EESK        | $T_{EECSH}$ | 0      | –    | –    | ns      | –                     |
| EEDO Hold Time from EESK        | $T_{EEDOH}$ | 70     | –    | –    | ns      | –                     |
| EEDO Output Delay to “1” or “0” | $T_{EEDOP}$ | –      | –    | 2    | $\mu$ s | –                     |
| EEDI Setup Time to EESK         | $t_{EEDIS}$ | 0.4    | –    | –    | $\mu$ s | –                     |
| EEDI Hold Time from EESK        | $t_{EEDIH}$ | 0.4    | –    | –    | $\mu$ s | –                     |

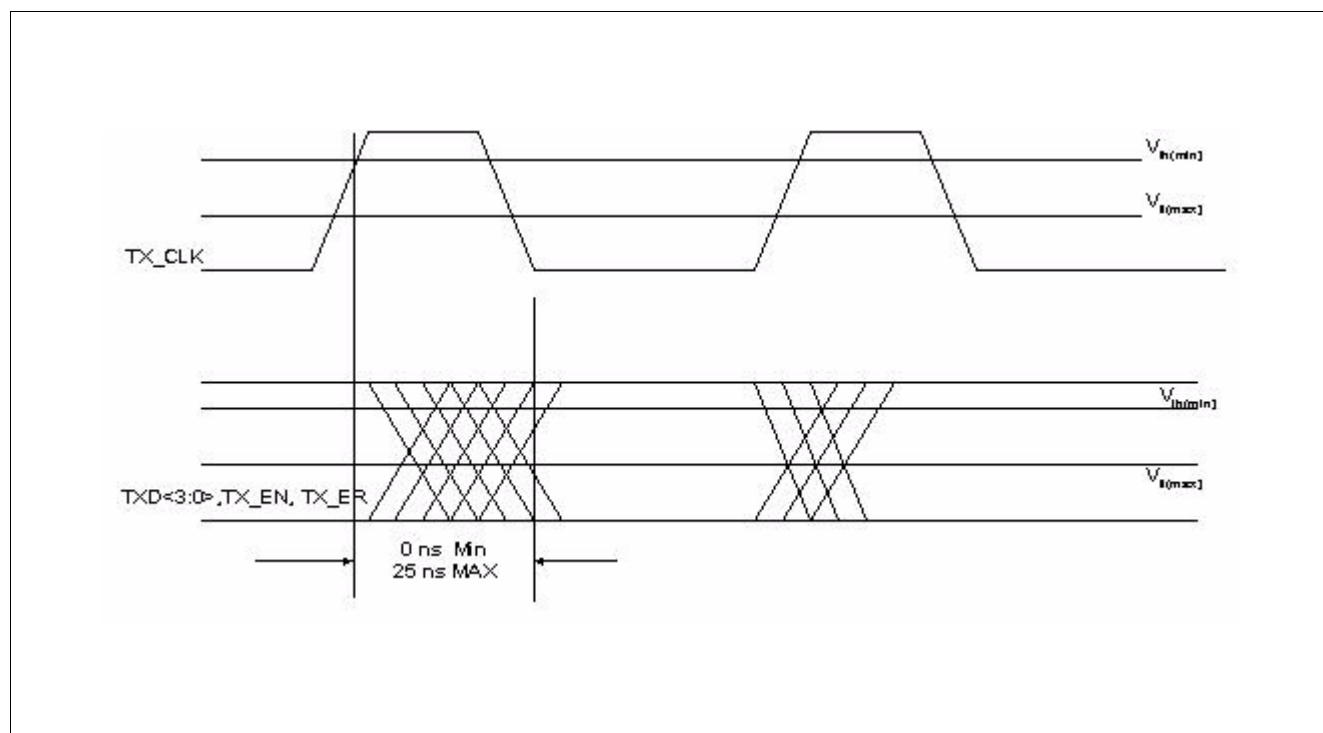


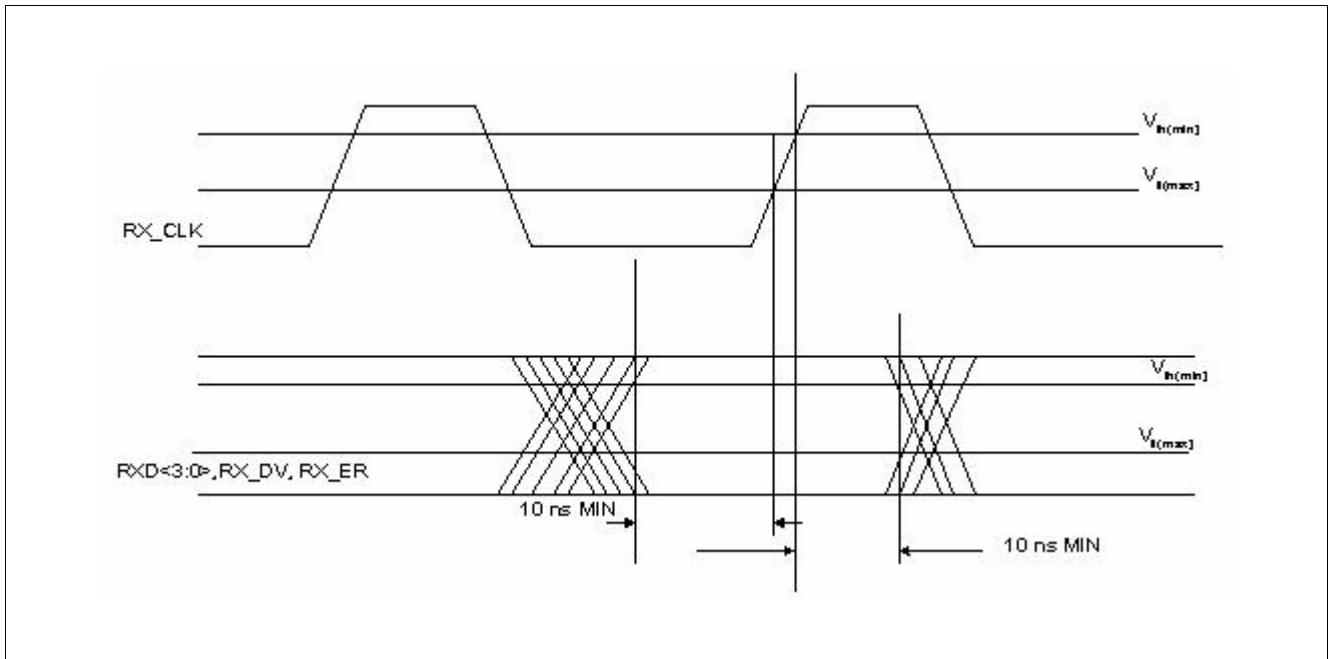
**Figure 3 EEPROM Interface Timings**

## 5.5 Home PNA Interface Timing

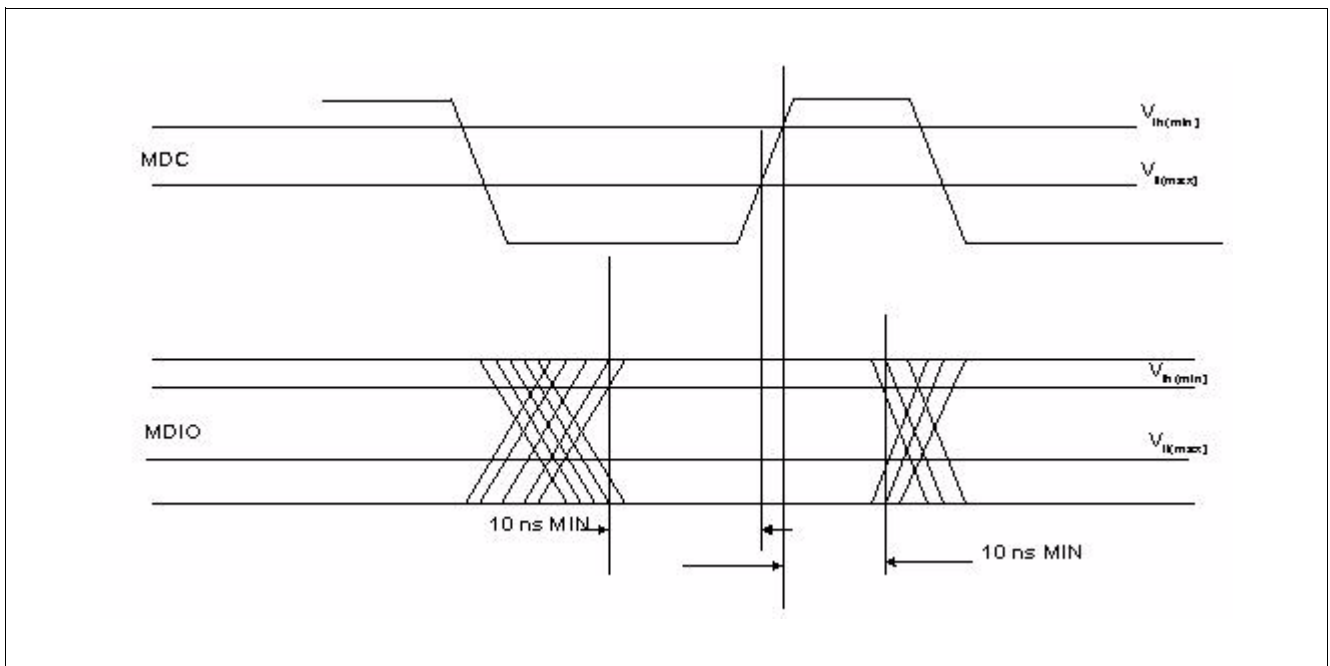
**Table 36 Home PNA Interface Timing**

| Parameter                                             | Symbol | Values  |      |         | Unit | Note / Test Condition |
|-------------------------------------------------------|--------|---------|------|---------|------|-----------------------|
|                                                       |        | Min.    | Typ. | Max.    |      |                       |
| HPN_TXCLK during MAC preamble and delimiter           |        | 100e-9  | –    | 100e-6  | s    | –                     |
| HPN_TXCLK during Ethernet packet                      |        | 100e-9  | –    | 10e-6   | s    | –                     |
| HPN_RXCLK during MAC preamble and delimiter           |        | 100e-9  | –    | 100e-6  | s    | –                     |
| HPN_RXCLK during Ethernet packet                      |        | 100e-9  | –    | 10e-6   | s    | –                     |
| HPN_TXCLK and HPN_RXCLK during 96-bit inter-frame gap |        | 233.334 | –    | 233.334 | ns   | –                     |
| HPN_TXCLK and HPN_RXCLK during idle                   |        | 583.335 | –    | 583.335 | ns   | –                     |

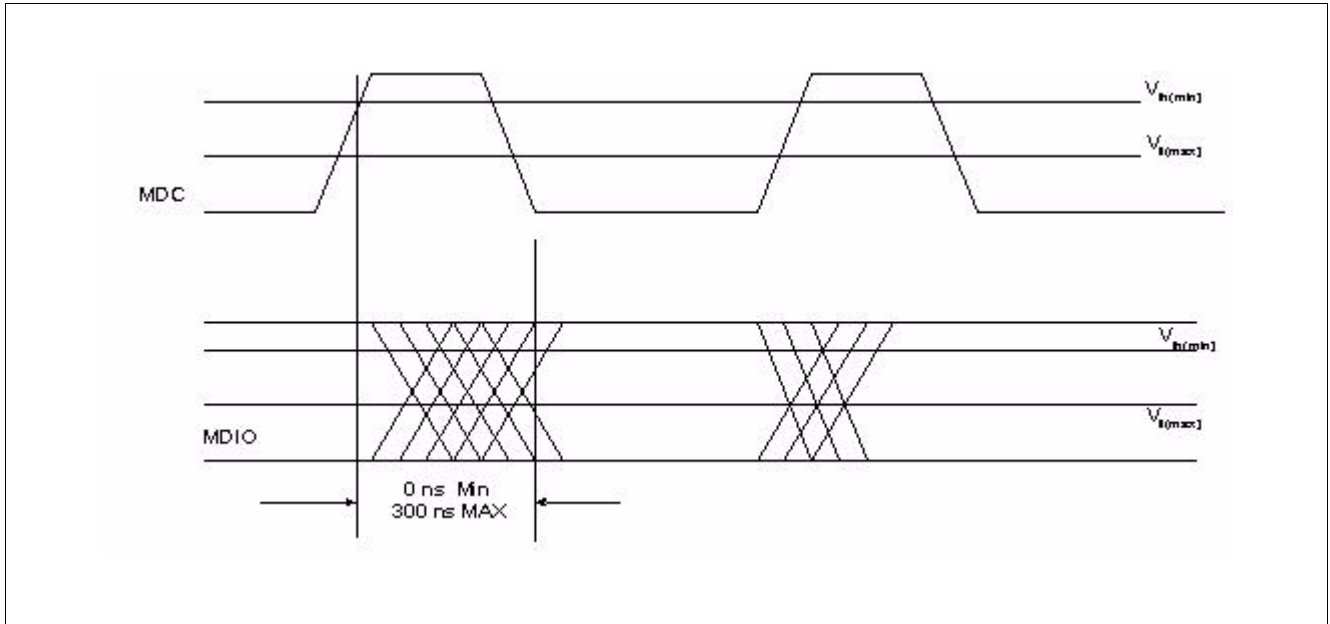

**Figure 4 Transmit Signal Timing Relationships at the MII**



**Figure 5** Receive Signal Timing Relations at the MII



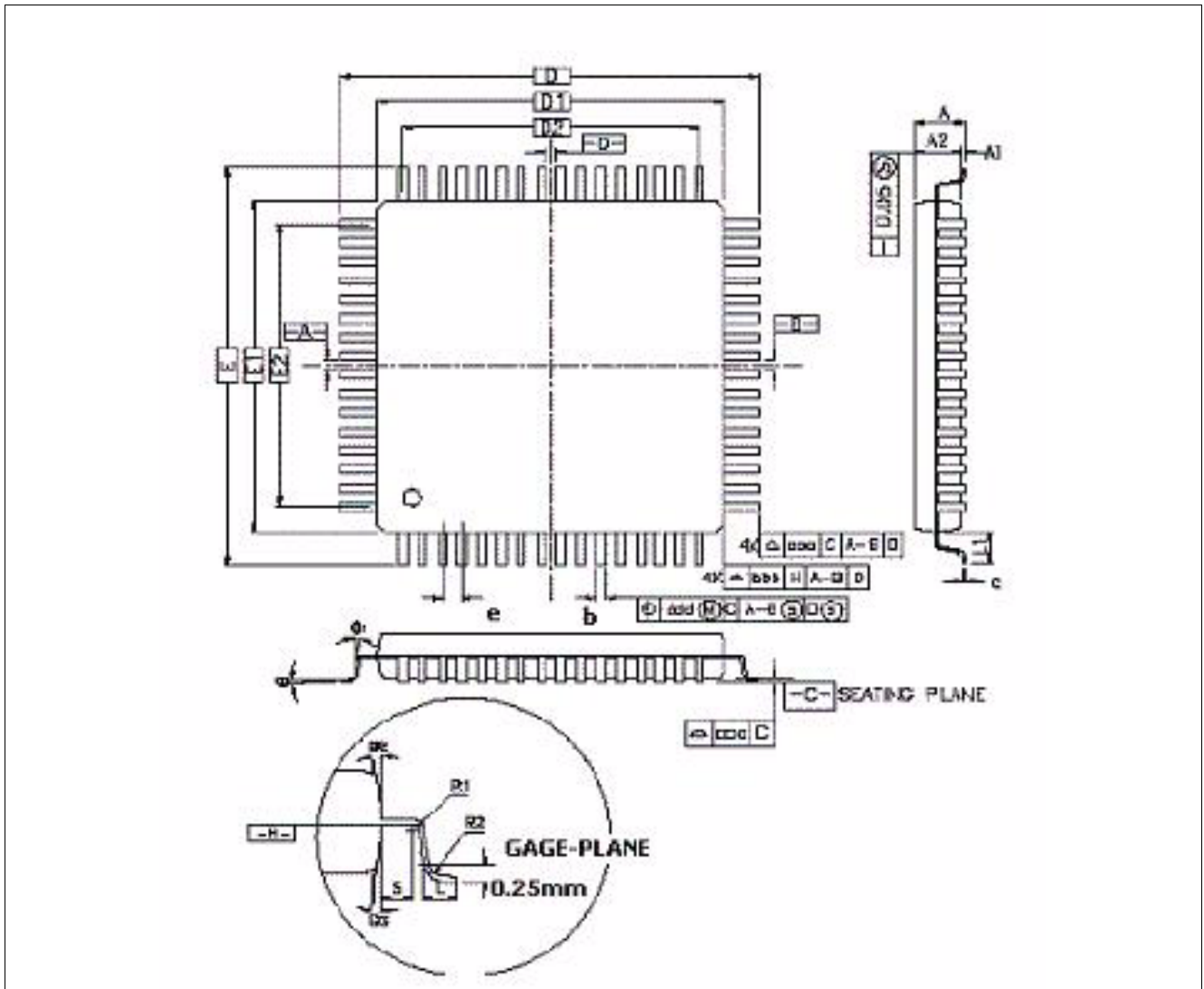
**Figure 6** MDIO Sourced by STA



**Figure 7 MDIO Sourced by PHY**

## 6 Packaging

Package Outline of ADM8511/X, P-LQFP-100



**Figure 8** P-LQFP-100-1 (Plastic Low Profile Quad Flat Package)

Note: Dimensions in mm

**Table 37 Dimensions for 100 Pin LQFP Package**

| Symbol                         | Millimeter (mm) |      |      | Inch       |       |       |
|--------------------------------|-----------------|------|------|------------|-------|-------|
|                                | Min.            | Typ. | Max. | Min.       | Typ.  | Max.  |
| A                              | —               | —    | 1.60 | —          | —     | 0.063 |
| A <sub>1</sub>                 | 0.05            | —    | 0.15 | 0.002      | —     | 0.006 |
| A <sub>2</sub>                 | 1.35            | 1.40 | 1.45 | 0.053      | 0.005 | 0.057 |
| D                              | 16.00 BSC.      |      |      | 0.630 BSC. |       |       |
| D <sub>1</sub>                 | 14.00 BSC       |      |      | 0.551 BSC. |       |       |
| E                              | 16.00 BSC       |      |      | 0.630 BSC. |       |       |
| E <sub>1</sub>                 | 14.00 BSC       |      |      | 0.551 BSC. |       |       |
| R <sub>2</sub>                 | 0.08            | —    | 0.20 | 0.003      | —     | 0.008 |
| R <sub>1</sub>                 | 0.08            | —    | —    | 0.003      | —     | —     |
| Θ                              | 0°              | 3.5° | 7°   | 0°         | 3.5°  | 7°    |
| Θ <sub>1</sub>                 | 0°              | —    | —    | 0°         | —     | —     |
| Θ <sub>2</sub>                 | 11°             | 12°  | 13°  | 11°        | 12°   | 13°   |
| Θ <sub>3</sub>                 | 11°             | 12°  | 13°  | 11°        | 12°   | 13°   |
| c                              | 0.09            | —    | 0.20 | 0.004      | —     | 0.008 |
| L                              | 0.45            | 0.60 | 0.75 | 0.018      | 0.024 | 0.030 |
| L <sub>1</sub>                 | 1.00 Ref.       |      |      | 0.039 Ref. |       |       |
| S                              | 0.20            | —    | —    | 0.008      | —     | —     |
| b                              | 0.17            | 0.20 | 0.27 | 0.007      | 0.008 | 0.011 |
| e                              | 0.50 BSC.       |      |      | 0.020 BSC. |       |       |
| D <sub>2</sub>                 | 12.00           |      |      | 0.472      |       |       |
| E <sub>2</sub>                 | 12.00           |      |      | 0.472      |       |       |
| Tolerance of Form and Position |                 |      |      |            |       |       |
| aaa                            | 0.20            |      |      | 0.008      |       |       |
| bbb                            | 0.20            |      |      | 0.008      |       |       |
| ccc                            | 0.08            |      |      | 0.003      |       |       |
| ddd                            | 0.08            |      |      | 0.003      |       |       |

Note:

1. Dimensions D<sub>1</sub> and E<sub>1</sub> do not include mold protrusion. Allowable protrusion is 0.25 mm per. Side D<sub>1</sub> and E<sub>1</sub> are Maximum plastic body size dimensions including mold mismatch.
2. Dimensions b does not include dambar protrusion shall not cause the lead width to exceed the maximum b dimensions by more than 0.08 mm. Dambar can not be located on the lower radius or the foot. Maximum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.

## 7 APPENDIX 1 - Layout Guide

### 7.1 Placement

1. On USB side, Place PegasusII and USB connector as close as possible.
2. On Ethernet side, place PegasusII, transformer and RJ45 as close as possible.
3. The crystal or OSC device should be close to PegasusII and away from the following items:
  - a) Any analog signal
  - b) PCB edge
  - c) Any other high frequency components and their associated traces.
4. Place the filtering capacitor as close as possible at the power pin of ADM 8511 (Pegasus II) and its trace is short and wide.

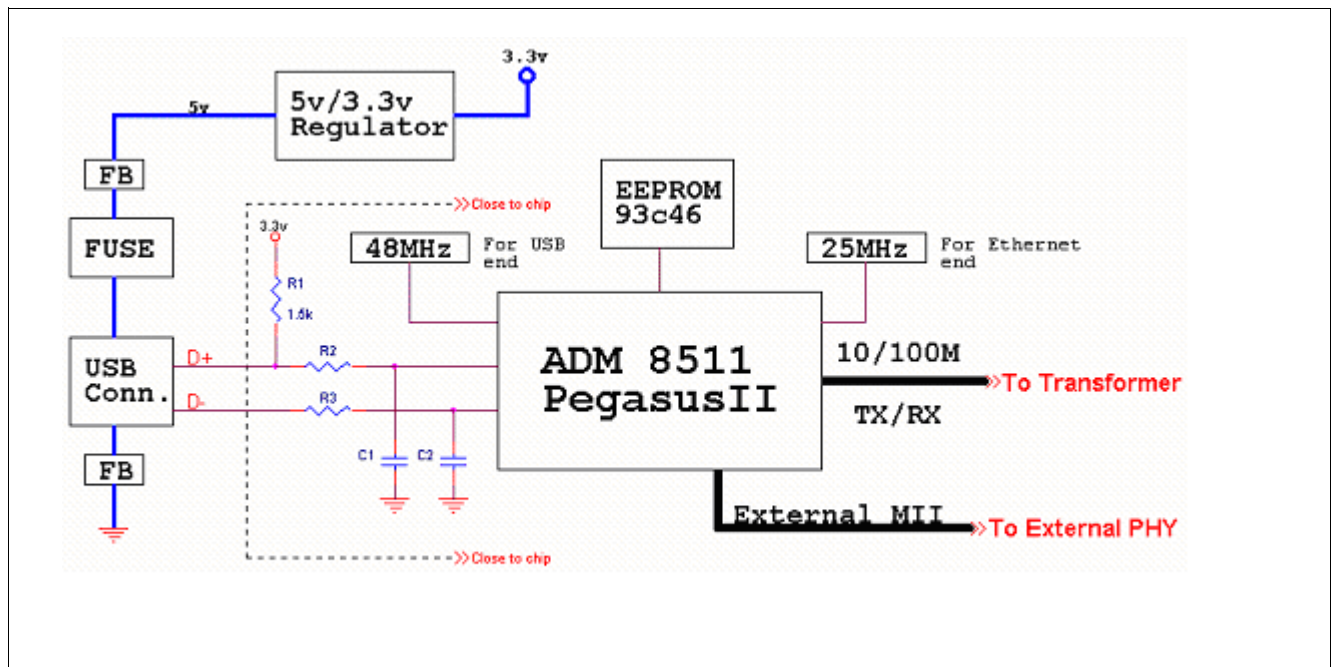
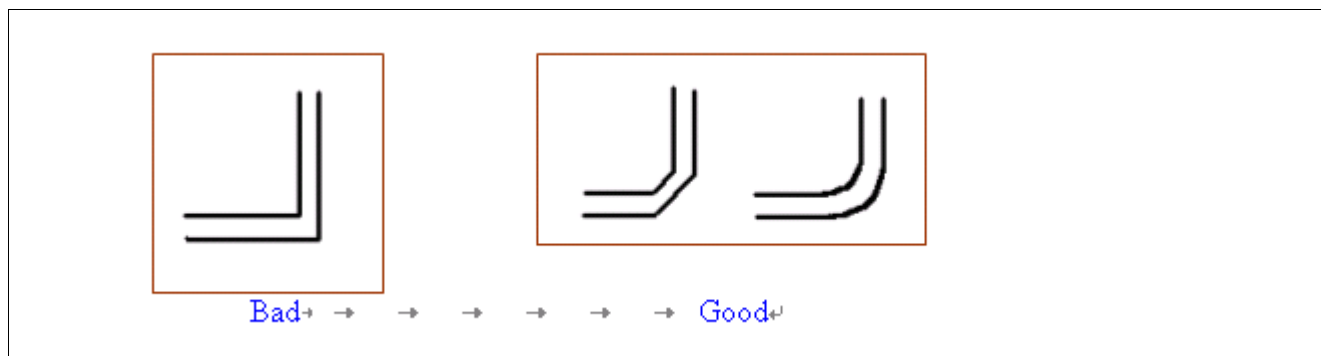


Figure 9 Correct placement

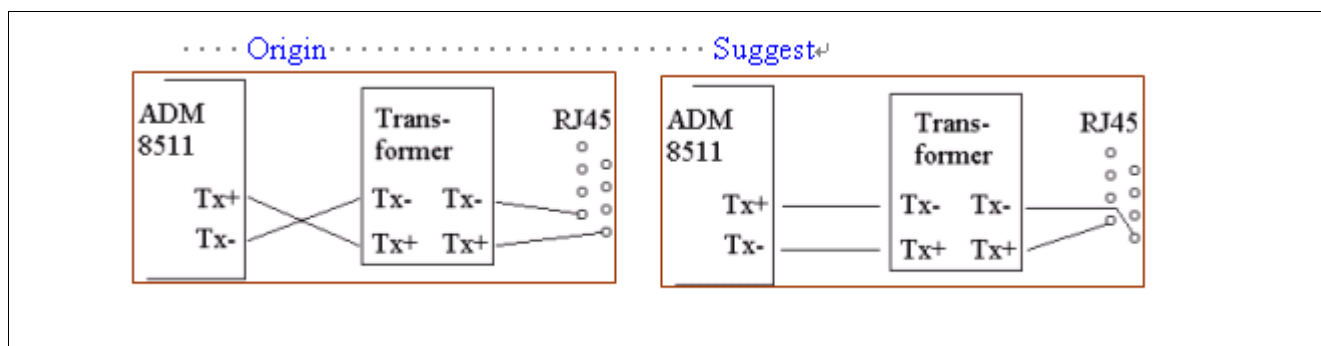
### 7.2 Trace routing

- Keep USB differential pair data signal D+ and D-:
  - Trace width should be as wide as possible.
  - Make D+ and D- traces route at the same signal plane and doesn't pass through other plane.
  - Inhibit crossover on D+ and D-
  - The termination resistance (R2,R3) and decoupling capacitors (C1,C2) should be close to ADM8511/X.
  - D+ and D- Signal trace length should be equal and as short as possible
- Arrangement Tx and Rx trace
  - Tx+/- and Rx+/- trace avoid right angle and round angle >90 degree; suggested.



**Figure 10** Trace routing

- Trace width must be wide and should be wider than 8 miles.
  - Signal trace length between Tx+/- differential pairs should be cross and have equal length. The total length should be no longer than 2 cm. The same requirement also apply to Rx+/-.
  - Make Tx and Rx trace route at the same signal plane and doesn't pass through other plane.
  - Every differential pairs as cross as possible, but no less than 8 miles and space should be almost equal
  - Keep space large between Tx and Rx differential pairs, even separated ground planes underneath Tx and Rx signal pairs
  - Away from clock and power traces.
  - If Tx routed trace must cross, the trace can be swapped between chip and transformer, and transformer to RJ45, too.



**Figure 11** Crossed Tx routed trace

- Digital signal should be away from analog signal and power traces. If this can't be avoided, analog and VCC should cross over 90 degree at other plane.
- Vcc trace should short and prefer to route in this plane format, special for GND.

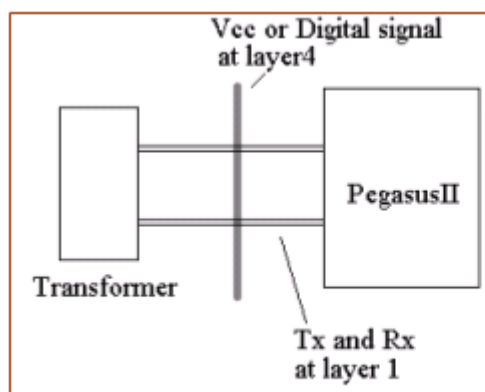


Figure 12 Vcc trace

### 7.3 Power and Ground

- Every power pin should have 0.1uF SMD capacitors placed with it. To be effective, the capacitors should be placed as close as possible at the pin.
- The chassis ground plane connected to the USB B type and network connector chassis should be isolated from the signal plane with 0.1uF capacitors or bead to prevent any radiation from leaking and resulting in FCC failure.
- Right angle is recommend when partition Vcc as well as GND planes.
- Avoid power and ground planes placing directly under the transformer. See [Figure 13](#).

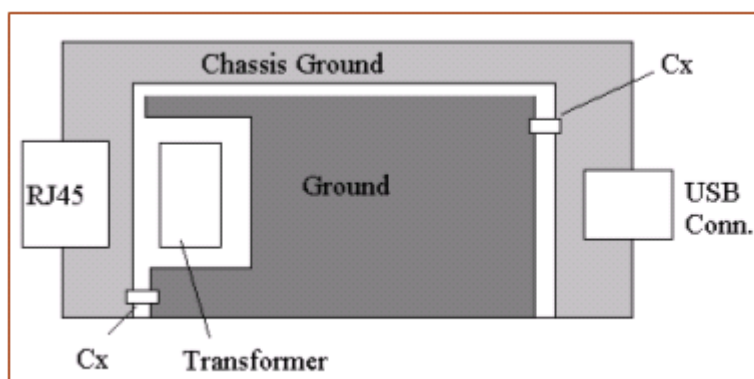
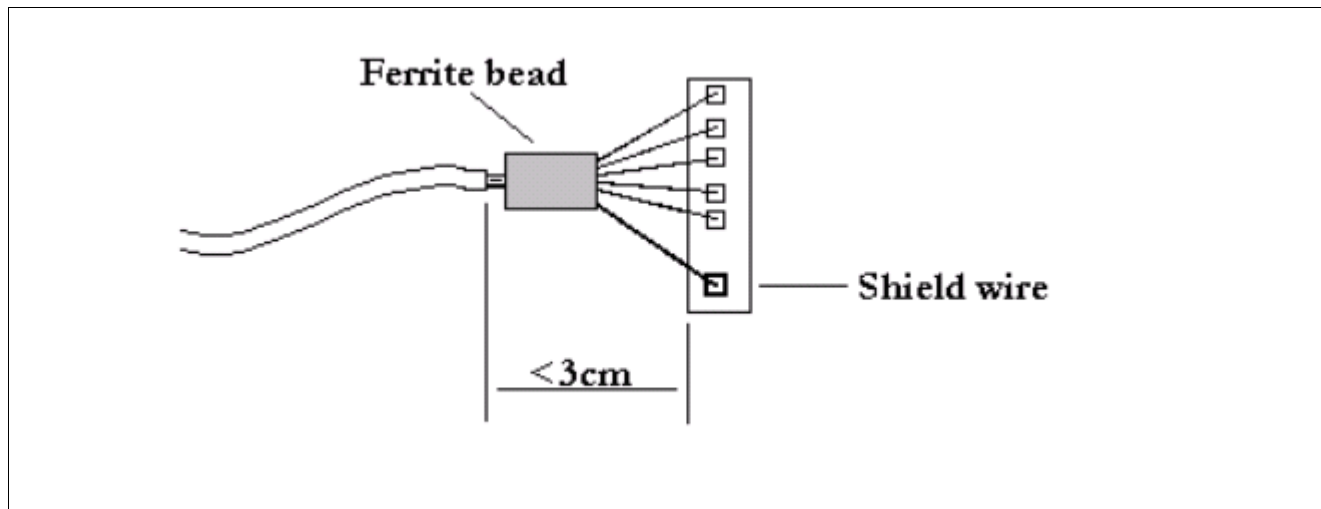


Figure 13 Correct placement of power and ground planes

- If you use a permanently attached cable (plus the shield wire).it may require additional filtering for FCC test pass.and the length of unshielded cable should be limited to 3cm or less.



**Figure 14** Limited length of unshielded cable

- Please connect pin12(GndRef) and pin8(GndR) first then use signal via to Gnd.



**Figure 15** Connection of pin12(GndRef) and pin8(GndR)

## 8 APPENDIX 2 - EEPROM Interface & Example

### 8.1 General EEPROM Format Description

If the EEPROM contents from offset 0 to offset 5 is "FF\_FF\_FF\_FF\_FF\_FF", it means the EEPROM isn't programmed correctly, The default values for every field are used instead of loading from EEPROM.

**Table 38 General EEPROM Format Description**

| Offset(byte) | Field                           | Description                                                                                                                                                        |
|--------------|---------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 00           | node_id0                        | The 1st byte of Ethernet node ID.                                                                                                                                  |
| 01           | node_id1                        | The 2nd byte of Ethernet node ID.                                                                                                                                  |
| 02           | node_id2                        | The 3rd byte of Ethernet node ID.                                                                                                                                  |
| 03           | node_id3                        | The 4th byte of Ethernet node ID.                                                                                                                                  |
| 04           | node_id4                        | The 5th byte of Ethernet node ID.                                                                                                                                  |
| 05           | node_id5                        | The 6th byte of Ethernet node ID.                                                                                                                                  |
| 06-07        | reserved                        |                                                                                                                                                                    |
| 08           | max_pwr                         | The maximum USB power consumption.                                                                                                                                 |
| 09           | ep3_interval                    | The polling interval for endpoint 3. If this value is 0, EP3 is disabled.                                                                                          |
| 0A[0]        | iso_enable                      | 0                                                                                                                                                                  |
| 0A[1]        | USB<br>transceiver<br>Test_mode | 0: select external USB transceiver.<br>1: select internal USB transceiver.                                                                                         |
| 0A[4:2]      | MII Test_mode                   | 000b: tri-state MII pins<br>001b: enable MAC's MII signals to external interface<br>010b: enable PHY's MII signals to external interface<br>011b: monitor MII mode |
| 0A[7]        | Remote<br>wake-up<br>Enable     | 0: Enable<br>1: Disable                                                                                                                                            |
| 0B[7:6]      | LED mode                        | Refer to pin assignment                                                                                                                                            |
| 0B[5:0]      | reserved                        |                                                                                                                                                                    |
| 0C           | languageid_lo                   | The low byte of language ID.                                                                                                                                       |
| 0D           | languageid_hi                   | The high byte of language ID.                                                                                                                                      |
| 0E-0F        | reserved                        |                                                                                                                                                                    |
| 10           | manuid_lo                       | The low byte of manufacture ID.                                                                                                                                    |
| 11           | manuid_hi                       | The high byte of manufacture ID.                                                                                                                                   |
| 12           | proid_lo                        | The low byte of product ID.                                                                                                                                        |
| 13           | proid_hi                        | The high byte of product ID.                                                                                                                                       |
| 14           | manu_str_len                    | The length for manufacture string.                                                                                                                                 |
| 15           | manu_str_offset                 | The word offset address of manufacture string.                                                                                                                     |
| 16           | pro_str_len                     | The length for product string.                                                                                                                                     |
| 17           | pro_str_offset                  | The word offset address of product string.                                                                                                                         |

## APPENDIX 2 - EEPROM Interface & Example

**Table 38 General EEPROM Format Description (cont'd)**

| Offset(byte) | Field           | Description                                      |
|--------------|-----------------|--------------------------------------------------|
| 18           | seri_str_len    | The length for serial number string              |
| 19           | seri_str_offset | The word offset address of serial number string. |

## 8.2 Example

**Table 39 Example 1**

| offset(byte) | value                    |
|--------------|--------------------------|
| 0000h        | 00, 00 E8 00 02 2C 00 00 |
| 0008h        | 50 01 02 00 09 04 00 00  |
| 0010h        | A6 07 11 85 0E 10 2A 20  |
| 0018         | 0A 38 00 00 00 00 00 00  |
| 0020         | 0E 03 41 00 44 00 4D 00  |
| 0028         | 74 00 65 00 6B 00 00 00  |
| 0030         | 1E 00 55 00 53 00 42 00  |
| 0038         | 20 00 31 00 30 00 2F 00  |
| 0040         | 2A 03 55 00 53 00 42 00  |
| 0048         | 20 00 54 00 6F 00 20 00  |
| 0050         | 4C 00 41 00 4E 00 20 00  |
| 0058         | 43 00 6F 00 6E 00 76 00  |
| 0060         | 65 00 72 00 74 00 65 00  |
| 0068         | 72 00 00 00 00 00 00 00  |
| 0070         | 0A 03 30 00 30 00 30 00  |
| 0078         | 31 00 00 00 00 00 00 00  |

**Table 40 Example 2**

| Offset(byte) | Value                 | Description                                                                                                      |
|--------------|-----------------------|------------------------------------------------------------------------------------------------------------------|
| 00-05        | 00_00_E8_10<br>_46_02 | NIC node ID                                                                                                      |
| 08           | 50                    | maximum power 160mA                                                                                              |
| 09           | 01                    | interrupt endpoint 3 polling interval 1ms                                                                        |
| 0A           | 02                    | isochronous endpoint disable, select internal USB transceiver<br>Use internal Ethernet PHY<br>Wake on Lan enable |
| 0C-0D        | 0904                  | Language ID 0409                                                                                                 |
| 10-11        | A607                  | manufacture ID 07A6                                                                                              |
| 12-13        | 8511                  | product ID 8511                                                                                                  |
| 14           | 0E                    | manufacture string length 0E bytes                                                                               |
| 15           | 10                    | manufacture string starts from word offset 10h, thus byte offset 20h.                                            |
| 16           | 1E                    | product string length 1E bytes                                                                                   |

## APPENDIX 2 - EEPROM Interface & Example

**Table 40 Example 2**

| Offset(byte) | Value                                           | Description                                                                              |
|--------------|-------------------------------------------------|------------------------------------------------------------------------------------------|
| 17           | 18                                              | product string starts from word offset 18h, thus byte offset 30h.                        |
| 18           | 0A                                              | serial number string length 0A bytes                                                     |
| 19           | 38                                              | serial number string starts from word offset 38h, thus byte offset 70h.                  |
| 20-2E        | 0E 03 41 00 44<br>00 4D 00 74 00<br>65 00 6B 00 | 0E:descriptor size 14 bytes<br>03: string descriptor<br>41.....: UNICODE encoded string  |
| 30-4E        | 1E 03 55 00 53<br>00 42 00<br>20<br>00.....     | 1E:descriptor size 30 bytes<br>03: string descriptor<br>55.....: UNICODE encoded string  |
| 50-5A        | 0A 03 30 00 30<br>00 30 00<br>31 00             | 0A: descriptor size 10 bytes<br>03: string descriptor<br>30.....: UNICODE encoded string |

## 9 APPENDIX 3 - USB Device Operation

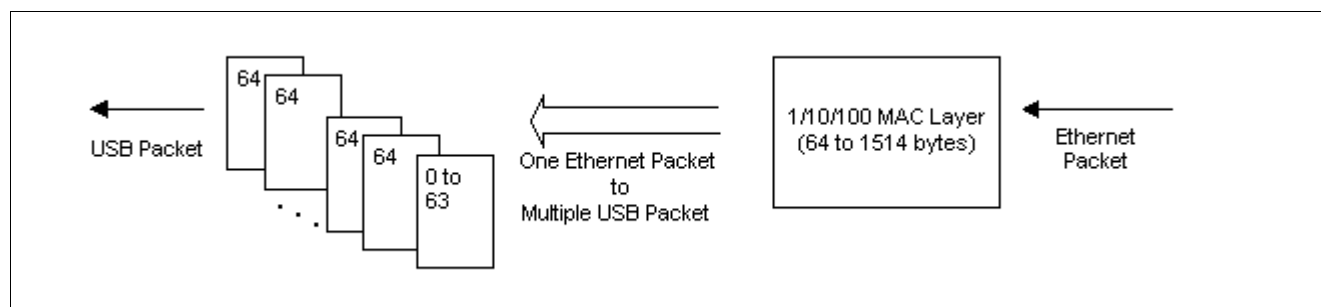
### 9.1 Endpoint 0

Endpoint 0 is in charge of response to standard USB commands and vendor specific commands. Internal registers setting are also via this endpoint. The response to each command is described in section 7.

### 9.2 Endpoint 1 bulk IN

Endpoint 1 is in charge of sending the received Ethernet packet to USB host. An Ethernet packet will be split to multiple 64-byte USB packets on USB. The end of the Ethernet packet is indicated by less than 64-byte or 0 length data transfer in this pipe. The Ethernet received status is optionally reported at the end of the packet.

While accessing to this endpoint if RX FIFO is either full or any packet is inside, the data in RX FIFO is returned in USB data stage. If ACK is received from USB host, data in RX FIFO is flushed. If no response or NAK is received from USB host, the content in RX FIFO will be re-transmitted. If RX FIFO isn't ready for transmission, NAK is returned to USB host.



**Figure 16** Transmission of RX FIFO

The received status is reported as follows:

**Table 41** Received status

| Offset  | Bit | Field           | Description                                              |
|---------|-----|-----------------|----------------------------------------------------------|
| Offset0 | 7-0 | rx_bytecnt_lo   | The received byte count[7:0].                            |
| Offset1 | 3-0 | rx_bytecnt_hi   | The received byte count[11:8].                           |
|         | 7-4 | reserved        |                                                          |
| Offset2 | 0   | Multicast_frame | Indicate receive a multicast frame.                      |
|         | 1   | Long_pkt        | Indicate received packet length > 1518 bytes             |
|         | 2   | Runt_pkt        | Indicate received packet length < 64 bytes.              |
|         | 3   | crc_err         | Indicate CRC check error.                                |
|         | 4   | Dribble_bit     | Indicate packet length is not integer multiple of 8-bit. |
|         | 7-5 | reserved        |                                                          |
| Offset3 | 7-0 | reserved        |                                                          |

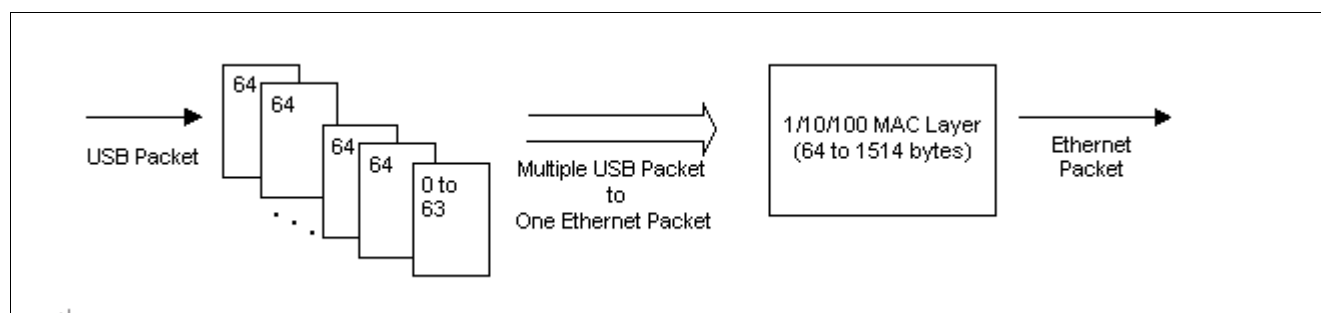
### 9.3 Endpoint 2 bulk OUT

Endpoint 2 is in charge of sending the USB packet to Ethernet. An Ethernet packet is concatenated as multiple 64-byte USB packets on USB. The first two bytes in every first concatenated USB packet indicate the total length of the Ethernet packet. The end of the Ethernet packet is indicated with less than 64-byte or 0 length data transfer in this pipe. The Ethernet transmit status is reported in transmit status register.

When access to this endpoint, data in USB data stage is transferred to TX FIFO when TX FIFO is free and ACK is returned. If TX FIFO isn't free, NAK is returned.

**Table 42 Endpoint 2 bulk OUT**

| Field   | 1st byte in 1st USB packet                | 2nd byte in 1st USB packet | The following packets |
|---------|-------------------------------------------|----------------------------|-----------------------|
| Content | len[7:0]: Low byte Ethernet packet length | {reserved[4:0], len[10:8]} | Ethernet packet       |



**Figure 17 Sending the USB packet to Ethernet**

### 9.4 Endpoint 3 interrupt IN

Endpoint 3 is in charge of returning the current Ethernet transfer status every polling interval. When access to this endpoint, 8 bytes data is returned to USB host. The 8-byte packet contains

**Table 43 Endpoint 3 interrupt IN**

| Offset0            | Offset1            | Offset2            | Offset3             | Offset4             | Offset5                | Offset6-7 (2B) |
|--------------------|--------------------|--------------------|---------------------|---------------------|------------------------|----------------|
| tx_status(Reg 2Bh) | tx_status(Reg 2Ch) | rx_status(Reg 2Dh) | rx_lostpkt(Reg 2Eh) | rx_lostpkt(Reg 2Fh) | Wakeup_status(Reg 7Ah) | 0              |

## 10 APPENDIX 4 - USB Command

- Get\_Register (Vendor Specific) Single/Burst read

**Table 44 Setup Stage**

| bmReq | bReq | wValue(2B) | wIndex(2B)          | wLength(2B) |
|-------|------|------------|---------------------|-------------|
| C0    | F0   | 0          | {RegIndex[0:7], 00} | length      |

**Table 45 Data Stage**

| Offset0(1B) | Offset1(1B)  | Offset2(1B)  |
|-------------|--------------|--------------|
| {RegIndex}  | {RegIndex+1} | {RegIndex+2} |

The returned total number of registers depends on the length field.

- Set\_Register (Vendor Specific) Single write

**Table 46 Setup Stage**

| bmReq | bReq | wValue(2B)             | wIndex(2B)          | wLength(2B) |
|-------|------|------------------------|---------------------|-------------|
| 40    | F1   | {value[0:7],mask[0:7]} | {RegIndex[0:7], 00} | 1           |

- Set\_Register(Vendor Specific) Burst write

**Table 47 Setup Stage**

| bmReq | bReq | wValue(2B) | wIndex(2B)          | wLength(2B) |
|-------|------|------------|---------------------|-------------|
| 40    | F1   | 0          | {RegIndex[0:7], 00} | length      |

**Table 48 Data Stage**

| Offset0(1B) | Offset1(1B)  | Offset2(1B)  | Offset3(1B)  |
|-------------|--------------|--------------|--------------|
| {RegIndex}  | {RegIndex+1} | {RegIndex+2} | {RegIndex+3} |

Ex. Write 44 to RegIndex=05h, the transfer will be

**Table 49 Setup Stage**

| bmReq | bReq | wValue(2B) | wIndex(2B) | wLength(2B) |
|-------|------|------------|------------|-------------|
| 40    | FE   | 4400       | 0500       | 0100        |

If wLength > 1, more than 1 register is accessed (burst write) and mask is not supported => DataStage for 8-byte OUT transfer appears

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Ex. Burst write 20 registers from RegIndex=07h and data from 01d to 20d

**Table 50 Setup Stage**

| bmReq | bReq | wValue(2B) | wIndex(2B) | wLength(2B) |
|-------|------|------------|------------|-------------|
| 40    | FE   | 0000       | 0700       | 1400        |

**Table 51 Data Stage - 1st OUT transfer**

| Offset0(1B) | Offset1(1B) | Offset2(1B) | Offset3(1B) | Offset4(1B) | Offset5(1B) | Offset6(1B) | Offset7(1B) |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 01          | 02          | 03          | 04          | 05          | 06          | 07          | 08          |

**Table 52 Data Stage - 2nd OUT transfer**

| Offset0(1B) | Offset1(1B) | Offset2(1B) | Offset3(1B) | Offset4(1B) | Offset5(1B) | Offset6(1B) | Offset7(1B) |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 09          | 02          | 0A          | 0B          | 0C          | 0D          | 0E          | 10          |

**Table 53 Data Stage - 3rd OUT transfer**

| Offset0(1B) | Offset1(1B) | Offset2(1B) |
|-------------|-------------|-------------|
| 11          | 12          | 13          |

- Get\_Status(Device)

**Table 54 Setup Stage**

| bmReq | bReq | wValue(2B) | wIndex(2B) | wLength(2B) |
|-------|------|------------|------------|-------------|
| 80    | 0    | 0          | 0          | 2           |

**Table 55 Data Stage**

| D[15:2] | D[1]: Remote Wakeup       | D[0]:Self Powered |
|---------|---------------------------|-------------------|
| 0       | Register of remote_wakeup | 1                 |

- Get\_Status(Interface)

**Table 56 Setup Stage**

| bmReq | bReq | wValue(2B) | wIndex(2B) | wLength(2B) |
|-------|------|------------|------------|-------------|
| 81    | 0    | 0          | 0          | 2           |

**Table 57 Data Stage**

| D[15:0] |
|---------|
| 0       |

## APPENDIX 4 - USB Command

- Get\_Status(EP0)

**Table 58 Setup Stage**

| bmReq | bReq | wValue(2B) | wIndex(2B)   | wLength(2B) |
|-------|------|------------|--------------|-------------|
| 82    | 0    | 0          | 0080 or 0000 | 2           |

**Table 59 Data Stage**

| D[15:1] | D[0]: Halt           |
|---------|----------------------|
| 0       | register of ep0_halt |

- Get\_Status(EP1) bulk IN

**Table 60 Setup Stage**

| bmReq | bReq | wValue(2B) | wIndex(2B) | wLength(2B) |
|-------|------|------------|------------|-------------|
| 82    | 0    | 0          | 0081       | 2           |

**Table 61 Data Stage**

| D[15:1] | D[0]: Halt           |
|---------|----------------------|
| 0       | register of ep1_halt |

- Get\_Status(EP2) bulk OUT

**Table 62 Setup Stage**

| bmReq | bReq | wValue(2B) | wIndex(2B) | wLength(2B) |
|-------|------|------------|------------|-------------|
| 82    | 0    | 0          | 0002       | 2           |

**Table 63 Data Stage**

| D[15:1] | D[0]: Halt           |
|---------|----------------------|
| 0       | register of ep2_halt |

- Get\_Status(EP3) interrupt IN

**Table 64 Setup Stage**

| bmReq | bReq | wValue(2B) | wIndex(2B) | wLength(2B) |
|-------|------|------------|------------|-------------|
| 82    | 0    | 0          | 0083       | 2           |

**Table 65 Data Stage**

| D[15:1] | D[0]: Halt           |
|---------|----------------------|
| 0       | register of ep3_halt |

## APPENDIX 4 - USB Command

- Get\_Descriptor(Device) total 18-byte

**Table 66 Setup Stage**

| bmReq | bReq | wValue(2B) | wIndex(2B) | wLength(2B) |
|-------|------|------------|------------|-------------|
| 80    | 6    | 0001       | 0          | length      |

**Table 67 Data Stage: wLength field specifies the total byte count to return (1)**

| Offset0 | Offset1(type) | Offset2(USB release no.) | Offset4(Class code) | Offset5(Sub Class Code) | Offset6(Protocol) | Offset7(EP0 MaxPktSize) | Offset8 (vendor ID) |
|---------|---------------|--------------------------|---------------------|-------------------------|-------------------|-------------------------|---------------------|
| 12(1B)  | 01(1B)        | 0110(2B)                 | 00(1B)              | 00(1B)                  | 00(1B)            | 8(1B)                   | (2B)                |

**Table 68 Data Stage: wLength field specifies the total byte count to return (2)**

| Offset10 (productID) | Offset12(releaseID) | Offset14 (manufacture) | Offset15 (Product) | Offset16(serial no.) | Offset17(no. of config) |
|----------------------|---------------------|------------------------|--------------------|----------------------|-------------------------|
| (2B)                 | 0001(2B)            | 01(1B)                 | 02(1B)             | 03(1B)               | 01(1B)                  |

- Get\_Descriptor(Configuration) total 39-byte

**Table 69 Setup Stage**

| bmReq | bReq | wValue(2B) | wIndex(2B) | wLength(2B) |
|-------|------|------------|------------|-------------|
| 80    | 6    | 0002       | 0          | length      |

**Table 70 Setup Stage - Configuration Descriptor**

| Offset 0 (Length) | Offset1 (DscrType) | Offset2 (TotalLength) | Offset4 (NumInterface) | Offset5 (CfgValu e) | Offset6 (StringIndex) | Offset7 (Attribute) | Offset8 (MaxPower) |
|-------------------|--------------------|-----------------------|------------------------|---------------------|-----------------------|---------------------|--------------------|
| 09(1B)            | 02(1B)             | 0027(2B)              | 01(1B)                 | 00(1B)              | 00(1B)                | E0(1B)              | max_pwr(1B)        |

**Table 71 Setup Stage - Interface 0 Descriptor**

| Offset 0 (Length) | Offset1 (DscrType) | Offset2 (InterfaceNum) | Offset3 (AltInterface) | Offset4 (NumEP) | Offset5 (IntfClass) | Offset6 (IntfSubClass) | Offset7 (IntfProtocol) | Offset8 (StringIndex) |
|-------------------|--------------------|------------------------|------------------------|-----------------|---------------------|------------------------|------------------------|-----------------------|
| 09(1B)            | 04(1B)             | 00(1B)                 | 00(1B)                 | 04(1B)          | xx(1B)              | E0(1B)                 | xx(1B)                 | 00(1B)                |

**Table 72 Setup Stage - FEP1 Descriptor**

| Offset 0 (Length) | Offset1 (DscrType) | Offset2 (EPAddr) | Offset3 (Attribute) | Offset4 (MaxPktSize) | Offset6 (Interval) |
|-------------------|--------------------|------------------|---------------------|----------------------|--------------------|
| 07(1B)            | 05(1B)             | 81(1B)           | 02(1B) bulk         | 0064(2B)             | 00(1B)             |

Table 73 Setup Stage - FEP2 Descriptor

| Offset 0<br>(Length) | Offset1<br>(DscrType) | Offset2<br>(EPAddr) | Offset3<br>(Attribute) | Offset4<br>(MaxPktSize) | Offset6<br>(Interval) |
|----------------------|-----------------------|---------------------|------------------------|-------------------------|-----------------------|
| 07(1B)               | 05(1B)                | 02(1B)              | 02(1B) bulk            | 0064(2B)                | 00(1B)                |

Table 74 Setup Stage - FEP2 Descriptor

| Offset 0<br>(Length) | Offset1<br>(DscrType) | Offset2<br>(EPAddr) | Offset3<br>(Attribute) | Offset4<br>(MaxPktSize) | Offset6<br>(Interval) |
|----------------------|-----------------------|---------------------|------------------------|-------------------------|-----------------------|
| 07(1B)               | 05(1B)                | 83(1B)              | 03(1B) interrupt       | 0008(2B)                | p3_interval(1B)       |

- Get\_Descriptor(String) Index0, LanguageID Code

Table 75 Setup Stage

| bmReq | bReq | wValue(2B) | wIndex(2B) | wLength(2B) |
|-------|------|------------|------------|-------------|
| 80    | 06   | 0003       | 0000       | length      |

Table 76 Data Stage

| Offset0 (Length) | Offset1 (DscrType) | Offset2 (LanguageID) |
|------------------|--------------------|----------------------|
| 04(1B)           | 03(1B)             | 0904(2B)             |

- Get\_Descriptor(String) Index1, manufacture

Table 77 Setup Stage

| bmReq | bReq | wValue(2B) | wIndex(2B) | wLength(2B) |
|-------|------|------------|------------|-------------|
| 80    | 06   | 0103       | 0904       | length      |

Table 78 Data Stage

| Offset0 (Length) | Offset1 (DscrType) |        |
|------------------|--------------------|--------|
| length(1B)       | 03(1B)             | String |

- Get\_Descriptor(String) Index2, product

Table 79 Setup Stage

| bmReq | bReq | wValue(2B) | wIndex(2B) | wLength(2B) |
|-------|------|------------|------------|-------------|
| 80    | 06   | 0203       | 0904       | length      |

Table 80 Data Stage

| Offset0 (Length) | Offset1 (DscrType) |        |
|------------------|--------------------|--------|
| length(1B)       | 03(1B)             | String |

## APPENDIX 4 - USB Command

- Get\_Descriptor(String) Index3, serial no.

**Table 81 Setup Stage**

| bmReq | bReq | wValue(2B) | wIndex(2B) | wLength(2B) |
|-------|------|------------|------------|-------------|
| 80    | 06   | 0303       | 0904       | length      |

**Table 82 Data Stage**

| Offset0 (Length) | Offset1 (DscrType) |        |
|------------------|--------------------|--------|
| length(1B)       | 03(1B)             | String |

- Get\_Configuration

**Table 83 Setup Stage**

| bmReq | bReq | wValue(2B) | wIndex(2B) | wLength(2B) |
|-------|------|------------|------------|-------------|
| 80    | 08   | 0          | 0          | 0001        |

**Table 84 Data Stage**

| Offset0 (ConfigValue)(1B) |
|---------------------------|
|                           |

- Get\_Interface

**Table 85 Setup Stage**

| bmReq | bReq | wValue(2B) | wIndex(2B) | wLength(2B) |
|-------|------|------------|------------|-------------|
| 81    | 10   | 0          | 0          | 0001        |

**Table 86 Data Stage**

| Offset0 (AltIntf)(1B) |
|-----------------------|
| 00                    |

- Set\_Address
- Set\_Configuration
- Set\_Interface
- Clear\_Feature(Device) Remote Wakeup

**Table 87 Setup Stage**

| bmReq | bReq | wValue(2B) | wIndex(2B) | wLength(2B) |
|-------|------|------------|------------|-------------|
| 00    | 01   | 0100       | 0          | 0           |

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- Set\_feature(Device) Remote Wakeup

**Table 88 Setup Stage**

| bmReq | bReq | wValue(2B) | wIndex(2B) | wLength(2B) |
|-------|------|------------|------------|-------------|
| 00    | 03   | 0100       | 0          | 0           |

- Clear\_Feature(EP0,1,2,3) Halt

**Table 89 Setup Stage**

| bmReq | bReq | wValue(2B) | wIndex(2B)  | wLength(2B) |
|-------|------|------------|-------------|-------------|
| 02    | 03   | 0000       | {00, EP no} | 0           |

- Set\_Feature(EP0,1,2,3) Halt

**Table 90 Setup Stage**

| bmReq | bReq | wValue(2B) | wIndex(2B)  | wLength(2B) |
|-------|------|------------|-------------|-------------|
| 02    | 03   | 0000       | {00, EP no} | 0           |

## 11 APPENDIX 5 - Design Notes for Ethernet & MII Application(HPNA&HomePlug)

### 11.1 48MHz Crystal

ADM8511/X need a 48 MHz crystal (+/- 50ppm, over tone) to work on USB side. Because the 48 MHz crystal is a over tone part, It need work with a L/C pair. However, 48 MHz fundamental crystal is also valid and associates with two ceramic capacitor.

### 11.2 SRAM

All of the SRAM pin can be NC (No Connection).

### 11.3 RST# and POREN\_N

- Internal Power On Reset in ethernet only or combo (Ethernet & HPNA) solution: The ADM8511/X provides internal power reset. In ethernet only or combo solution, you can let RST# and POREN\_N pin NC.
- External reset in external PHY only solution.(e.g. Home PNA only) Condition: (1) POREN\_N pull to high and (2) RST# asserts low when external reset is active.

RST# combines with a reset circuit (e.g. RC circuit) to provide a low pulse to be reset signal. The duration of the low pulse is 50ms at least. The recommended time is more than 80ms. Moreover, it still needs 25MHz crystal oscillation circuit and Ribb pin connects a 10K resistor to ground.

### 11.4 XLNKSTS

1. Ethernet only solution: This pin need strapping to low directly
2. Combo or External PHY only solution: reports link status information to system and level change trigger.

### 11.5 LED

All of the LED pin are active Low and only display internal PHY status.

### 11.6 Ethernet pin (LED,XTLP/N,TXOP/N,RXIP/N,RIBB,TST0.....K3

In External PHY solution, All can be NC.

### 11.7 MII interface signal pins

- In ethernet only solution: All of the MII pin can be NC.
- In combo or external PHY only solution
  - MDIO requires external 1.5k pull-up resistor.
  - TXEN requires external 4.7k pull-down resistor. If the external PHY did not provide RXER, this pin needs strapping to low directly.

[www.infineon.com](http://www.infineon.com)