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THIS SPEC IS OBSOLETE

Spec No: 38-05356

Spec Title: CY7C1461AV33/CY7C1463AV33, 36-MBIT (1M X 36/2M X 18) FLOW-THROUGH SRAM WITH NOBL(TM) ARCHITECTURE

Replaced by: None

CY7C1461AV33
CY7C1463AV33

36-Mbit (1M × 36/2M × 18) Flow-Through SRAM with NoBL™ Architecture

Features

- No Bus Latency™ (NoBL™) architecture eliminates dead cycles between write and read cycles
- Supports up to 133 MHz bus operations with zero wait states
  - Data is transferred on every clock
- Pin compatible and functionally equivalent to ZBT™ devices
- Internally self timed output buffer control to eliminate the need to use $\overline{OE}$
- Registered inputs for flow through operation
- Byte write capability
- 3.3 V and 2.5 V I/O power supply
- Fast clock-to-output times
  - 6.5 ns (for 133 MHz device)
- Clock Enable ($\overline{CEN}$) pin to enable clock and suspend operation
- Synchronous self timed writes
- Asynchronous Output Enable
- CY7C1461AV33, CY7C1463AV33 available in JEDEC-standard Pb-free 100-pin TQFP package.
- Three chip enables for simple depth expansion
- Automatic power down feature available using ZZ mode or CE deselect
- Burst capability – linear or interleaved burst order
- Low standby power

Functional Description

The CY7C1461AV33/CY7C1463AV33 are 3.3 V, 1M × 36/2M × 18 Synchronous Flow-Through Burst SRAMs designed specifically to support unlimited true back-to-back read and write operations without the insertion of wait states. The CY7C1461AV33/CY7C1463AV33 is equipped with the advanced NoBL logic required to enable consecutive read and write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data through the SRAM, especially in systems that require frequent write-read transitions.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable ($\overline{CEN}$) signal, which when deasserted suspends operation and extends the previous clock cycle. Maximum access delay from the clock rise is 6.5 ns (133 MHz device).

Write operations are controlled by the two or four Byte Write Select (BW_X) and a Write Enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self timed write circuitry.

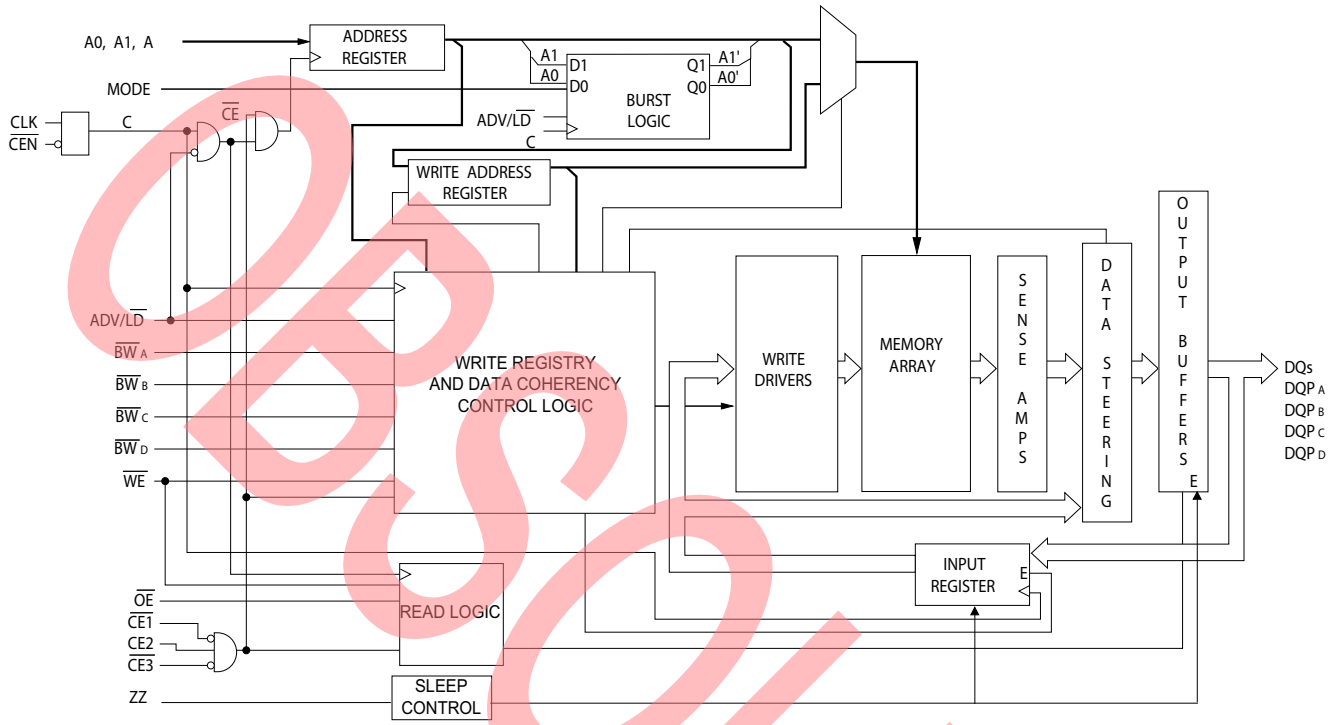
Three synchronous Chip Enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output tri-state control. To avoid bus contention, the output drivers are synchronously tri-stated during the data portion of a write sequence.

For a complete list of related documentation, click here.

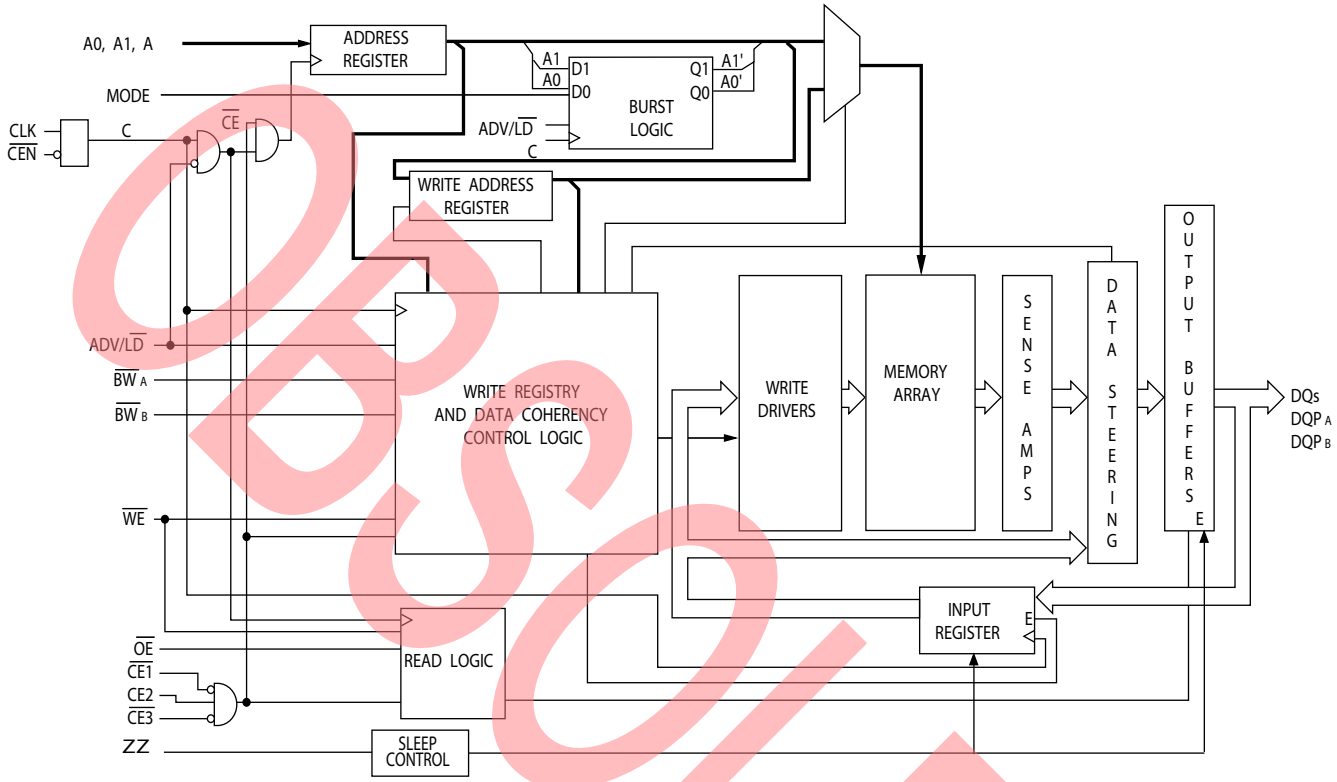
Selection Guide

Description	133 MHz	Unit
Maximum Access Time	6.5	ns
Maximum Operating Current	310	mA
Maximum CMOS Standby Current	120	mA

Logic Block Diagram – CY7C1461AV33



Logic Block Diagram – CY7C1463AV33



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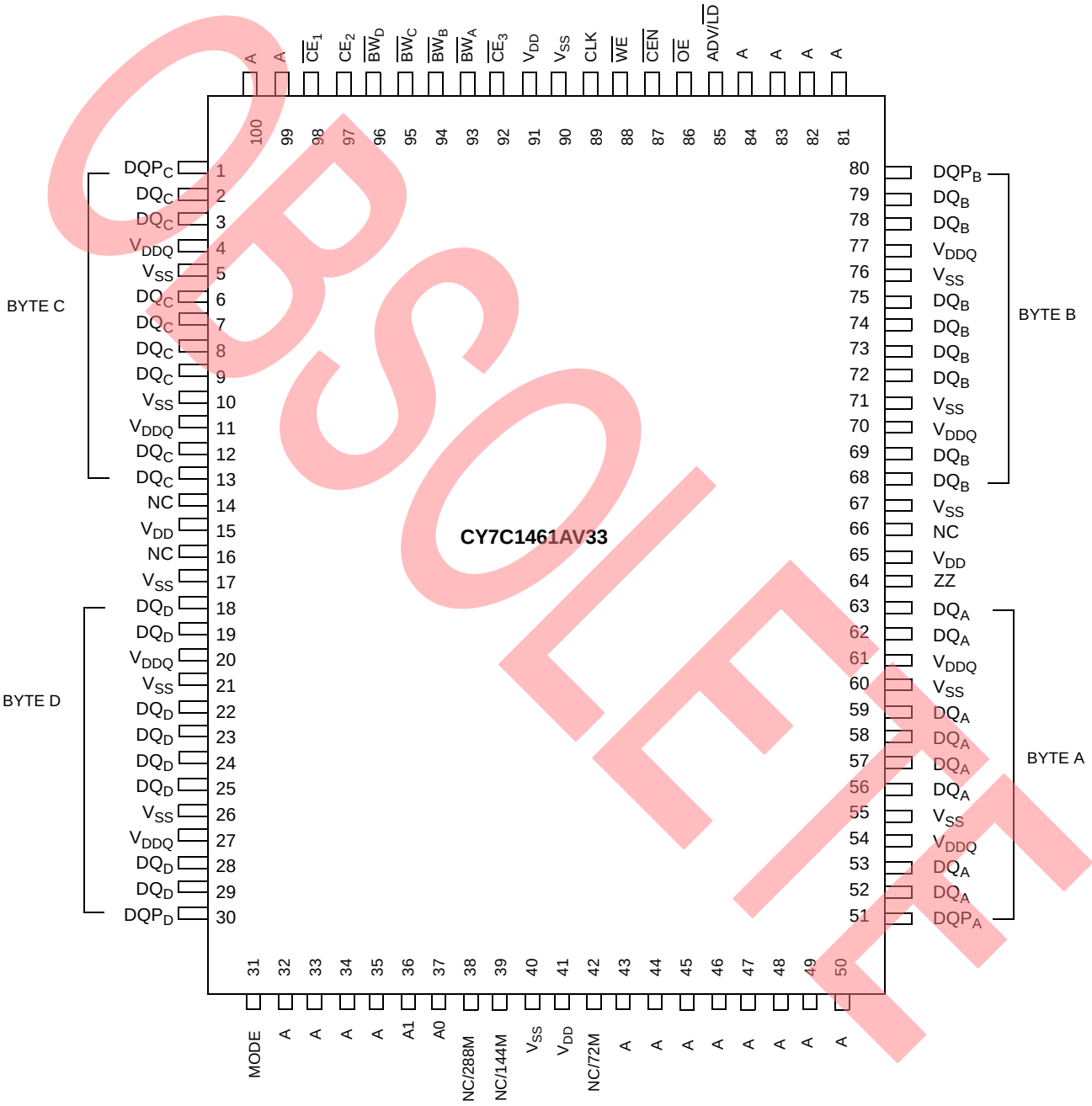
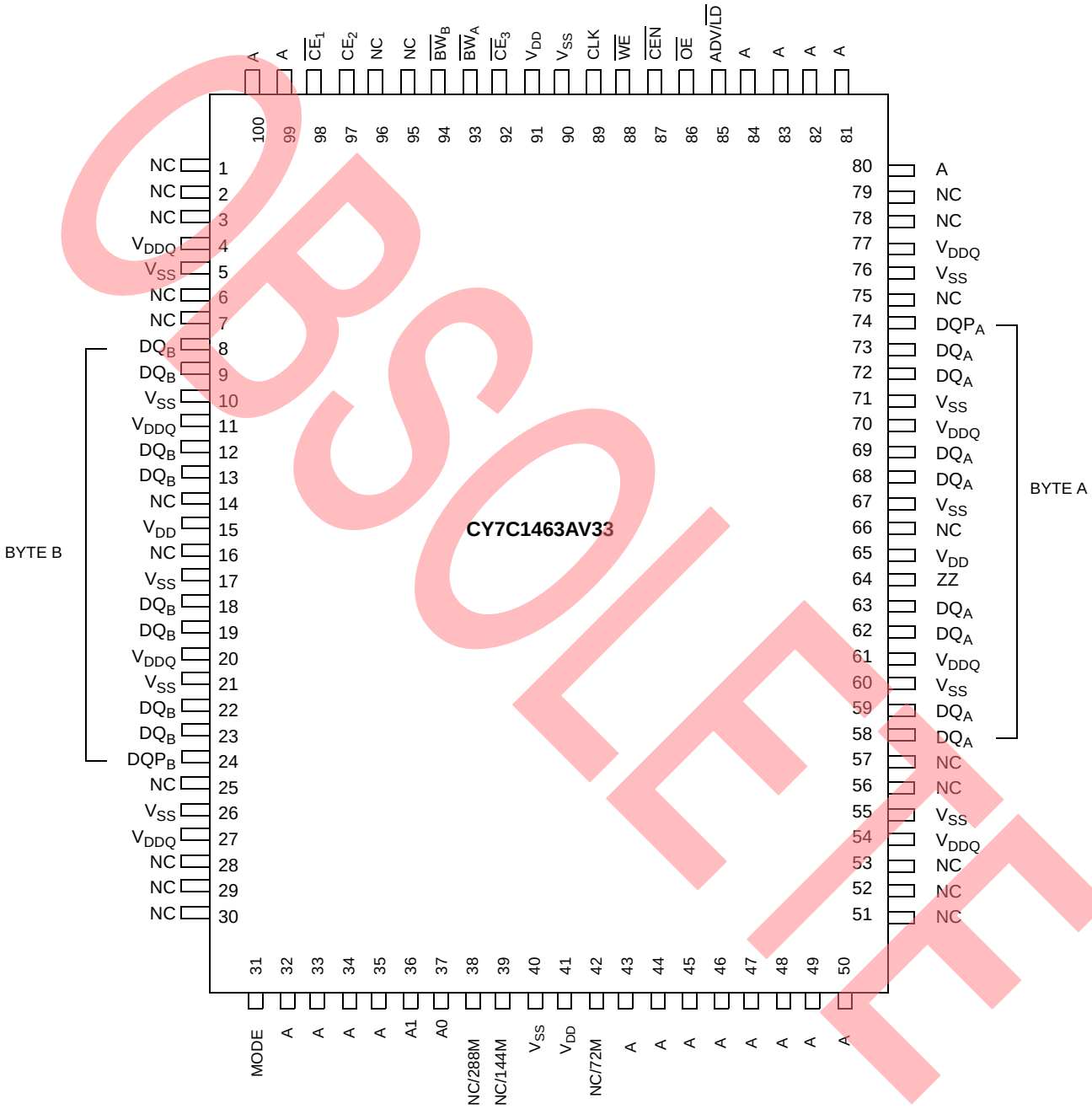
Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout



Pin Configurations (continued)

Figure 2. 100-pin TQFP (14 × 20 × 1.4 mm) pinout



Pin Definitions

Pin Name	I/O	Description
A_0, A_1, A	Input-Synchronous	**Address Inputs.** Used to select one of the address locations. Sampled at the rising edge of the CLK. $A_{[1:0]}$ are fed to the two-bit burst counter.
$\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$	Input-Synchronous	**Byte Write Inputs, Active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{WE}$	Input-Synchronous	**Write Enable Input, Active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/$\overline{LD}$	Input-Synchronous	**Advance or Load Input**. Used to advance the on-chip address counter or load a new address. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After deselecting, drive ADV/$\overline{LD}$ LOW to load a new address.
CLK	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE}_1$	Input-Synchronous	**Chip Enable 1 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select or deselect the device.
CE_2	Input-Synchronous	**Chip Enable 2 Input, Active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select or deselect the device.
$\overline{CE}_3$	Input-Synchronous	**Chip Enable 3 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select or deselect the device.
$\overline{OE}$	Input-Asynchronous	**Output Enable, Asynchronous Input, Active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected.
$\overline{CEN}$	Input-Synchronous	**Clock Enable Input, Active LOW**. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Because deasserting $\overline{CEN}$ does not deselect the device, use $\overline{CEN}$ to extend the previous cycle when required.
ZZ	Input-Asynchronous	**ZZ "Sleep" Input**. This active HIGH input places the device in a non time critical sleep condition with data integrity preserved. During normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull down.
DQ_s	I/O-Synchronous	**Bidirectional Data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ_s and $DQP_{[A:D]}$ are placed in a tri-state condition.The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
DQP_X	I/O-Synchronous	**Bidirectional Data Parity I/O Lines.** Functionally, these signals are identical to DQ_s. During write sequences, DQP_X is controlled by BW_X correspondingly.
MODE	Input Strap Pin	**Mode Input.** Selects the burst order of the device. When tied to Gnd selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence.
V_{DD}	Power Supply	**Power Supply Inputs to the Core of the Device**.
V_{DDQ}	I/O Power Supply	**Power Supply for I/O Circuitry**.
V_{SS}	Ground	**Ground for the Device**.
NC	N/A	**No Connects**. Not internally connected to the die.
NC/72M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/144M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/288M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.

Pin Definitions (continued)

Pin Name	I/O	Description
NC/576M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/1G	N/A	**Not Connected to the Die**. Can be tied to any voltage level.

Functional Overview

The CY7C1461AV33/CY7C1463AV33 is a synchronous flow through burst SRAM designed specifically to eliminate wait states during Write-Read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the clock enable input signal (CEN). If CEN is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with CEN. Maximum access delay from the clock rise (t_{CDV}) is 6.5 ns (133 MHz device).

Accesses can be initiated by asserting all three chip enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) active at the rising edge of the clock. If CEN is active LOW and ADV/LD is asserted LOW, the address presented to the device is latched. The access can either be a read or write operation, depending on the status of the write enable ($\overline{WE}$). BW_X can be used to conduct byte write operations.

Write operations are qualified by the Write Enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous chip enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous output enable ($\overline{OE}$) simplify depth expansion. All operations (reads, writes, and deselects) are pipelined. ADV/LD must be driven LOW after the device is deselected to load a new address for the next operation.

Single Read Accesses

A read access is initiated when these conditions are satisfied at clock rise:

- $\overline{CEN}$ is asserted LOW
- $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are ALL asserted active
- The write enable input signal $\overline{WE}$ is deasserted HIGH
- ADV/$\overline{LD}$ is asserted LOW

The address presented to the address inputs is latched into the address register and presented to the memory array and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the output buffers. The data is available within 6.5 ns (133 MHz device) provided $\overline{OE}$ is active LOW. After the first clock of the read access, the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW for the device to drive out the requested data. On the subsequent clock, another operation (Read/Write/Deselect) can be initiated. When the SRAM is deselected at clock rise by one of the chip enable signals, its output is tri-stated immediately.

Burst Read Accesses

The CY7C1461AV33/CY7C1463AV33 has an on-chip burst counter that provides the ability to supply a single address and conduct up to four reads without reasserting the address inputs. ADV/LD must be driven LOW to load a new address into the SRAM, as described in the Single Read Accesses section. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and wraps around when incremented sufficiently. A HIGH input on ADV/LD increments the internal burst counter regardless of the state of chip enable inputs or WE. WE is latched at the beginning of a burst cycle. Therefore, the type of access (read or write) is maintained throughout the burst sequence.

Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) CEN is asserted LOW, (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are ALL asserted active, and (3) the write signal WE is asserted LOW. The address presented to the address bus is loaded into the address register. The write signals are latched into the control logic block. The data lines are automatically tri-stated regardless of the state of the $\overline{OE}$ input signal. This allows the external logic to present the data on DQs and DQP_X.

On the next clock rise the data presented to DQs and DQP_X (or a subset for byte write operations, see Truth Table on page 10 for details) inputs is latched into the device and the write is complete. Additional accesses (read/write/deselect) can be initiated on this cycle.

The data written during the write operation is controlled by $\overline{BW_X}$ signals. The CY7C1461AV33/CY7C1463AV33 provides byte write capability that is described in the truth table. Asserting the (WE) with the selected byte write select input selectively writes to only the desired bytes. Bytes not selected during a byte write operation remains unaltered. A synchronous self timed write mechanism is provided to simplify the write operations. Byte write capability is included to greatly simplify Read/Modify/Write sequences, which can be reduced to simple byte write operations.

Because the CY7C1461AV33/CY7C1463AV33 is a common I/O device, data must not be driven into the device when the outputs are active. The $\overline{OE}$ can be deasserted HIGH before presenting data to the DQs and DQP_X inputs. This tri-states the output drivers. As a safety precaution, DQs and DQP_X are automatically tri-stated during the data portion of a write cycle, regardless of the state of $\overline{OE}$.

Burst Write Accesses

The CY7C1461AV33/CY7C1463AV33 has an on-chip burst counter that provides the ability to supply a single address and conduct up to four write operations without reasserting the address inputs. ADV/LD must be driven LOW to load the initial address, as described in the Single Write Accesses on page 8. When ADV/LD is driven HIGH on the subsequent clock rise, the chip enables ($\overline{CE_1}$, CE_2, and $\overline{CE_3}$) and WE inputs are ignored and the burst counter is incremented. The correct BW_X inputs must be driven in each cycle of the burst write, to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation sleep mode. Two clock cycles are required to enter into or exit from this sleep mode. When in this mode, data integrity is guaranteed. Accesses pending when entering the sleep mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the sleep mode. $\overline{CE}_1$, CE_2, and $\overline{CE}_3$, must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	ZZ $\geq V_{DD} - 0.2$ V	–	100	mA
t_{ZZS}	Device operation to ZZ	ZZ $\geq V_{DD} - 0.2$ V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ $\leq$ 0.2 V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

Truth Table

The truth table for CY7C1461AV33/CY7C1463AV33 follows.

Operation [1, 2, 3, 4, 5, 6, 7]	Address Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	ADV/$\overline{LD}$	$\overline{WE}$	$\overline{BW_X}$	$\overline{OE}$	$\overline{CEN}$	CLK	DQ
Deselect Cycle	None	H	X	X	L	L	X	X	X	L	L->H	Tristate
Deselect Cycle	None	X	X	H	L	L	X	X	X	L	L->H	Tristate
Deselect Cycle	None	X	L	X	L	L	X	X	X	L	L->H	Tristate
Continue Deselect Cycle	None	X	X	X	L	H	X	X	X	L	L->H	Tristate
Read Cycle (Begin Burst)	External	L	H	L	L	L	H	X	L	L	L->H	Data Out (Q)
Read Cycle (Continue Burst)	Next	X	X	X	L	H	X	X	L	L	L->H	Data Out (Q)
NOP/Dummy Read (Begin Burst)	External	L	H	L	L	L	H	X	H	L	L->H	Tristate
Dummy Read (Continue Burst)	Next	X	X	X	L	H	X	X	H	L	L->H	Tristate
Write Cycle (Begin Burst)	External	L	H	L	L	L	L	L	X	L	L->H	Data In (D)
Write Cycle (Continue Burst)	Next	X	X	X	L	H	X	L	X	L	L->H	Data In (D)
NOP/Write Abort (Begin Burst)	None	L	H	L	L	L	L	H	X	L	L->H	Tristate
Write Abort (Continue Burst)	Next	X	X	X	L	H	X	H	X	L	L->H	Tristate
Ignore Clock Edge (Stall)	Current	X	X	X	L	X	X	X	X	H	L->H	–
Sleep Mode	None	X	X	X	H	X	X	X	X	X	X	Tristate

Notes
1. X = "Don't Care." H = logic HIGH, L = logic LOW. $\overline{BW}$x = L signifies at least one byte write select is active, $\overline{BW}$x = Valid signifies that the desired byte write selects are asserted, see truth table for details.
2. Write is defined by $\overline{BW_X}$, and $\overline{WE}$. See truth table for read or write.
3. When a write cycle is detected, all IOs are tristated, even during byte writes.
4. The DQs and DQP_X pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
5. $\overline{CEN}$ = H, inserts wait states.
6. Device powers up deselected and the IOs in a tri-state condition, regardless of $\overline{OE}$.
7. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and DQP_X = Tri-state when $\overline{OE}$ is inactive or when the device is deselected, and DQs and DQP_X = data when $\overline{OE}$ is active.

Truth Table for Read/Write

Function (CY7C1461AV33) [8, 9]	$\overline{WE}$	$\overline{BW_A}$	$\overline{BW_B}$	$\overline{BW_C}$	$\overline{BW_D}$
Read	H	X	X	X	X
Write – No Bytes Written	L	H	H	H	H
Write Byte A – (DQ_A and DQP_A)	L	L	H	H	H
Write Byte B – (DQ_B and DQP_B)	L	H	L	H	H
Write Byte C – (DQ_C and DQP_C)	L	H	H	L	H
Write Byte D – (DQ_D and DQP_D)	L	H	H	H	L
Write All Bytes	L	L	L	L	L

Truth Table for Read/Write

Function (CY7C1463AV33) [8, 9]	$\overline{WE}$	$\overline{BW_b}$	$\overline{BW_a}$
Read	H	X	X
Write – No Bytes Written	L	H	H
Write Byte a – (DQ_a and DQP_a)	L	H	L
Write Byte b – (DQ_b and DQP_b)	L	L	H
Write Both Bytes	L	L	L

Notes
8. X = “Don't Care.” H = logic HIGH, L = logic LOW. $\overline{BW}$x = L signifies at least one byte write select is active, $\overline{BW}$x = Valid signifies that the desired byte write selects are asserted, see truth table for details.
9. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{BW_X}$ is valid. Appropriate write is done based on which byte write is active.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{DD} Relative to GND .....–0.5 V to +4.6 V

Supply Voltage on V_{DDQ} Relative to GND .... –0.5 V to +V_{DD}

DC Voltage Applied to Outputs in Tri-State .....–0.5 V to V_{DDQ} + 0.5 V

DC Input Voltage .....–0.5 V to V_{DD} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V_{DD}
Industrial	–40 °C to +85 °C		

Electrical Characteristics

Over the Operating Range

Parameter [10, 11]	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power supply voltage			3.135	3.6	V
V_{DDQ}	I/O supply voltage	for 3.3 V I/O		3.135	V_{DD}	V
		for 2.5 V I/O		2.375	2.625	V
V_{OH}	Output HIGH voltage	for 3.3 V I/O, I_{OH} = –4.0 mA		2.4	–	V
		for 2.5 V I/O, I_{OH} = –1.0 mA		2.0	–	V
V_{OL}	Output LOW voltage	for 3.3 V I/O, I_{OL} = 8.0 mA		–	0.4	V
		for 2.5 V I/O, I_{OL} = 1.0 mA		–	0.4	V
V_{IH}	Input HIGH voltage[10]	for 3.3 V I/O		2.0	V_{DD} + 0.3 V	V
		for 2.5 V I/O		1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW voltage[10]	for 3.3 V I/O		–0.3	0.8	V
		for 2.5 V I/O		–0.3	0.7	V
I_X	Input leakage current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input current of MODE	Input = V_{SS}		–30	–	µA
		Input = V_{DD}		–	5	µA
	Input current of ZZ	Input = V_{SS}		–5	–	µA
		Input = V_{DD}		–	30	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		–5	5	µA
I_{DD}	V_{DD} operating supply current	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	7.5 ns cycle, 133 MHz	–	310	mA
I_{SB1}	Automatic CE power down current – TTL Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}; f = f_{MAX}, Inputs Switching	7.5 ns cycle, 133 MHz	–	180	mA
I_{SB2}	Automatic CE power down current – CMOS Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≤ 0.3 V or V_{IN} ≥ V_{DD} – 0.3 V, f = 0, Inputs Static	7.5 ns cycle, 133 MHz	–	120	mA
I_{SB3}	Automatic CE power down current – CMOS Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≤ 0.3 V or V_{IN} ≥ V_{DDQ} – 0.3 V f = f_{MAX}, Inputs Switching	7.5 ns cycle, 133 MHz	–	180	mA
I_{SB4}	Automatic CE Power down current – TTL Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≥ V_{DD} – 0.3 V or V_{IN} ≤ 0.3 V, f = 0, Inputs Static	7.5 ns cycle, 133 MHz	–	135	mA

Notes

10. Overshoot: $V_{IH(AC)}$ < V_{DD} + 1.5 V (Pulse width less than t_{CYC}/2), undershoot: $V_{IL(AC)}$ > –2 V (Pulse width less than t_{CYC}/2).
11. $T_{Power\text{-}up}$: Assumes a linear ramp from 0 V to $V_{DD(min)}$ within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

Capacitance

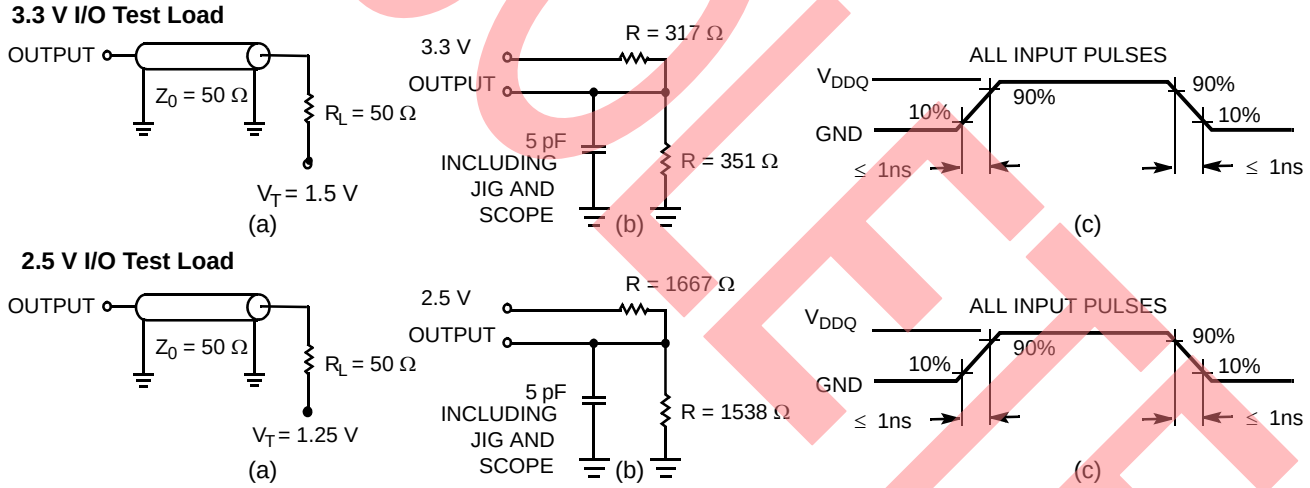
Parameter [12]	Description	Test Conditions	100-pin TQFP Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 2.5 V	6.5	pF
C_{CLK}	Clock input capacitance		3	pF
C_{IO}	Input/Output capacitance		5.5	pF

Thermal Resistance

Parameter [12]	Description	Test Conditions	100-pin TQFP Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51.	25.21	°C/W
Θ_{JC}	Thermal resistance (junction to case)		2.28	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Note
12. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

Over the Operating Range

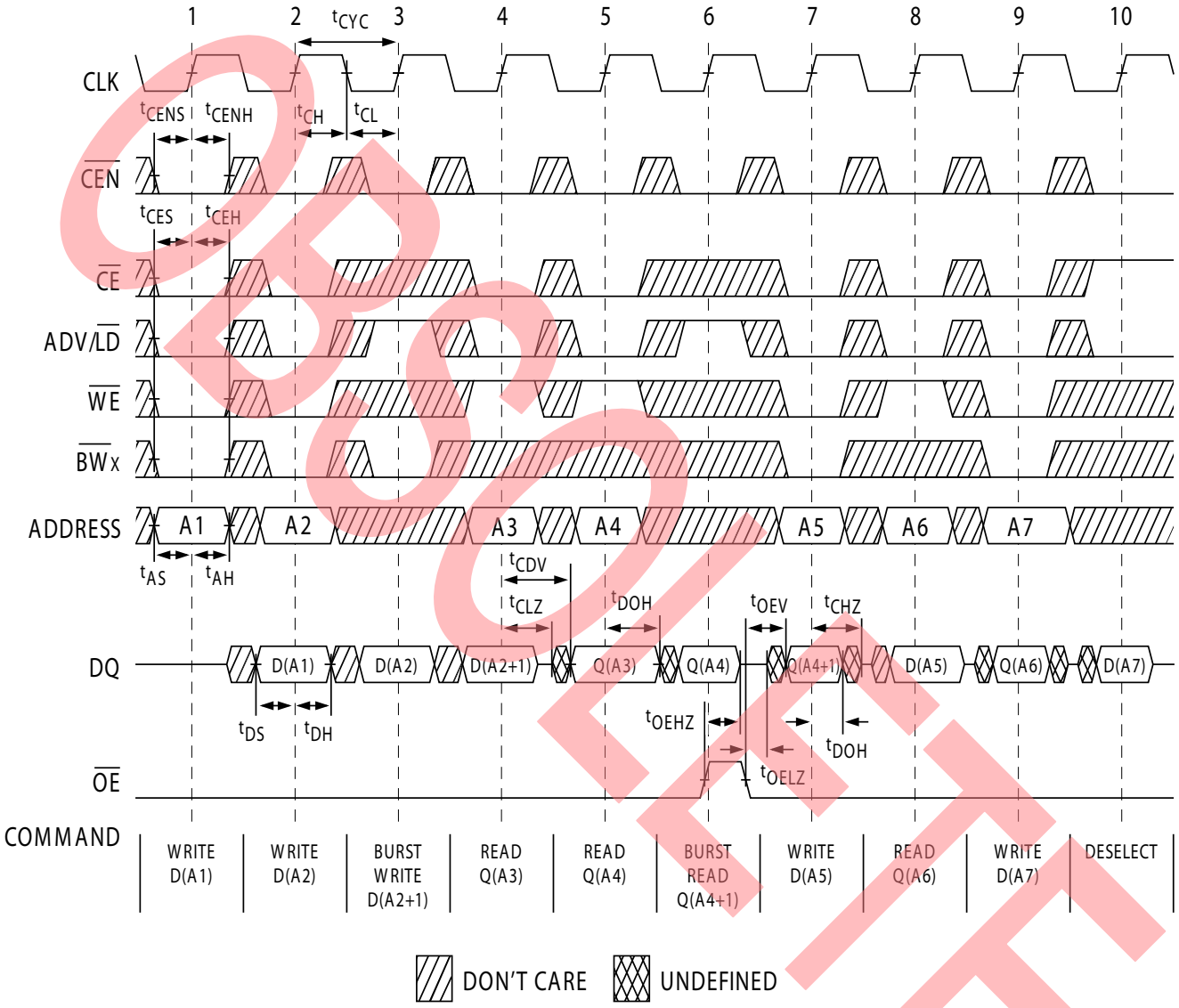
Parameter [13, 14]	Description	133 MHz		Unit
		Min	Max	
t_{POWER}[15]		1	–	ms
Clock				
t_{CYC}	Clock Cycle Time	7.5	–	ns
t_{CH}	Clock HIGH	2.5	–	ns
t_{CL}	Clock LOW	2.5	–	ns
Output Times				
t_{CDV}	Data Output Valid after CLK Rise	–	6.5	ns
t_{DOH}	Data Output Hold after CLK Rise	2.5	–	ns
t_{CLZ}	Clock to Low Z [16, 17, 18]	2.5	–	ns
t_{CHZ}	Clock to High Z [16, 17, 18]	–	3.8	ns
t_{OEV}	$\overline{OE}$ LOW to Output Valid	–	3.0	ns
t_{OELZ}	$\overline{OE}$ LOW to Output Low Z [16, 17, 18]	0	–	ns
t_{OEHZ}	$\overline{OE}$ HIGH to Output High Z [16, 17, 18]	–	3.0	ns
Setup Times				
t_{AS}	Address Setup before CLK Rise	1.5	–	ns
t_{ALS}	ADV/$\overline{LD}$ Setup before CLK Rise	1.5	–	ns
t_{WES}	$\overline{WE}$, $\overline{BW}_X$ Setup before CLK Rise	1.5	–	ns
t_{CENS}	$\overline{CEN}$ Setup before CLK Rise	1.5	–	ns
t_{DS}	Data Input Setup before CLK Rise	1.5	–	ns
t_{CES}	Chip Enable Setup before CLK Rise	1.5	–	ns
Hold Times				
t_{AH}	Address Hold after CLK Rise	0.5	–	ns
t_{ALH}	ADV/$\overline{LD}$ Hold after CLK Rise	0.5	–	ns
t_{WEH}	$\overline{WE}$, $\overline{BW}_X$ Hold after CLK Rise	0.5	–	ns
t_{CENH}	$\overline{CEN}$ Hold after CLK Rise	0.5	–	ns
t_{DH}	Data Input Hold after CLK Rise	0.5	–	ns
t_{CEH}	Chip Enable Hold after CLK Rise	0.5	–	ns

Notes

13. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
14. Test conditions shown in (a) of Figure 3 on page 13 unless otherwise noted.
15. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above $V_{DD(minimum)}$ initially, before a read or write operation can be initiated.
16. t_{CHZ}, t_{CLZ},t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of Figure 3 on page 13. Transition is measured ±200 mV from steady-state voltage.
17. At any voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z prior to Low Z under the same system conditions.
18. This parameter is sampled and not 100% tested.

Switching Waveforms

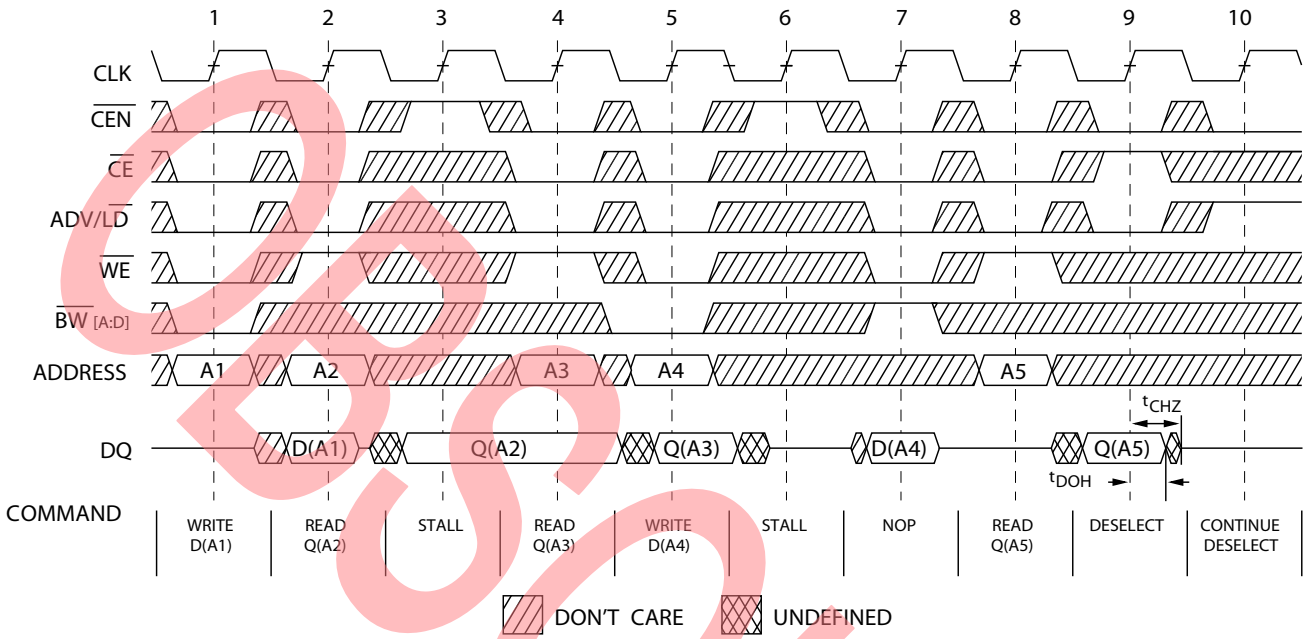
Figure 4. Read/Write Waveforms [19, 20, 21]



Notes
19. For this waveform ZZ is tied LOW.
20. When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
21. Order of the burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.

Switching Waveforms (continued)

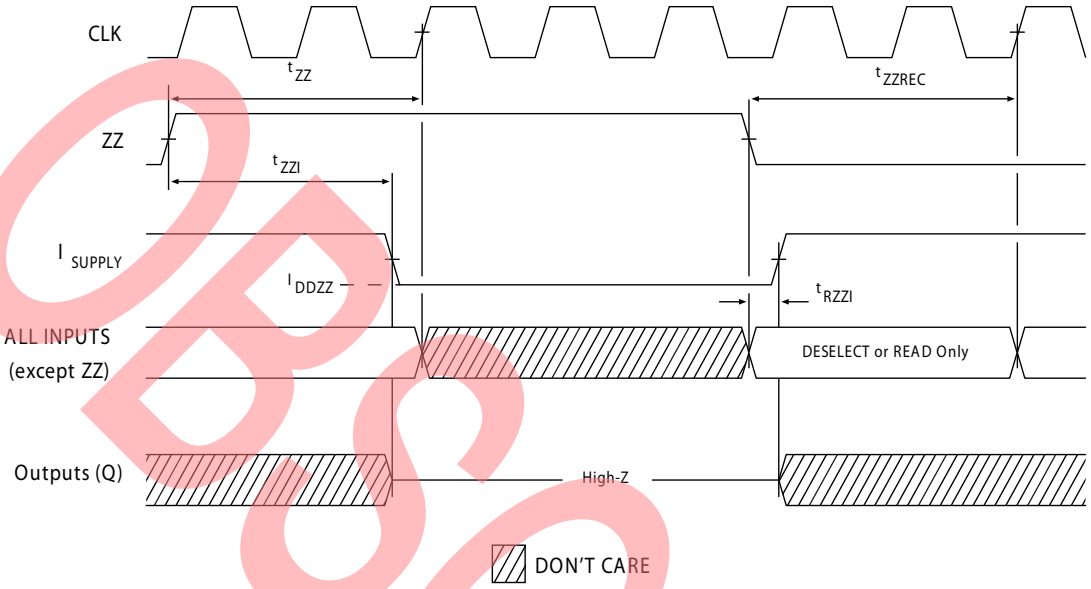
Figure 5. NOP, STALL, and DESELECT Cycles [22, 23, 24]



Notes
22. For this waveform ZZ is tied LOW.
23. When $\overline{CE}$ is LOW, $\overline{CE_1}$ is LOW, CE_2 is HIGH and $\overline{CE_3}$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE_1}$ is HIGH or CE_2 is LOW or $\overline{CE_3}$ is HIGH.
24. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrates $\overline{CEN}$ being used to create a pause. A write is not performed during this cycle.

Switching Waveforms (continued)

Figure 6. ZZ Mode Timing [25, 26]



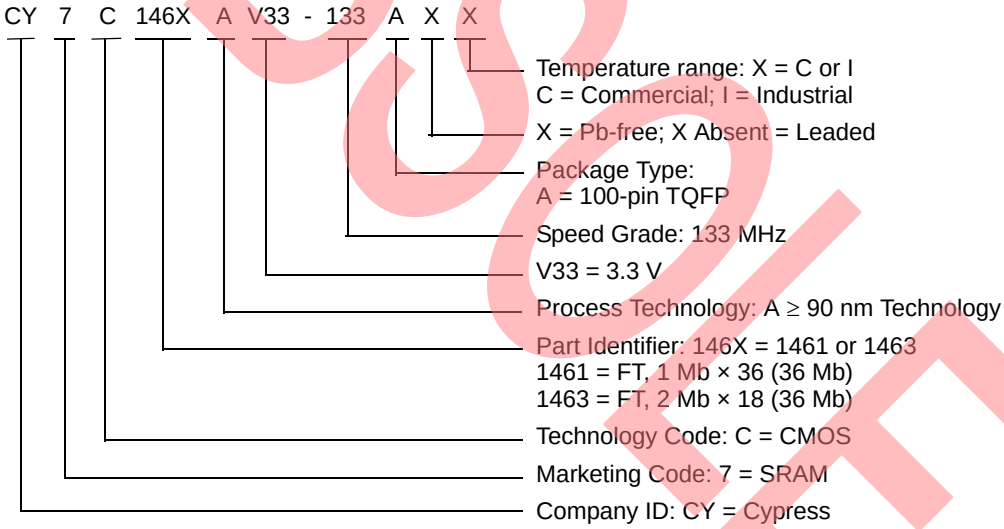
Notes
25. Device must be deselected when entering ZZ mode. See truth table for all possible signal conditions to deselect the device.
26. DQs are in High Z when exiting ZZ sleep mode.

Ordering Information

Cypress offers other versions of this type of product in different configurations and features. The following table contains only the list of parts that are currently available.
For a complete listing of all options, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products, or contact your local sales representative.
Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at http://www.cypress.com/go/datasheet/offices.

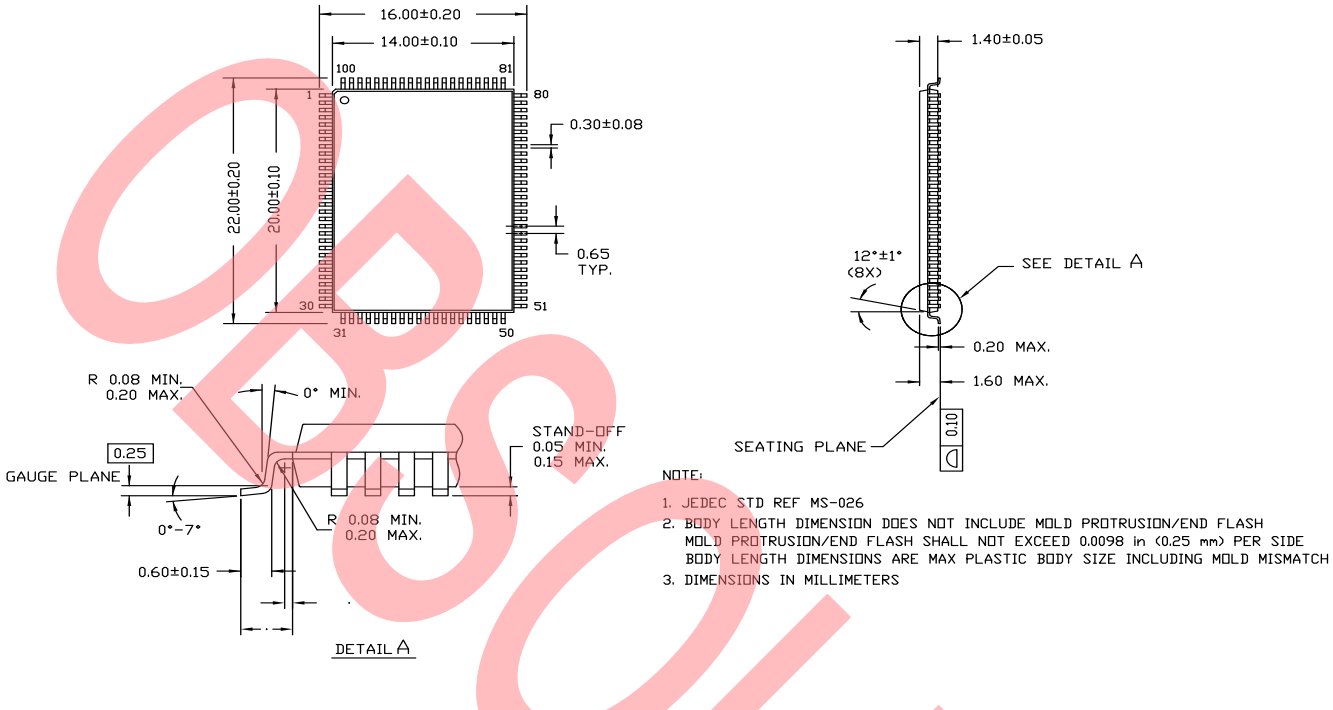
Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
133	CY7C1461AV33-133AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial
	CY7C1463AV33-133AXC			
	CY7C1461AV33-133AXI	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Industrial

Ordering Code Definitions



Package Diagrams

Figure 7. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
$\overline{CEN}$	Clock Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
LSB	Least Significant Bit
MSB	Most Significant Bit
NoBL	No Bus Latency
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mV	millivolt
mm	millimeter
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1461AV33/CY7C1463AV33, 36-Mbit (1M × 36/2M × 18) Flow-Through SRAM with NoBL™ Architecture Document Number: 38-05356				
Revision	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	254911	See ECN	SYT	New data sheet. Part number changed from previous revision (New and old part number differ by the letter “A”).
*A	300131	See ECN	SYT	Updated Features (Removed 150 MHz and 117 MHz frequencies related information). Updated Selection Guide (Removed 150 MHz and 117 MHz frequencies related information). Updated Electrical Characteristics (Removed 150 MHz and 117 MHz frequencies related information). Updated Thermal Resistance (Replaced values of Θ_{JA} and Θ_{JC} parameters from TBD to 25.21 °C/W and 2.58 °C/W respectively for 100-pin TQFP package). Updated Switching Characteristics (Removed 150 MHz and 117 MHz frequencies related information). Updated Ordering Information (Added Pb-free information for 100-pin TQFP, 165-ball FBGA and 209-ball FBGA packages, added “Pb-free BG and BZ packages availability” comment below the Ordering Information).
*B	320813	See ECN	SYT	Updated Pin Configurations (Changed H9 pin from V_{SSQ} to V_{SS} for 209-ball FBGA). Updated Electrical Characteristics (Changed the test condition for V_{OL} parameter from V_{DD} = Min. to V_{DD} = Max., replaced the TBD’s with their respective values for I_{DD}, I_{SB1}, I_{SB2}, I_{SB3} and I_{SB4} parameters). Updated Thermal Resistance (Replaced values of Θ_{JA} and Θ_{JC} parameters from TBD to respective Thermal Values for 165-ball FBGA and 209-ball FBGA Packages). Updated Capacitance (Changed values of C_{IN}, C_{CLK} and $C_{I/O}$ parameters to 6.5 pF, 3 pF and 5.5 pF from 5 pF, 5 pF and 7 pF for 100-pin TQFP Package). Updated Ordering Information (Removed “Pb-free BG packages availability” comment below the Ordering Information).
*C	331551	See ECN	SYT	Updated Pin Configurations (Modified Address Expansion balls in the pinouts for 165-ball FBGA and 209-ball FBGA Packages according to JEDEC standards). Updated Pin Definitions. Updated Functional Overview (Updated ZZ Mode Electrical Characteristics (Changed maximum value of I_{DDZZ} parameter from TBD to 100 mA)). Updated Operating Range (Added Industrial Temperature Range). Updated Electrical Characteristics (Updated test conditions for V_{OL} and V_{OH} parameters, changed maximum value of I_{SB2} parameter from 100 mA to 120 mA, changed maximum value of I_{SB4} parameter from 110 mA to 135 mA respectively). Updated Capacitance (Changed values of C_{IN}, C_{CLK} and $C_{I/O}$ parameters to 7 pF, 7 pF and 6 pF from 5 pF, 5 pF and 7 pF for 165-ball FBGA Package). Updated Ordering Information (By shading and unshading MPNs according to availability).

Document History Page (continued)

Document Title: CY7C1461AV33/CY7C1463AV33, 36-Mbit (1M × 36/2M × 18) Flow-Through SRAM with NoBL™ Architecture Document Number: 38-05356				
Revision	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
*D	417547	See ECN	RXU	Changed status from Preliminary to Final. Changed address of Cypress Semiconductor Corporation from “3901 North First Street” to “198 Champion Court”. Updated Electrical Characteristics (Updated Note 11 (Changed test condition from $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD}$), changed “Input Load Current except ZZ and MODE” to “Input Leakage Current except ZZ and MODE”, changed minimum value of I_X parameter (corresponding to Input current of MODE (Input = V_{SS})) from –5 µA to –30 µA, changed maximum value of I_X parameter (corresponding to Input current of MODE (Input = V_{DD})) from 30 µA to 5 µA respectively, changed minimum value of I_X parameter (corresponding to Input current of ZZ (Input = V_{SS})) from –30 µA to –5 µA, changed maximum value of I_X parameter (corresponding to Input current of ZZ (Input = V_{DD})) from 5 µA to 30 µA respectively). Updated Ordering Information (Updated part numbers, replaced Package Name column with Package Diagram in the Ordering Information table). Updated Package Diagrams.
*E	473650	See ECN	VKN	Updated Maximum Ratings (Added the Maximum Rating for Supply Voltage on V_{DDQ} Relative to GND). Updated TAP AC Switching Characteristics (Changed minimum value of t_{TH} and t_{TL} parameters from 25 ns to 20 ns, changed maximum value of t_{TDOV} parameter from 5 ns to 10 ns). Updated Ordering Information (Updated part numbers).
*F	1274733	See ECN	VKN / AESA	Updated Switching Waveforms (Updated Figure 5 (Corrected typo)).
*G	2499107	See ECN	VKN / PYRS	Updated Logic Block Diagram – CY7C1465AV33 (Corrected typo).
*H	2897278	03/22/2010	NJY	Updated Ordering Information (Removed obsolete part numbers). Updated Package Diagrams.
*I	3208774	03/29/2011	NJY	Updated Ordering Information (Updated part numbers) and added Ordering Code Definitions. Updated Package Diagrams. Updated to new template.
*J	3309506	07/12/2011	OSN	Updated Package Diagrams. Added Acronyms and Units of Measure.

Document History Page (continued)

Document Title: CY7C1461AV33/CY7C1463AV33, 36-Mbit (1M × 36/2M × 18) Flow-Through SRAM with NoBL™ Architecture Document Number: 38-05356				
Revision	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
*K	3591743	05/10/2012	NJY / PRIT	Updated Features (Removed CY7C1465AV33 related information, removed 165-ball FBGA package, 209-ball FBGA package related information). Updated Functional Description (Removed CY7C1465AV33 related information, removed the Note “For best practices recommendations, refer to the Cypress application note *System Design Guidelines* on www.cypress.com.” and its reference). Updated Selection Guide (Removed 100 MHz frequency related information). Removed Logic Block Diagram – CY7C1465AV33. Updated Pin Configurations (Removed 165-ball FBGA package (corresponding to CY7C1461AV33 and CY7C1463AV33), 209-ball FBGA package (corresponding to CY7C1465AV33) related information). Updated Pin Definitions (Removed JTAG related information). Updated Functional Overview (Removed CY7C1465AV33 related information). Updated Truth Table (Removed CY7C1465AV33 related information). Removed Truth Table for Read/Write (Corresponding to CY7C1465AV33). Removed IEEE 1149.1 Serial Boundary Scan (JTAG). Removed TAP Controller State Diagram. Removed TAP Controller Block Diagram. Removed TAP Timing. Removed TAP AC Switching Characteristics. Removed 3.3 V TAP AC Test Conditions. Removed 3.3 V TAP AC Output Load Equivalent. Removed 2.5 V TAP AC Test Conditions. Removed 2.5 V TAP AC Output Load Equivalent. Removed TAP DC Electrical Characteristics and Operating Conditions. Removed Identification Register Definitions. Removed Scan Register Sizes. Removed Identification Codes. Removed Boundary Scan Order (Corresponding to 165-ball FBGA package). Removed Boundary Scan Order (Corresponding to 209-ball FBGA package). Updated Electrical Characteristics (Removed 100 MHz frequency related information). Updated Capacitance (Removed 209-ball FBGA package related information). Updated Thermal Resistance (Removed 209-ball FBGA package related information). Updated Switching Characteristics (Removed 100 MHz frequency related information). Updated Package Diagrams (Removed 165-ball FBGA package, 209-ball FBGA package related information). Replaced all instances of IO with I/O across the document.
*L	3690005	07/24/2012	PRIT	No technical updates. Completing Sunset Review.
*M	4572829	11/18/2014	PRIT	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Package Diagrams: spec 51-85050 – Changed revision from *D to *E.
*N	4865506	07/30/2015	PRIT	Updated to new template. Completing Sunset Review.
*O	5373812	07/26/2016	PRIT	Obsolete document. Completing Sunset Review.

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