

# TLF4277-2

Low Drop Out Linear Voltage Regulator  
Integrated Current Monitor

## Data Sheet

Rev. 1.0, 2014-03-13

Automotive Power

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## Low Drop Out Linear Voltage Regulator Integrated Current Monitor

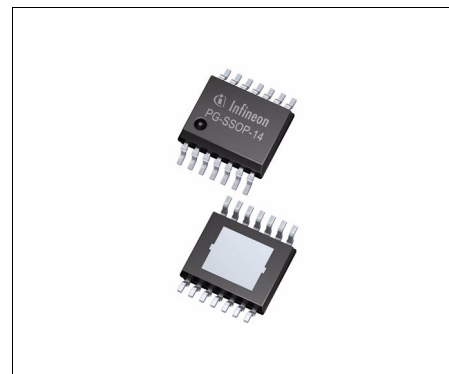
TLF4277-2EL



### 1 Overview

#### Features

- Integrated Current Monitor
- Overvoltage, Overtemperature and Overcurrent Detection
- Adjustable Output Voltage
- Output Current up to 300 mA
- Adjustable Output Current Limitation
- Very Low Current Consumption
- Very Low Dropout Voltage
- Stable with Ceramic Output Capacitor of 1  $\mu$ F
- Wide Input Voltage Range up to 40 V
- Reverse Polarity Protection
- Short Circuit Protected
- Overtemperature Shutdown
- Automotive Temperature Range  $-40\text{ }^{\circ}\text{C} \leq T_j \leq 150\text{ }^{\circ}\text{C}$
- Green Product (RoHS and WEEE compliant)
- AEC Qualified



PG-SSOP14 EP

#### Description

The TLF4277-2 is the ideal companion IC to supply active antennas for car infotainment applications. The adjustable output voltage makes the TLF4277-2 capable of supplying the majority of standard active antennas such as:

- FM/AM
- DAB
- XM
- SIRIUS

The TLF4277-2 is a monolithic integrated low drop out voltage regulator capable of supplying loads up to 300 mA. For an input voltage up to 40 V the TLF4277-2 provides an adjustable output voltage in a range from 5 V up to 12 V. The integrated current monitor function is a unique feature that provides diagnosis and system protection functionality. Fault conditions such as overtemperature and output overvoltage are monitored and indicated at the current sense output. The maximum output current limit of the device is adjustable to provide additional protection to the connected load.

Via the enable function the IC can be disabled to lower the power consumption. The PG-SSOP14 EP package provides an enhanced thermal performance within a SO8 body size.

| Type        | Package      | Marking |
|-------------|--------------|---------|
| TLF4277-2EL | PG-SSOP14 EP | 4277-2  |

## 2 Block Diagram

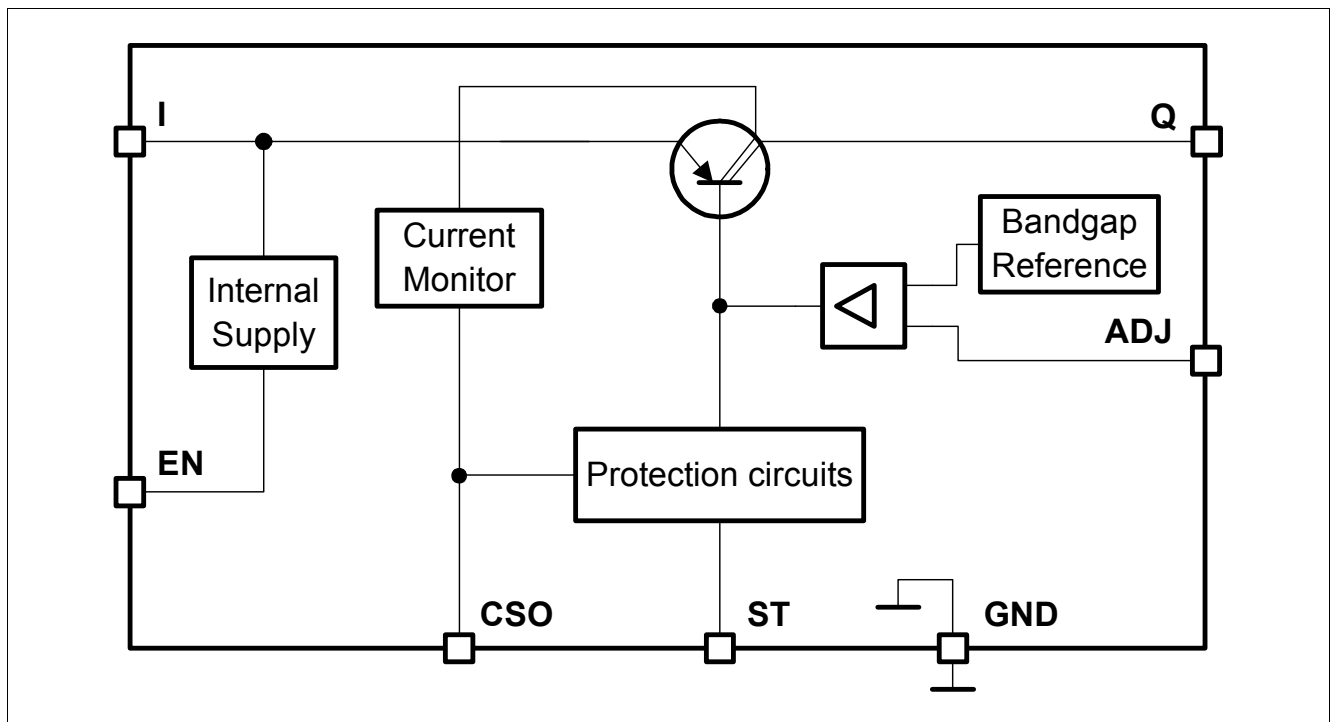


Figure 1 Block and simplified application diagram TLF4277-2 (Package PG-SSOP14 EP)

## 3 Pin Configuration

### 3.1 Pin Assignment

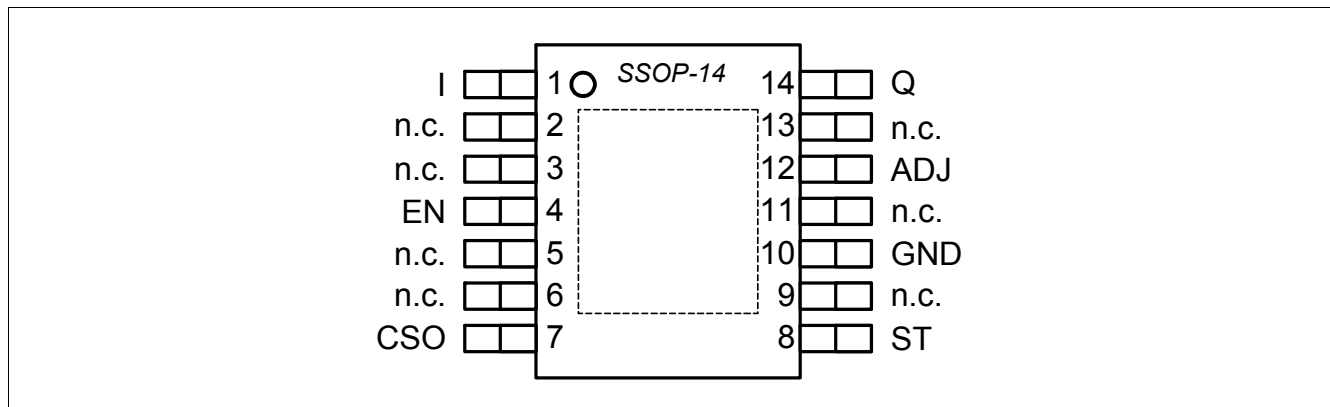


Figure 2 Pin Configuration (top view)

### 3.2 Pin Definitions and Functions

| Pin     | Symbol | Function                                                                                                                                                                                      |
|---------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | I      | <b>IC Supply</b><br>Place a capacitor from I to GND close to the IC for compensating line influences.                                                                                         |
| 4       | EN     | <b>Enable</b><br>High signal enables the regulator;<br>Low signal disables the regulator;<br>Connect to I, if the Enable function is not needed                                               |
| 7       | CSO    | <b>Current Sense Out</b><br>Current monitor and status output                                                                                                                                 |
| 8       | ST     | <b>Status Output</b><br>Digital output signal with open collector output.<br>A low signal indicates fault conditions at the regulator's output.                                               |
| 10      | GND    | <b>Ground</b>                                                                                                                                                                                 |
| 12      | ADJ    | <b>Voltage Adjust</b><br>Connect an external voltage divider to configure the output voltage                                                                                                  |
| 14      | Q      | <b>Regulator Output</b><br>Connect a capacitor between Q and GND close to the IC pins, respecting the values given for its capacitance $C_Q$ and ESR in the table <a href="#">Chapter 4.2</a> |
|         | PAD    | <b>Heat sink</b><br>Connect to PCB heat sink area and GND                                                                                                                                     |
| 2,3,5,6 | n.c.   | <b>Not Connected</b><br>Internally not connected; Connect to PCB GND                                                                                                                          |
| 9,11,13 | n.c.   | <b>Not Connected</b><br>Internally not connected; Connect to PCB GND                                                                                                                          |

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

**Table 1 Absolute Maximum Ratings<sup>1)</sup>**

$T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter                                               | Symbol            | Values |      |      | Unit | Note / Test Condition                         | Number   |
|---------------------------------------------------------|-------------------|--------|------|------|------|-----------------------------------------------|----------|
|                                                         |                   | Min.   | Typ. | Max. |      |                                               |          |
| Voltage Ratings                                         |                   |        |      |      |      |                                               |          |
| IC Supply I                                             | $V_I$             | -16    |      | 45   | V    | –                                             | P_4.1.1  |
| Enable Input EN                                         | $V_{EN}$          | -16    |      | 45   | V    | –                                             | P_4.1.2  |
| Voltage Adjust Input ADJ                                | $V_{ADJ}$         | -0.3   |      | 16   | V    | –                                             | P_4.1.3  |
| Regulator Output Q                                      | $V_Q$             | -0.3   |      | 45   | V    | $V_Q < V_I + 5\text{ V}$                      | P_4.1.4  |
| Current Monitor Out CSO                                 | $V_{CSO}$         | -0.3   |      | 5    | V    | –                                             | P_4.1.5  |
| Status Output                                           | $V_{ST}$          | -0.3   |      | 45   | V    | <sup>2)</sup> see also “Status Output Signal” | P_4.1.6  |
| Temperatures                                            |                   |        |      |      |      |                                               |          |
| Junction Temperature                                    | $T_j$             | -40    |      | 150  | °C   | –                                             | P_4.1.7  |
| Storage Temperature                                     | $T_{stg}$         | -55    |      | 150  | °C   | –                                             | P_4.1.8  |
| ESD Susceptibility                                      |                   |        |      |      |      |                                               |          |
| ESD Susceptibility to GND                               | $V_{ESD}$         | -2     |      | 2    | kV   | HBM <sup>3)</sup>                             | P_4.1.9  |
| ESD Susceptibility to GND                               | $V_{ESD}$         | -500   |      | 500  | V    | CDM <sup>4)</sup>                             | P_4.1.10 |
| ESD Susceptibility Pin 1, 7, 8, 14 (corner pins) to GND | $V_{ESD1,7,8,14}$ | -750   |      | 750  | V    | CDM <sup>4)</sup>                             | P_4.1.11 |

1) Not subject to production test, specified by design.

2) Special care must be taken to control (e.g. by optical inspection) the proper handling of ST pin with an external resistor and not connecting directly to a higher voltage level, which allows an uncontrolled current flowing into the pin.

3) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)

4) ESD susceptibility, Charged Device Model “CDM” according JEDEC JESD22-C101

#### Notes

1. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.
2. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## 4.2 Functional Range

**Table 2 Functional Range**

| Parameter                                    | Symbol     | Values         |      |        | Unit        | Note / Test Condition | Number  |
|----------------------------------------------|------------|----------------|------|--------|-------------|-----------------------|---------|
|                                              |            | Min.           | Typ. | Max.   |             |                       |         |
| Input Voltage                                | $V_I$      | $V_Q + V_{dr}$ | –    | 40     | V           | –                     | P_4.2.1 |
| Output Voltage Range                         | $V_Q$      | 5              | –    | 12     | V           | –                     | P_4.2.2 |
| Current Sense Output Resistor                | $R_{CSO}$  | 850            | –    | 25.5 k | $\Omega$    | –                     | P_4.2.3 |
| Current Sense Output Capacitor <sup>1)</sup> | $C_{CSO}$  | 1              | –    | 4.7    | $\mu F$     | –                     | P_4.2.4 |
| Junction Temperature                         | $T_j$      | -40            | –    | 150    | $^{\circ}C$ | –                     | P_4.2.5 |
| Output Capacitor Requirements <sup>1)</sup>  | $C_Q$      | 1              | –    | –      | $\mu F$     | – <sup>2)</sup>       | P_4.2.6 |
| Output Capacitor Requirements <sup>1)</sup>  | $ESR_{CQ}$ | –              | –    | 10     | $\Omega$    | – <sup>3)</sup>       | P_4.2.7 |

1) Not subject to production test, specified by design

2) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

3) Relevant ESR value at  $f = 10$  kHz

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

## 4.3 Thermal Resistance

**Table 3 Thermal Resistance <sup>1)</sup>**

| Parameter           | Symbol     | Values |      |      | Unit | Note / Test Condition                                | Number  |
|---------------------|------------|--------|------|------|------|------------------------------------------------------|---------|
|                     |            | Min.   | Typ. | Max. |      |                                                      |         |
| Junction to Case... | $R_{thJC}$ | –      | 8    | –    | K/W  | measured to the exposed pad                          | P_4.3.1 |
| Junction to Ambient | $R_{thJA}$ | –      | 132  | –    | K/W  | Footprint only <sup>2)</sup>                         | P_4.3.2 |
| Junction to Ambient | $R_{thJA}$ | –      | 59   | –    | K/W  | 300 mm <sup>2</sup> PCB heat sink area <sup>2)</sup> | P_4.3.3 |
| Junction to Ambient | $R_{thJA}$ | –      | 49   | –    | K/W  | 600 mm <sup>2</sup> PCB heat sink area <sup>2)</sup> | P_4.3.4 |
| Junction to Ambient | $R_{thJA}$ | –      | 42   | –    | K/W  | 2s2p PCB <sup>3)</sup>                               | P_4.3.5 |

1) Not subject to production test, specified by design

2) Specified  $R_{thJA}$  value is according to Jedec JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm<sup>3</sup> board with 1 copper layer (1 × 70μm Cu).

3) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm<sup>3</sup> board with 2 inner copper layers (2 × 70μm Cu, 2 × 35μm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

## 5 Voltage Regulator

### 5.1 Description Voltage Regulator

The output voltage  $V_Q$  is controlled by comparing the feedback voltage ( $V_{ADJ}$ ) to an internal reference voltage and driving a PNP pass transistor accordingly. The control loop stability depends on the output capacitor  $C_Q$ , the output capacitor ESR, the load current and the chip temperature. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in the [Table 2 "Functional Range" on Page 7](#) have to be maintained. For stability details please refer to the typical performance graph "Output Capacitor Series Resistivity  $ESR_{CQ}$ " on [Page 11](#). In addition the output capacitor may need to be sized larger to buffer load transients.

An input capacitor  $C_I$  is not needed for the control loop stability, but recommended to buffer line influences. Connect the capacitors close to the IC terminals. In general a buffered supply voltage is recommended for the device. For details see [Chapter 9.1](#).

Protection circuitry prevents the IC as well as the application from destruction in case of catastrophic events. The integrated safeguards consist of output current limitation, reverse polarity protection as well as thermal shutdown in case of overtemperature.

In order to avoid excessive power dissipation that could never be handled by the pass element and the package, an integrated safe operation monitor lowers the maximum output current input voltages above  $V_{BAT} = 22\text{ V}$ .

The thermal shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to a cycling behavior of the output voltage until the fault is removed. However, junction temperatures above  $150\text{ °C}$  are outside the maximum ratings and therefore significantly reduce the IC lifetime.

The TLF4277-2 allows a negative supply voltage. However, several small currents are flowing into the IC increasing its junction temperature. This reverse current has to be considered for the thermal design, respecting that the thermal protection circuit is not operating during reverse polarity condition.

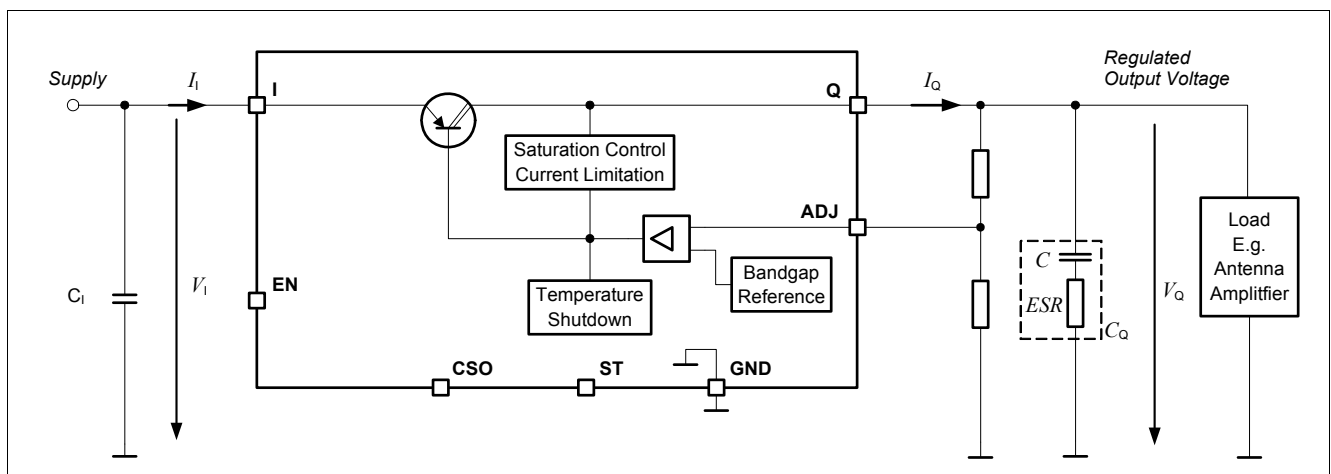


Figure 3 Block Diagram Voltage Regulator Circuit



## 5.2 Electrical Characteristics Voltage Regulator

**Table 4 Electrical Characteristics: Voltage Regulator**

$V_{BAT} = 13.5 \text{ V}$ ,  $T_j = -40 \text{ }^{\circ}\text{C}$  to  $+150 \text{ }^{\circ}\text{C}$ , all voltages with respect to ground, direction of currents as shown in [Figure 9.1 "Application Diagram" on Page 20](#) (unless otherwise specified)

| Parameter                                     | Symbol        | Values |      |      | Unit               | Note / Test Condition                                                                                                                                                           | Number   |
|-----------------------------------------------|---------------|--------|------|------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
|                                               |               | Min.   | Typ. | Max. |                    |                                                                                                                                                                                 |          |
| Reference Voltage                             | $V_{REF,int}$ | —      | 1.19 | —    | V                  | <sup>1)</sup> —                                                                                                                                                                 | P_5.2.1  |
| Output Voltage Tolerance <sup>2)</sup>        | $V_Q$         | -2     | —    | 2    | %                  | $1 \text{ mA} \leq I_Q \leq 300 \text{ mA}$ ;<br>$9 \text{ V} \leq V_{BAT} \leq 16 \text{ V}$<br>$5 \text{ V} \leq V_Q \leq 12 \text{ V}$ with<br>$V_{BAT} > V_Q + 2 \text{ V}$ | P_5.2.2  |
| Output Voltage Tolerance                      | $V_Q$         | -2     | —    | 2    | %                  | $1 \text{ mA} \leq I_Q \leq 150 \text{ mA}$ ;<br>$6 \text{ V} \leq V_{BAT} \leq 16 \text{ V}$<br>$5 \text{ V} \leq V_Q \leq 12 \text{ V}$ with<br>$V_{BAT} > V_Q + 1 \text{ V}$ | P_5.2.3  |
| Output Voltage Tolerance                      | $V_Q$         | -2     | —    | 2    | %                  | $1 \text{ mA} \leq I_Q \leq 100 \text{ mA}$ ;<br>$16 \text{ V} \leq V_{BAT} \leq 32 \text{ V}^{3)}$<br>$5 \text{ V} \leq V_Q \leq 12 \text{ V}$                                 | P_5.2.4  |
| Output Voltage Tolerance                      | $V_Q$         | -2     | —    | 2    | %                  | $1 \text{ mA} \leq I_Q \leq 10 \text{ mA}$ ;<br>$32 \text{ V} \leq V_{BAT} \leq 40 \text{ V}^{3)}$<br>$5 \text{ V} \leq V_Q \leq 12 \text{ V}$                                  | P_5.2.5  |
| Load Regulation steady-state                  | $dV_{Q,load}$ | -30    | -5   | —    | mV                 | $I_Q = 1 \text{ mA}$ to $250 \text{ mA}$ ;<br>$V_{BAT} = 6 \text{ V}$ ; $V_Q = 5 \text{ V}$                                                                                     | P_5.2.7  |
| Line Regulation steady-state                  | $dV_{Q,line}$ | —      | 5    | 20   | mV                 | $V_{BAT} = 6 \text{ V}$ to $32 \text{ V}$ ;<br>$I_Q = 5 \text{ mA}$ ; $V_Q = 5 \text{ V}$                                                                                       | P_5.2.8  |
| Power Supply Ripple Rejection <sup>1)</sup>   | $PSRR$        | 60     | 65   | —    | dB                 | $f_{ripple} = 100 \text{ Hz}$ ;<br>$V_{ripple} = 1 \text{ Vpp}$ ;<br>$V_Q = 5 \text{ V}$ ;<br>$I_Q < 100 \text{ mA}$                                                            | P_5.2.9  |
| Dropout Voltage<br>$V_{dr} = V_I - V_Q$       | $V_{dr}$      | —      | 100  | 250  | mV                 | $I_Q = 100 \text{ mA}^{4)}$<br>$V_Q = 5 \text{ V}$                                                                                                                              | P_5.2.10 |
| Dropout Voltage<br>$V_{dr} = V_I - V_Q$       | $V_{dr}$      | —      | 200  | 500  | mV                 | $I_Q = 200 \text{ mA}^{4)}$<br>$V_Q = 5 \text{ V}$                                                                                                                              | P_5.2.11 |
| Output Current Limitation                     | $I_{Q,max}$   | 301    | —    | 700  | mA                 | $0 \text{ V} \leq V_Q \leq 0.95 \cdot V_{Q,nom}$                                                                                                                                | P_5.2.13 |
| Reverse Current                               | $I_Q$         | -2     | -1   | —    | mA                 | $V_{BAT} = 0 \text{ V}$ ; $V_Q = 5 \text{ V}$                                                                                                                                   | P_5.2.14 |
| Reverse Current at Negative Input Voltage     | $I_{BAT}$     | -10    | -6   | —    | mA                 | $V_{BAT} = -16 \text{ V}$ ; $V_Q = 0 \text{ V}$                                                                                                                                 | P_5.2.15 |
| Overtemperature Shutdown Threshold            | $T_{j,sd}$    | 151    | —    | 200  | $^{\circ}\text{C}$ | $T_j$ increasing <sup>1)</sup>                                                                                                                                                  | P_5.2.16 |
| Overtemperature Shutdown Threshold Hysteresis | $T_{j,hy}$    | —      | 15   | —    | K                  | $T_j$ decreasing <sup>1)</sup>                                                                                                                                                  | P_5.2.17 |

1) Parameter not subject to production test; specified by design.

2) Referring to the device tolerance only, the tolerance of the resistor divider can cause additional deviation.

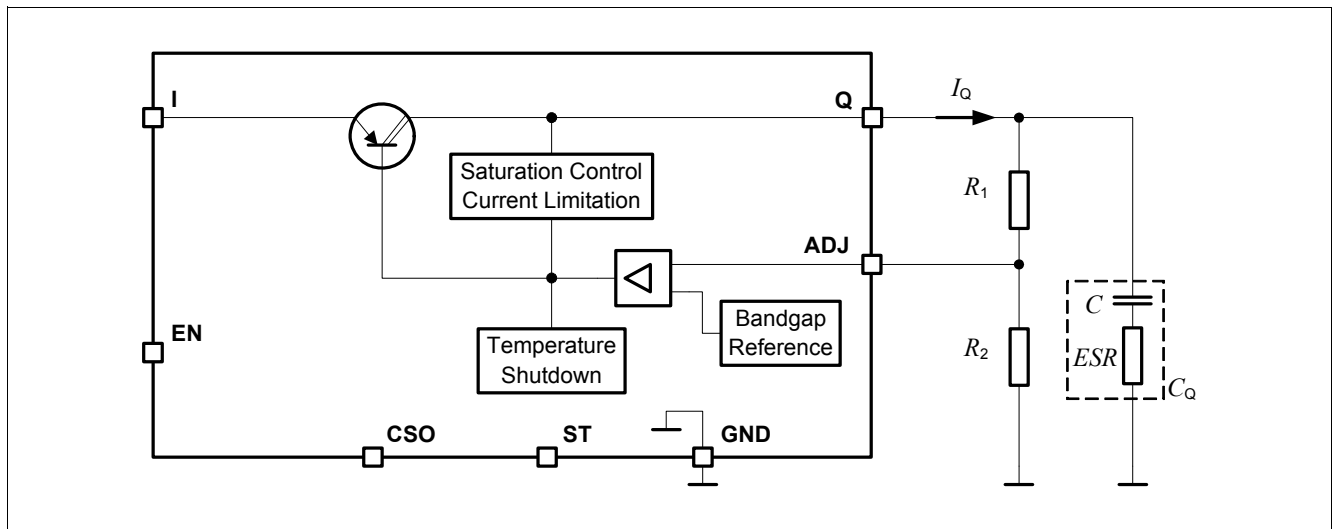
3) See typical performance graph for details.

4) Measured when the output voltage  $V_Q$  has dropped 100 mV from its nominal value.

### 5.3 Application Information for setting the variable output voltage

The output voltage of the TLF4277-2 can be adjusted between 5 V and 12 V by an external output voltage divider, closing the control loop to the voltage adjust pin ADJ.

The voltage at pin ADJ is compared to the internal reference of typical 1.19 V in an error amplifier. It controls the output voltage.



**Figure 4 Application Detail External Components at Output for Variable Voltage Regulator**

The output voltage is calculated according to [Equation \(1\)](#):

$$V_Q = (R_1 + R_2)/R_2 \times V_{REF,int}, \text{ neglecting } I_{ADJ} \quad (1)$$

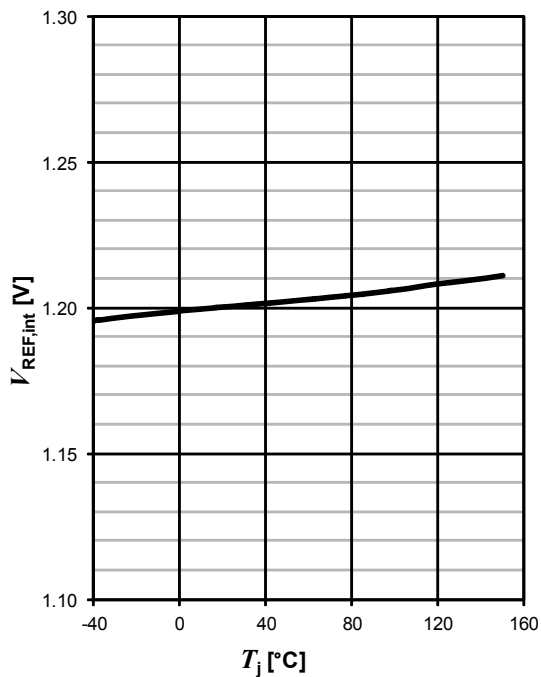
$V_{REF,int}$  is typically 1.19 V.

To avoid errors caused by leakage current  $I_{ADJ}$ , we recommend to choose the resistor value for  $R_2 < 27 \text{ k}\Omega$ .

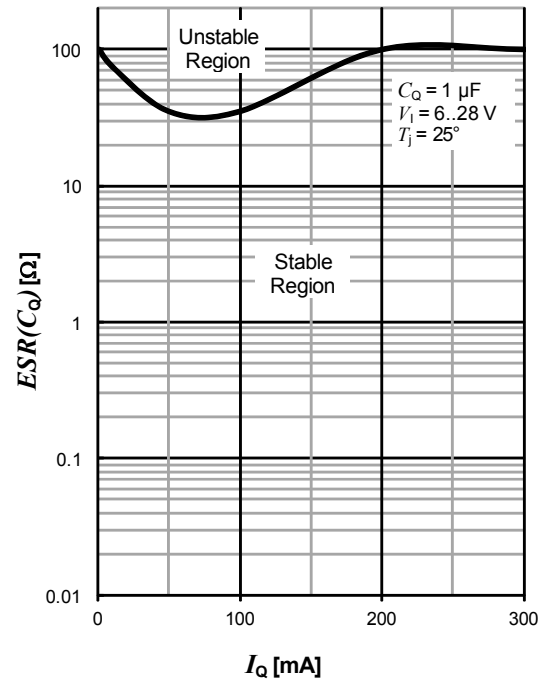
The accuracy of the resistors for the external voltage divider can lead to a higher tolerance of the output voltage. To achieve a reasonable accuracy resistors with a tolerance of 1% or lower are recommended for the feedback divider.

## 5.4 Typical Performance Characteristics Voltage Regulator

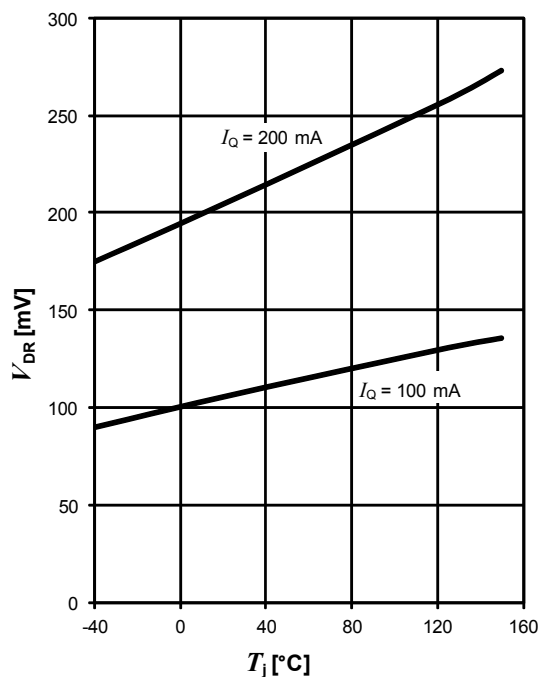
Reference Voltage  $V_{REF,int}$  vs.  
Junction Temperature  $T_j$



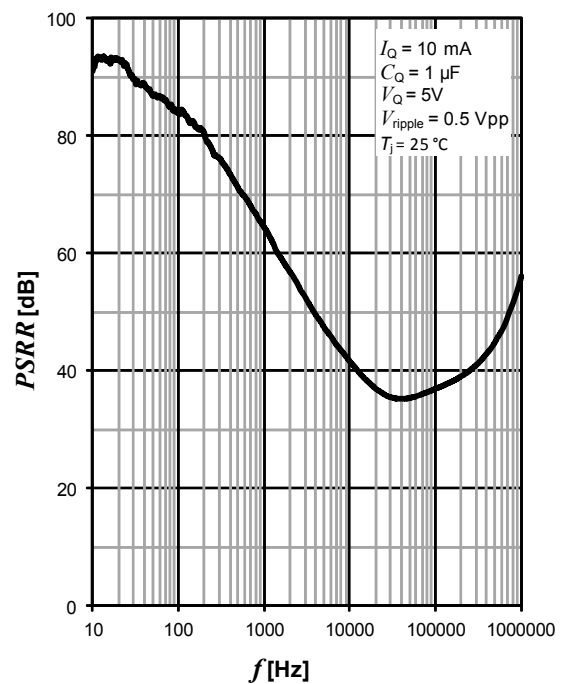
Output Capacitor Series Resistivity  $ESR_{CQ}$   
vs. Output Current  $I_Q$



Dropout Voltage  $V_{DR}$  vs.  
Junction Temperature  $T_j$



Power Supply Ripple Rejection  $PSRR$



## 6 Current Consumption

### 6.1 Electrical Characteristics Current Consumption

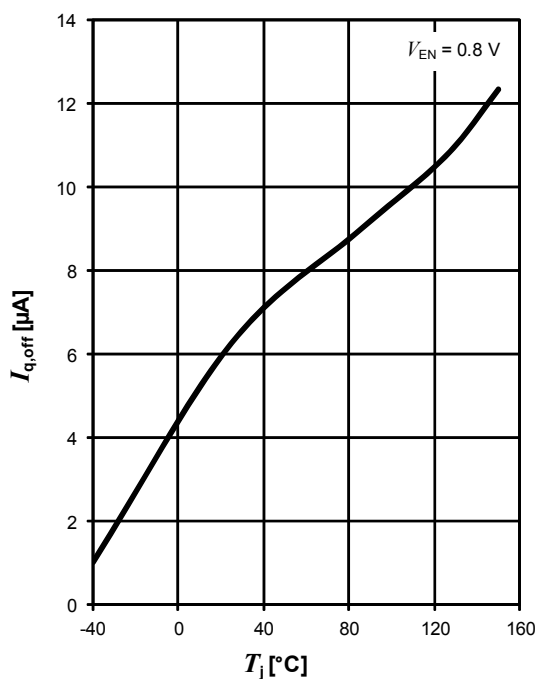
**Table 5 Electrical Characteristics: Current Consumption**

$V_{BAT} = 13.5 \text{ V}$ ,  $T_j = -40 \text{ }^{\circ}\text{C}$  to  $+150 \text{ }^{\circ}\text{C}$ , all voltages with respect to ground; direction of currents as shown in [Figure 9.1 "Application Diagram" on Page 20](#) (unless otherwise specified)

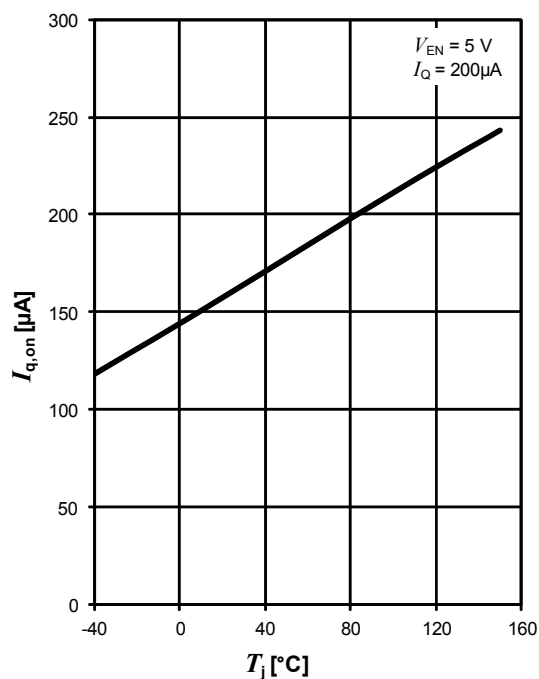
| Parameter           | Symbol      | Values |      |      | Unit          | Note / Test Condition                                                                                                         | Number  |
|---------------------|-------------|--------|------|------|---------------|-------------------------------------------------------------------------------------------------------------------------------|---------|
|                     |             | Min.   | Typ. | Max. |               |                                                                                                                               |         |
| Current Consumption | $I_{q,on}$  | –      | 150  | 200  | $\mu\text{A}$ | $I_Q \leq 200 \mu\text{A}$ ; $T_j \leq 25 \text{ }^{\circ}\text{C}$ ;<br>$V_{EN} = 5 \text{ V}$ ; $I_q = I_I - I_Q - I_{CSO}$ | P_6.1.1 |
| Current Consumption | $I_{q,on}$  | –      | –    | 250  | $\mu\text{A}$ | $I_Q \leq 200 \mu\text{A}$ ; $T_j \leq 85 \text{ }^{\circ}\text{C}$ ;<br>$V_{EN} = 5 \text{ V}$ ; $I_q = I_I - I_Q - I_{CSO}$ | P_6.1.2 |
| Current Consumption | $I_{q,on}$  | –      | 1.2  | 2.6  | $\text{mA}$   | $I_Q = 50 \text{ mA}$ ; $V_{EN} = 5 \text{ V}$ ;<br>$I_q = I_I - I_Q - I_{CSO}$                                               | P_6.1.3 |
| Current Consumption | $I_{q,on}$  | –      | 5.5  | 11   | $\text{mA}$   | $I_Q = 200 \text{ mA}$ ; $V_{EN} = 5 \text{ V}$ ;<br>$I_q = I_I - I_Q - I_{CSO}$                                              | P_6.1.4 |
| Current Consumption | $I_{q,off}$ | –      | –    | 3    | $\mu\text{A}$ | $T_j \leq 25 \text{ }^{\circ}\text{C}$ ; $V_{EN} = 0 \text{ V}$<br>$I_q = I_I - I_Q$                                          | P_6.1.5 |
| Current Consumption | $I_{q,off}$ | –      | –    | 5    | $\mu\text{A}$ | $T_j \leq 85 \text{ }^{\circ}\text{C}$ ; $V_{EN} = 0 \text{ V}$<br>$I_q = I_I - I_Q$                                          | P_6.1.6 |
| Current Consumption | $I_{q,off}$ | –      | –    | 15   | $\mu\text{A}$ | $T_j \leq 85 \text{ }^{\circ}\text{C}$ ; $V_{EN} = 0.8 \text{ V}$<br>$I_q = I_I - I_Q$                                        | P_6.1.7 |

## 6.2 Typical Performance Graphs Current Consumption

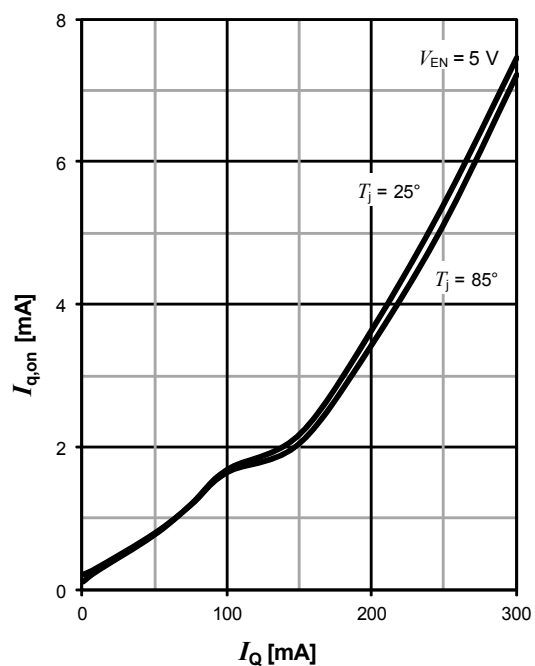
Current Consumption  $I_{q,off}$  vs.  
Junction Temperature  $T_j$



Current Consumption  $I_{q,on}$  vs.  
Junction Temperature  $T_j$



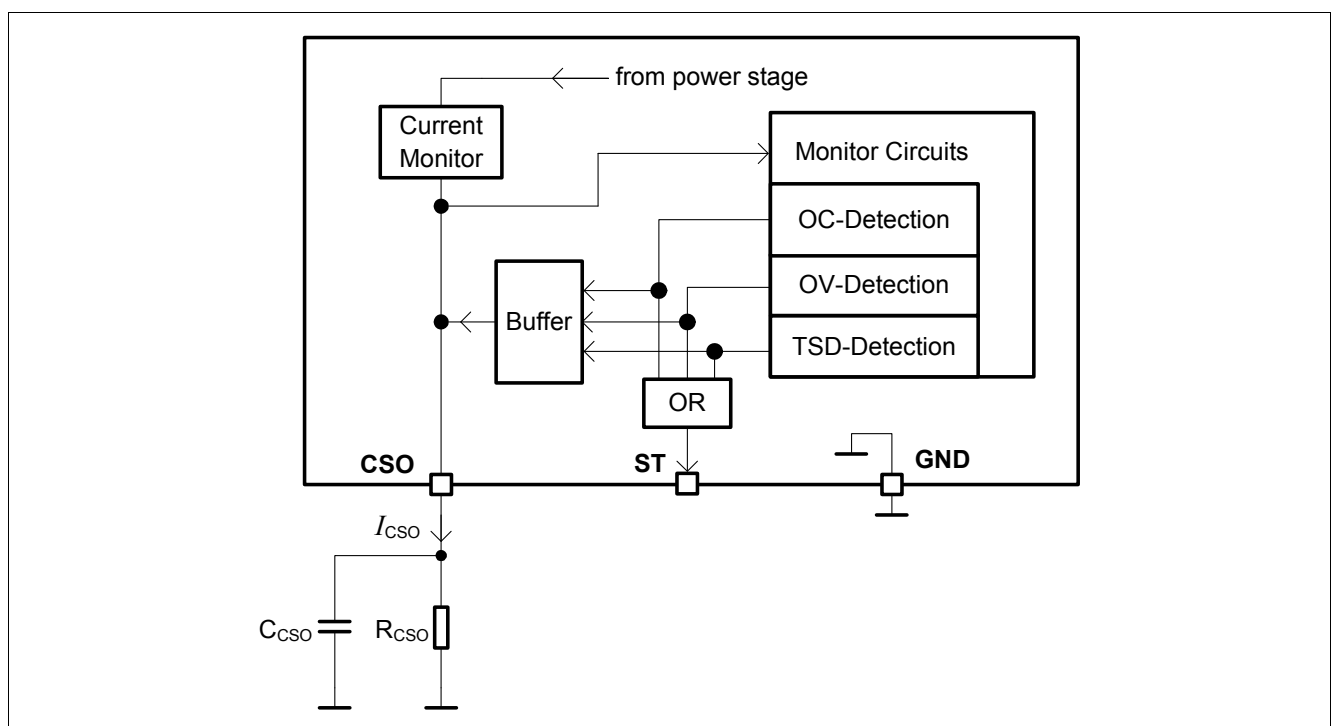
Current Consumption  $I_{q,on}$  vs.  
Output Current  $I_Q$



## 7 Current and Protection Monitor Functions

### 7.1 Functional Description Current and Protection Monitors

The TLF4277-2 provides a set of advanced monitor functionality. The current flowing out of the power stage can be monitored at the CSO output. In addition the current limitation can be adjusted via external resistor. Events of the implemented protection functions are reported through dedicated voltage levels at the CSO output. This information can be processed by an external  $\mu\text{C}$  for system analysis and failure identification. The monitored events are over-current, overvoltage, and temperature shutdown. In addition all three fault conditions are routed also to the digital output pin ST.



**Figure 5** Block diagram current and protection monitor

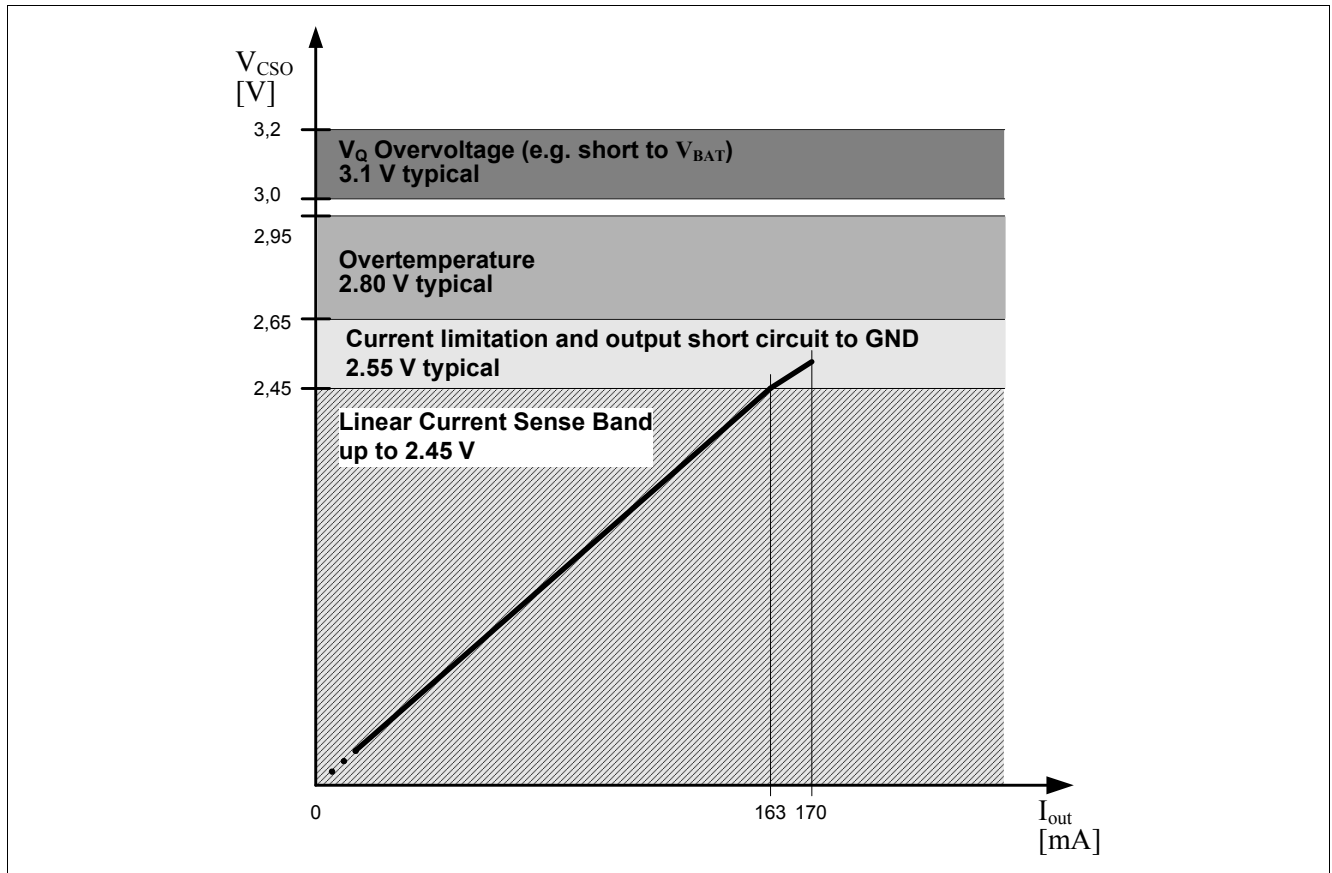
To reduce possible effects from the supply voltage  $V_{\text{BAT}}$  additional filtering of the supply voltage is recommended. A 100 nF capacitor should be placed as close as possible to the IC terminal, which is connected to  $V_{\text{BAT}}$ .

**Figure 6** shows the output level at the CSO pin versus the operation or fault condition. The graph is valid for the following set up of external components:

$$C_{\text{CSO}} = 2.2 \mu\text{F}$$

$$R_{\text{CSO}} = 1.5 \text{ k}\Omega$$

*Note: In case of high input voltage ( $V_I > 20 \text{ V}$ ), high junction temperature ( $T_j > 151^\circ\text{C}$ ) and CSO pin is directly connected to GND without resistor, the return to normal operation from the "thermal shutdown mode" can't be ensured.*



**Figure 6** Output levels and functionality of the CSO output

*Note:* The graph is just an example and only valid for an certain configuration of the external components.

### 7.1.1 Linear Current Monitor

Inside the linear current monitor area the current driven out of the CSO pin is direct proportional to the output current ( $I_Q$ ).

The level of the current  $I_{CSO}$  can be calculated according to [Equation \(2\)](#):

(2)

$$I_{CSO} = \frac{I_Q}{F_{I_Q/CSO}}$$

### 7.1.2 Adjustable Output Current Limitation

The TLF4277-2 has an adjustable current limitation for the current flowing out of the power stage. If the level of the output current exceeds the defined current limit threshold ( $I_{Q,lim}$ ), the output current of the TLF4277-2 will be limited.

Setting of the adjustable current limitation: (3)

$$I_{Q,lim} = \frac{2.55V \times F_{I_{Q/CSO}}}{R_{CSO}}$$

A voltage level as defined in **“CSO Voltage Level” on Page 17** will be applied at the CSO pin. In addition the ST pin will be set low.

*Note: During power up of the device, the regulator works in output current limitation. Regardless if the output current is limited by the protection function according to **“Output Current Limitation” on Page 9**, or by the adjustable output current limitation according to **“Adjustable Current Limit” on Page 17**. If an adjustable current limit is set, the status output pin ST is set to low as long as the adjustable current limitation is active during power up sequence.*

Example: To achieve a current limitation of e.g. 170mA the following configuration can be used:

$$I_{Q,lim} = \frac{2.55V \times 100}{1.5k\Omega} = 170mA$$

$$F_{I_{Q/CSO}} = 100$$

$$R_{CSO} = 1.5 k\Omega$$

### 7.1.3 Overvoltage Detection

To detect a possible short circuit of the output to a higher supply rail the TLF4277-2 has an overvoltage detection implemented. An overvoltage will be detected, if the voltage level at the ADJ pin is 20% higher than the internal reference voltage  $V_{REF,int}$  defined in **“Reference Voltage” on Page 9**.

In case of overvoltage the CSO pin will set to a voltage level as defined in **“CSO Voltage Level” on Page 17**. In addition the ST pin will be set low.

### 7.1.4 Thermal Shutdown Detection

If the junction temperature will exceed the limits defined in the **“Overtemperature Shutdown Threshold” on Page 9** the TLF4277-2 will disable the output voltage. In this case a voltage level as defined in **“CSO Voltage Level” on Page 17** will be applied at the CSO pin. In addition the ST pin will be set low.

### 7.1.5 Status Output Signal

The status condition pin ST is an open collector output. An external pull-up resistor has to be applied for functionality and to limit the current into the pin (e.g. connect via a resistor to “Q”). Connecting the ST pin directly to a supply voltage may damage the device.

Is one or more of the monitored protection functions (over-current, overvoltage and temperature shutdown) activated, the digital Status Output pin ST is set to “low”.



## Current and Protection Monitor Functions

**Table 6 Electrical Characteristics: Current Monitor Function**

$V_{BAT} = 13.5 \text{ V}$ ,  $T_j = -40 \text{ }^{\circ}\text{C}$  to  $+150 \text{ }^{\circ}\text{C}$ , all voltages with respect to ground, direction of currents as shown in **Figure 9.1 "Application Diagram" on Page 20** (unless otherwise specified)

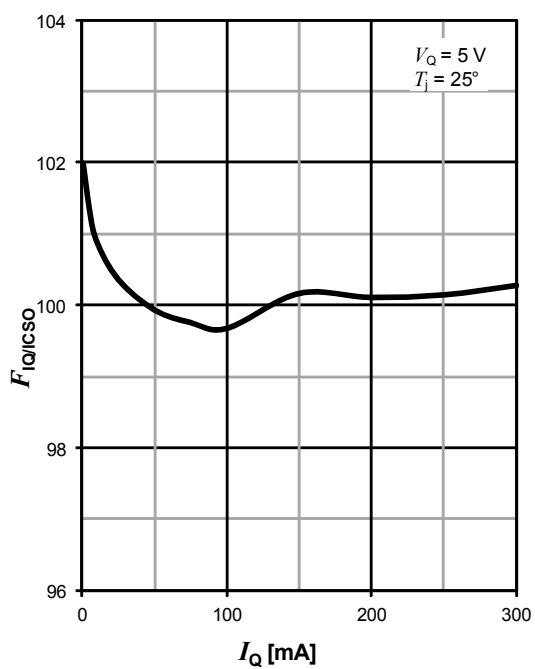
| Parameter                                                                                        | Symbol              | Values |      |      | Unit | Note / Test Condition                                                                                                                                                         | Number   |
|--------------------------------------------------------------------------------------------------|---------------------|--------|------|------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
|                                                                                                  |                     | Min.   | Typ. | Max. |      |                                                                                                                                                                               |          |
| Linear Current Monitor                                                                           |                     |        |      |      |      |                                                                                                                                                                               |          |
| Current Monitor Factor<br>Factor = $I_Q / I_{CSO}$<br>( $I_Q = 10 \text{ mA} - 150 \text{ mA}$ ) | $F_{I_{Q/I_{CSO}}}$ | 95     | 100  | 105  | –    | $T_j = -40^{\circ} \text{ to } 125^{\circ}\text{C}$<br>$V_{IN} = 9 \text{ V to } 16 \text{ V}$<br>$V_Q = 5 \text{ V to } 12 \text{ V}$<br>$V_{IN} > V_Q + 2.0 \text{ V}^{1)}$ | P_7.1.1  |
| Current Monitor Factor<br>Factor = $I_Q / I_{CSO}$                                               | $F_{I_{Q/I_{CSO}}}$ | 90     | 100  | 110  | –    | $1 \text{ mA} \leq I_Q \leq 300 \text{ mA}$<br>$V_Q = 5 \text{ V}$                                                                                                            | P_7.1.5  |
| CSO current at no load condition                                                                 | $I_{CSO,off}$       | –      | –    | 550  | nA   | no load connected at Q<br>$R_2 = 27 \text{ k}\Omega$<br>$V_Q = 5 \text{ V}$                                                                                                   | P_7.1.6  |
| Adjustable Current Limitation                                                                    |                     |        |      |      |      |                                                                                                                                                                               |          |
| Adjustable Current Limit<br>Range                                                                | $I_{Q,lim}$         | 10     | -    | 300  | mA   | $850 \Omega < R_{CSO} < 25.5 \text{ k}\Omega$<br>$V_Q < 0,95 * V_{Q,nom}^{1)}$                                                                                                | P_7.1.7  |
| Adjustable Current Limit<br>Tolerance                                                            | $I_{Q,lim}$         | -10    | –    | 10   | %    | $10 \text{ mA} \leq I_{Q,lim} \leq 300 \text{ mA}$<br>$T_j = -40^{\circ} \text{ to } 125^{\circ}\text{C}$<br>$0.95 * V_{Q,nom} > V_Q > 3.0 \text{ V}$                         | P_7.1.8  |
| Adjustable Current Limit<br>Tolerance                                                            | $I_{Q,lim}$         | -10    | –    | 25   | %    | $10 \text{ mA} \leq I_{Q,lim} \leq 300 \text{ mA}$<br>$T_j = -40^{\circ} \text{ to } 125^{\circ}\text{C}$<br>$0.95 * V_{Q,nom} > V_Q > 0 \text{ V}$                           | P_7.1.15 |
| CSO Voltage Level<br>Current limitation                                                          | $V_{CSO,cur\_lim}$  | 2.45   | 2.55 | 2.65 | V    | $V_Q < 0,95 * V_{Q,nom}^{1)}$                                                                                                                                                 | P_7.1.9  |
| Output Level Overvoltage Detected                                                                |                     |        |      |      |      |                                                                                                                                                                               |          |
| CSO Voltage Level<br>Overvoltage detected                                                        | $V_{CSO,ov}$        | 3.0    | 3.1  | 3.2  | V    | $V_{ADJ} > 1.2 * V_{REF,nom}^{1)}$                                                                                                                                            | P_7.1.10 |
| Output Level Overtemperature Detected                                                            |                     |        |      |      |      |                                                                                                                                                                               |          |
| CSO Voltage Level<br>Overtemperature Detected <sup>2)</sup>                                      | $V_{CSO,TSD}$       | 2.65   | 2.8  | 2.95 | V    | $151^{\circ}\text{C} < T_j < 180^{\circ}\text{C}$                                                                                                                             | P_7.1.12 |
| Status Output Signal                                                                             |                     |        |      |      |      |                                                                                                                                                                               |          |
| Status Output Digital Signal<br>Low Voltage                                                      | $V_{ST,low}$        | –      | 0.2  | 0.4  | V    | $I_{ST} \leq 1.8 \text{ mA}$                                                                                                                                                  | P_7.1.13 |
| Status Output Digital Signal<br>Sink current                                                     | $I_{ST}$            | –      | –    | 1.8  | mA   | –                                                                                                                                                                             | P_7.1.14 |

1) Referring to the device tolerance only, the tolerance of the external components can cause additional deviation

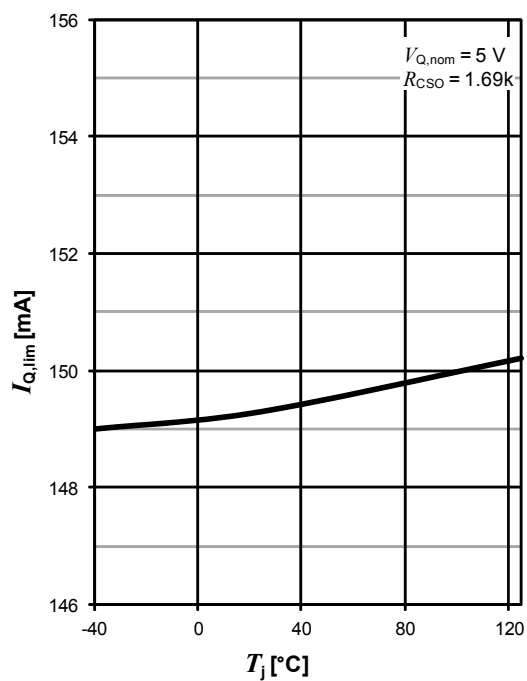
2) Specified by design; not subject to production test

### 7.1.6 Typical Performance Graphs Current Monitor

Current Monitor Factor  $F_{I_Q/ICSO}$  vs.  
Output Current  $I_Q$



External Current Limitation  $I_{Q,lim}$  vs.  
Junction Temperature  $T_j$



## 8 Enable Function

### 8.1 Description Enable Function

The TLF4277-2 can be turned on or turned off via the EN Input. With voltage levels higher than  $V_{EN,high}$  applied to the EN Input the device will be completely turned on. A voltage level lower than  $V_{EN,low}$  sets the device to low quiescent current mode. In this condition the device is turned off and is not functional. The Enable Input has a build in hysteresis to avoid toggling between ON/OFF state, if signals with slow slope are applied to the input. Enable input pin has an internal pull down resistor.

### 8.2 Electrical Characteristics Enable Function

**Table 7 Electrical Characteristics: Enable Function**

$V_{BAT} = 13.5 \text{ V}$ ,  $T_j = -40 \text{ °C}$  to  $+150 \text{ °C}$ , all voltages with respect to ground, direction of currents as shown in [Figure 9.1 "Application Diagram" on Page 20](#) (unless otherwise specified)

| Parameter                          | Symbol        | Values |      |      | Unit | Note / Test Condition                                                                                                                                                               | Number  |
|------------------------------------|---------------|--------|------|------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
|                                    |               | Min.   | Typ. | Max. |      |                                                                                                                                                                                     |         |
| Enable Low Signal Valid            | $V_{EN,low}$  | –      | –    | 0.8  | V    | –                                                                                                                                                                                   | P_8.2.1 |
| Enable High Signal Valid           | $V_{EN,high}$ | 2      | –    | –    | V    | see also startup time P_8.2.7                                                                                                                                                       | P_8.2.2 |
| Enable Threshold Hysteresis        | $V_{EN,hyst}$ | 50     | –    | –    | mV   | –                                                                                                                                                                                   | P_8.2.3 |
| Enable Input current               | $I_{EN,high}$ | –      | –    | 5    | μA   | $V_{EN} = 5 \text{ V}$                                                                                                                                                              | P_8.2.4 |
| Enable Input current               | $I_{EN,high}$ | –      | –    | 20   | μA   | $V_{EN} < 18 \text{ V}$                                                                                                                                                             | P_8.2.5 |
| Enable internal pull-down resistor | $R_{EN}$      | 0.94   | 1.5  | 2.5  | MΩ   | $V_{EN} < 5 \text{ V}$                                                                                                                                                              | P_8.2.6 |
| Startup time                       | $t_{EN}$      | –      | 180  | –    | μs   | $C_Q = 1 \text{ μF}$ ; $V_{Q,nom} = 5 \text{ V}$ ; $I_{Q,load} = 150 \text{ mA}$ ; time from $V_{EN} > 2 \text{ V}$ (0 V to 5 V transition) till $V_Q = 90 \text{ % of } V_{Q,nom}$ | P_8.2.7 |

## 9 Application Information

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

### 9.1 Application Diagram

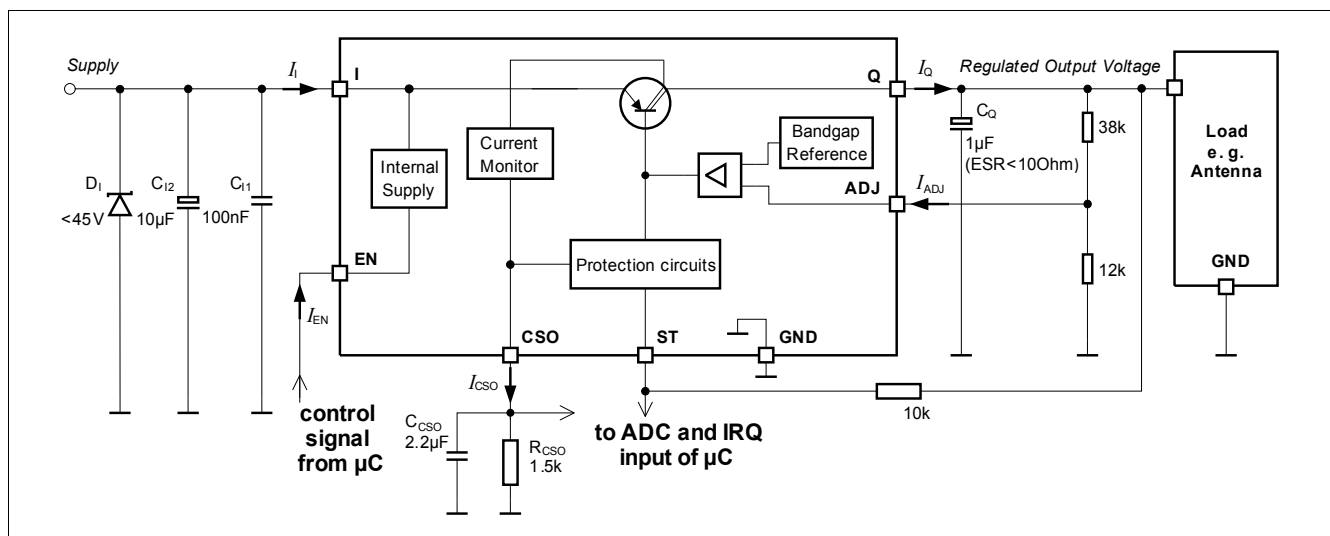


Figure 7 Application Diagram

### 9.2 Selection of External Components

#### 9.2.1 Input Pin

The typical input circuitry for a linear voltage regulator is shown in the application diagram above.

A ceramic capacitor at the input, in the range of 100nF to 470nF, is recommended to filter out the high frequency disturbances imposed by the line e.g. ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10µF to 470µF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to over-voltage above 45 V.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in order to protect the voltage regulator against external disturbances and damages.

#### 9.2.2 Output Pin

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in [“Functional Range” on Page 7](#). The graph [“Output Capacitor Series Resistivity ESR<sub>CQ</sub> vs. Output Current I<sub>Q</sub>” on Page 11](#) shows the stable operation range of the device.

TLF4277-2 is designed to be stable with extremely low ESR capacitors. According to the automotive requirements, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator's output and GND pins and on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application that the output stability requirements are fulfilled.

### 9.3 Thermal Considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q \quad (4)$$

with

- $P_D$ : continuous power dissipation
- $V_I$ : input voltage
- $V_Q$ : output voltage
- $I_Q$ : output current
- $I_q$ : quiescent current

The maximum acceptable thermal resistance  $R_{thJA}$  can then be calculated:

$$R_{thJA,max} = (T_{j,max} - T_a) / P_D \quad (5)$$

with

- $T_{j,max}$ : maximum allowed junction temperature
- $T_a$ : ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in ["Thermal Resistance" on Page 7](#).

#### Example

Application conditions:

$$V_I = 13.5V$$

$$V_Q = 5V$$

$$I_Q = 100mA$$

$$T_a = 85^\circ C$$

Calculation of  $R_{thJA,max}$ :

$$\begin{aligned} P_D &= (V_I - V_Q) \times I_Q + V_I \times I_q \\ &= (13.5V - 5V) \times 100mA + 13.5V \times 5.0mA \\ &= 0.850W + 0.068W \\ &= 0.918W \end{aligned}$$

$$\begin{aligned} R_{thJA,max} &= (T_{j,max} - T_a) / P_D \\ &= (150^\circ C - 85^\circ C) / 0.918W = 70.8K/W \end{aligned}$$

As a result, the PCB design must ensure a thermal resistance  $R_{thJA}$  lower than 70.8 K/W. According to **“Thermal Resistance” on Page 7**, at least 300 mm<sup>2</sup> heatsink area is needed on the FR4 1s0p PCB, or the FR4 2s2p board can be used.

#### 9.4 Reverse Polarity Protection

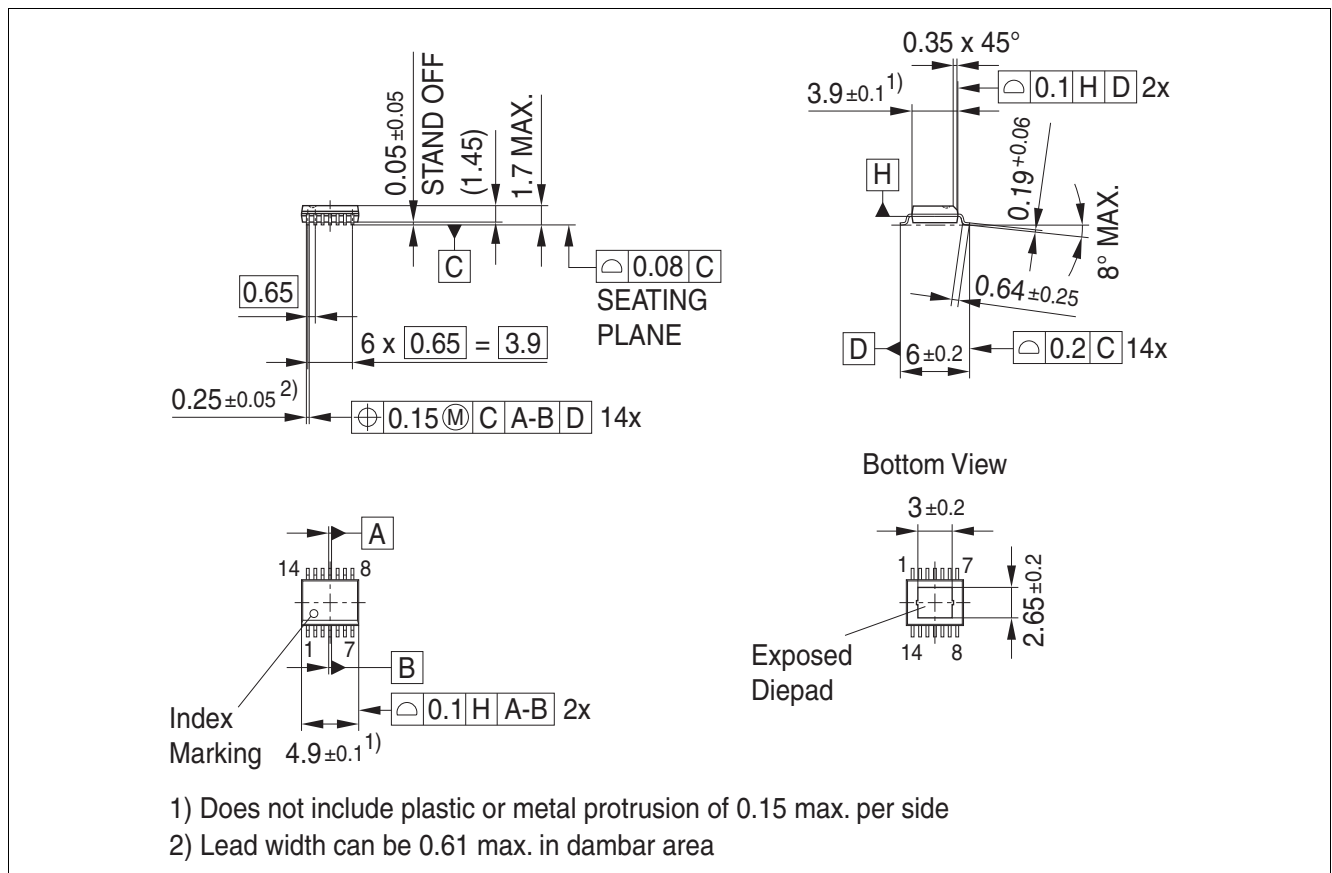
TLF4277-2 is self protected against reverse polarity faults and allows negative supply voltage. External reverse polarity diode is not needed. However, the absolute maximum ratings of the device as specified in **“Absolute Maximum Ratings” on Page 6** must be kept.

The reverse voltage causes several small currents to flow into the IC hence increasing its junction temperature. As the thermal shut down circuitry does not work in the reverse polarity condition, designers have to consider this in their thermal design.

#### 9.5 Further Application Information

- For further information you may contact <http://www.infineon.com/>

## 10 Package Outlines



**Figure 8 PG-SSOP14 EP**

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

## 11 Revision History

| Revision | Date       | Changes         |
|----------|------------|-----------------|
| 1.0      | 2014-03-13 | Initial version |



**Edition 2014-03-13**

**Published by  
Infineon Technologies AG  
81726 Munich, Germany**

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