

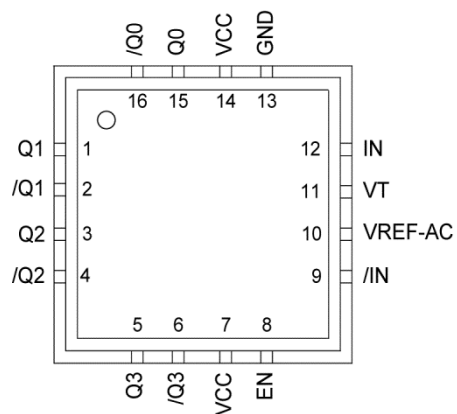
Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89833LMG	QFN-16	Industrial	833L with Pb-Free bar line indicator	NiPdAu Pb-Free
SY89833LMGTR ⁽²⁾	QFN-16	Industrial	833L with Pb-Free bar line indicator	NiPdAu Pb-Free

Note:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC Electricals only.
2. Tape and Reel.

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Function
15, 16 1, 2 3, 4 5, 6	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3	LVDS Differential (Outputs): Normally terminated with 100Ω across the pair (Q, /Q). See “LVDS Outputs” section, Figure 2a. Unused outputs should be terminated with a 100Ω resistor across each pair.
8	EN	This single-ended TTL/CMOS-compatible input functions as a synchronous output enable. The synchronous enable ensures that enable/disable will only occur when the outputs are in a logic LOW state. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state (enabled) if left open.
9, 12	/IN, IN	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-Coupled differential signals as small as 100mV. Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an intermediate state if left open. Please refer to the “Input Interface Applications” section for more details.
10	VREF-AC	Reference Voltage: These outputs bias to $V_{CC}-1.4V$. They are used when AC coupling the inputs (IN, /IN). For AC-Coupled applications, connect VREF-AC to VT pin and bypass with 0.01μF low ESR capacitor to V_{CC} . See “Input Interface Applications” section for more details. Maximum sink/source current is ±1.5mA. Due to the limited drive capability, each VREF-AC pin is only intended to drive its respective VT pin.
11	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT pins provide a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” section for more details.
13	GND	Ground. GND pins and exposed pad must be connected to the most negative potential of the device ground.
7, 14	VCC	Positive Power Supply: Bypass with 0.1μF//0.01μF low ESR capacitors and place as close to each VCC pin as possible.

Truth Tables

IN	/IN	EN	Q	/Q
0	1	1	0	1
1	0	1	1	0
X	X	0	0 ⁽³⁾	1 ⁽³⁾

Note:

3. On next negative transition of the input signal (IN).

Absolute Maximum Ratings⁽⁴⁾

Supply Voltage (V_{CC}) -0.5V to +4.0V
 Input Voltage (V_{IN}) -0.5 to $V_{CC} + 0.3V$
 LVDS Output Current (I_{OUT}) +10mA
 Input Current
 Source or Sink Current on (I_{VT}) $\pm 2mA$
 Maximum Operating Junction Temperature 125°C
 Lead Temperature (Soldering, 20 sec.) 260°C
 Storage Temperature (T_s) -65°C to +150°C

Operating Ratings⁽⁵⁾

Supply Voltage Range +3.0V to +3.6V
 Ambient Temperature (T_A) -40°C to +85°C
 Junction Thermal Resistance⁽⁶⁾
 QFN (θ_{JA})
 Still-Air 60°C/W
 QFN (ψ_{JB}) 33°C/W

Electrical Characteristics⁽⁷⁾

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage Range		3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC}		75	100	mA
R_{IN}	Input Resistance (IN-to-VT)		45	50	55	Ω
$R_{DIFF-IN}$	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input HIGH Voltage (IN-to-/IN)		0.1		$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage (IN-to-/IN)		-0.3		$V_{IH} - 0.1$	V
V_{IN}	Input Voltage Swing (IN-to-/IN)	Note 8, see Figure 2c.	0.1		V_{CC}	V
V_{DIFF_IN}	Differential Input Voltage	Note 8, see Figure 2d.	0.2			V
$ I_{IN} $	Input Current IN, /IN	Note 8.			45	mA
V_{REF-AC}	Reference Voltage		$V_{CC} - 1.525$	$V_{CC} - 1.425$	$V_{CC} - 1.325$	V

Notes:

- Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
- Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.
- The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
- Due to the internal termination (see "Input Buffer Structure" section) the input current depends on the applied voltages at IN, /IN and VT inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit!

LVDS Outputs DC Electrical Characteristics⁽⁹⁾

$V_{CC} = 3.3V \pm 10\%$, $R_L = 100\Omega$ across the outputs; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}	Output Voltage Swing	See Figure 2c.	250	325		mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 2d.	500	650		mV
V_{OCM}	Output Common Mode Voltage		1.125		1.275	V
ΔV_{OCM}	Change in Common Mode Voltage		-50		50	mV

LVTTTL/CMOS DC Electrical Characteristics⁽⁹⁾

$V_{CC} = 3.3V \pm 10\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage		0		0.8	V
I_{IH}	Input HIGH Current		-125		30	V
I_{IL}	Input LOW Current				-300	mV

Note:

9. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics⁽¹⁰⁾

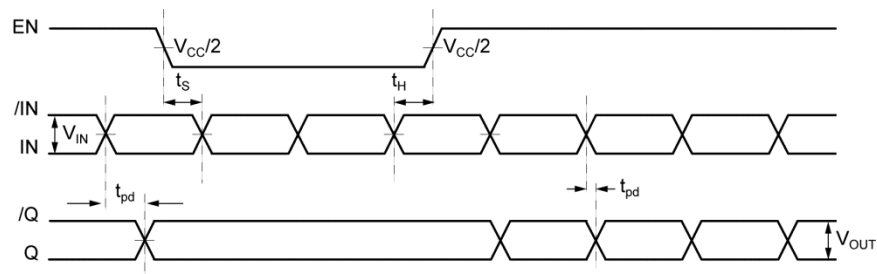
$V_{CC} = 3.3V \pm 10\%$, $R_L = 100\Omega$ across the outputs; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Frequency	$V_{OUT} \geq 200\text{mV}$	2.0			GHz
t_{pd}	Propagation Delay IN-to-Q	$V_{IN} < 400\text{mV}$	400	500	600	ps
		$V_{IN} \geq 400\text{mV}$	330	440	530	ps
t_{SKEW}	Within-Device Skew	Note 11		4	20	ps
	Part-to-Part Skew	Note 12			200	ps
t_S	Set-up Time EN to IN, /IN	Note 13	300			ps
t_H	Hold Time EN to IN, /IN	Note 13	500			ps
t_{JITTER}	Additive Jitter	Output = 622MHz Integration range: 12kHz – 20MHz		150		fs
t_r, t_f	Output Rise/Fall Times (20% to 80%)	At full output swing.	60	110	190	ps

Notes:

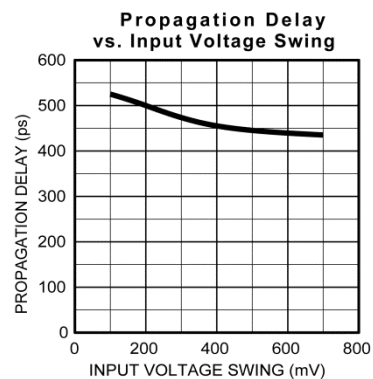
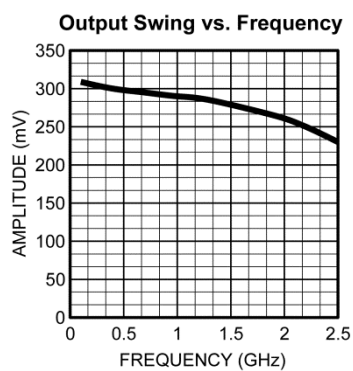
10. High-frequency AC parameters are guaranteed by design and characterization.
11. Within device skew is measured between two different outputs under identical input transitions.
12. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.
13. Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold times do not apply.

Timing Diagram



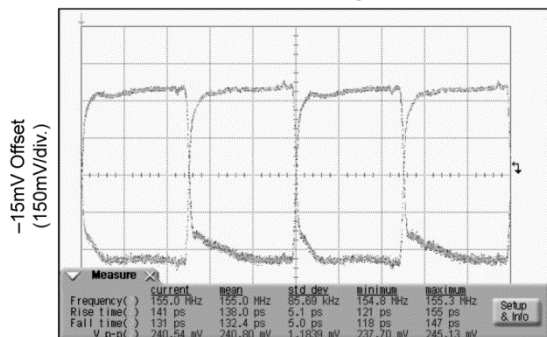
Typical Operating Characteristics

$V_{CC} = 3.3V$, $GND = 0V$, $V_{IN} = 400mV$, $R_L = 100\Omega$ across the outputs; $T_A = 25^\circ C$ unless otherwise stated.

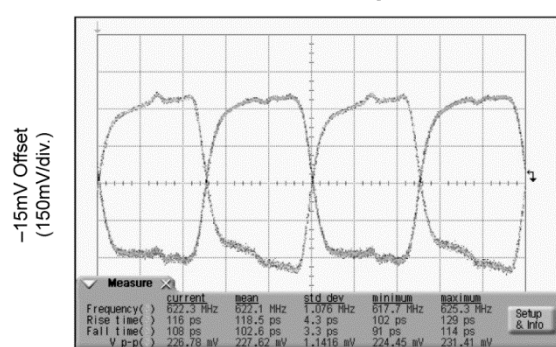


Functional Characteristics

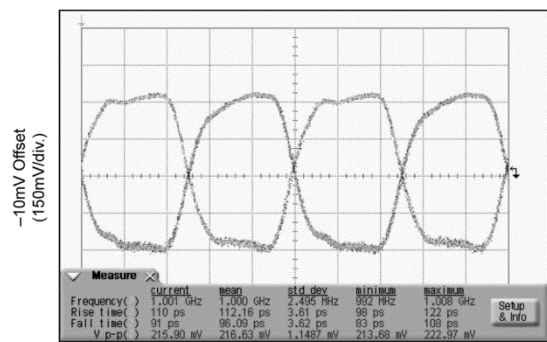
155MHz Output



622MHz Output

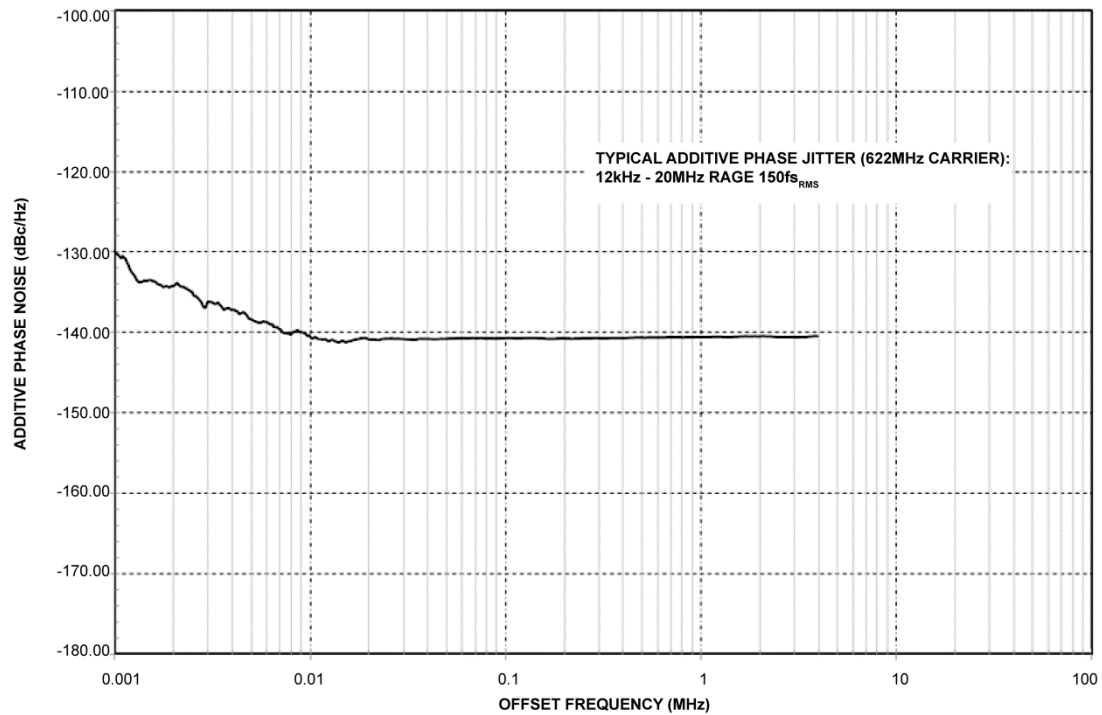


1GHz Output



Additive Phase Noise Plot

$V_{CC} = +3.3V$, $GND = 0$, $R_L = 50\Omega$ to $V_{CC}-2V$, $T_A = 25^\circ C$



Input Stage

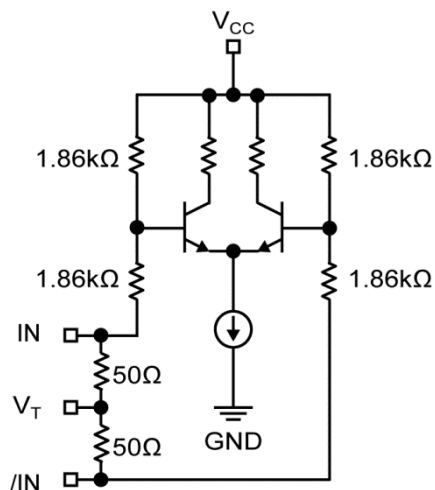


Figure 1. Simplified Differential Input Buffer

LVDS Outputs

LVDS specifies a small swing of 325mV typical, on a nominal 1.20V common mode above ground. The common mode voltage has tight limits to permit large variations in ground noise between a LVDS driver and receiver.

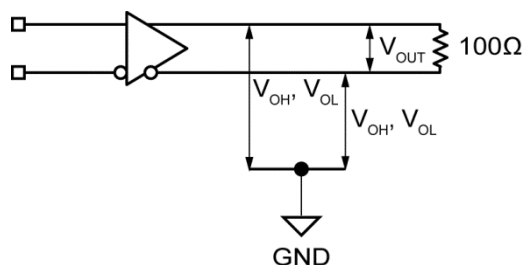


Figure 2. LVDS Differential Measurement

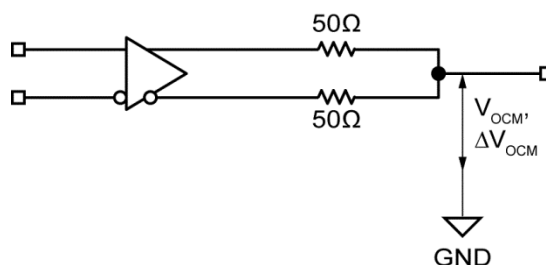


Figure 3. LVDS Common Mode Measurement

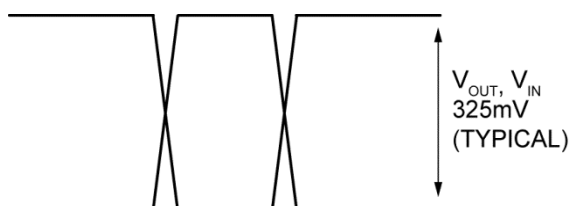


Figure 4. Single-Ended Swing

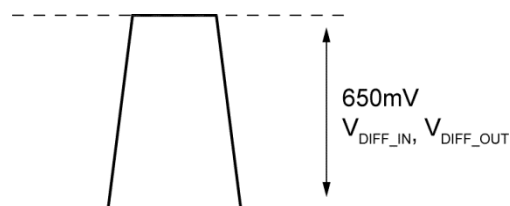


Figure 5. Differential Swing

Input Interface Applications

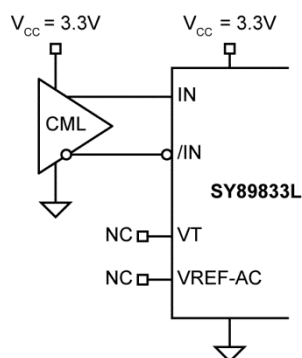


Figure 6. DC-Coupled CML Input Interface

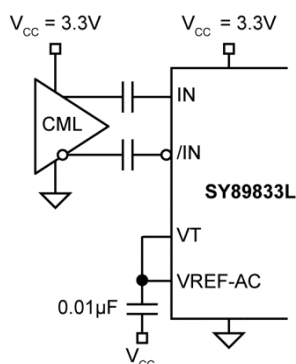


Figure 7. AC-Coupled CML Input Interface

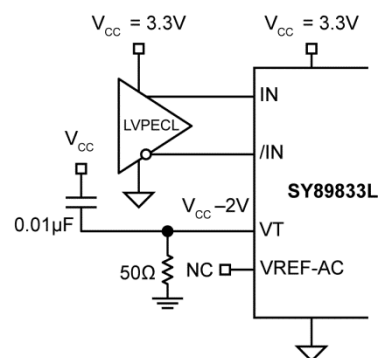


Figure 8. DC-Coupled LVPECL Input Interface

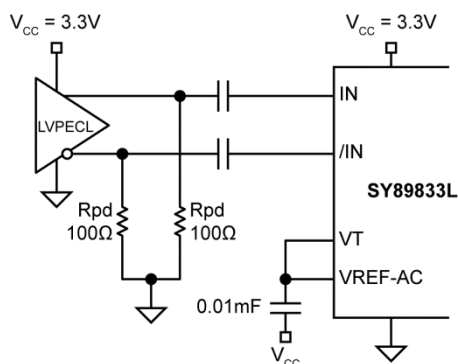


Figure 9. AC-Coupled LVPECL Input Interface

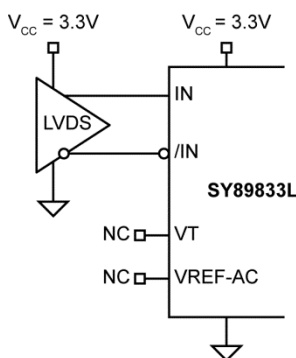
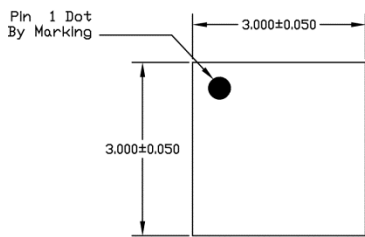


Figure 10. LVDS Input Interface

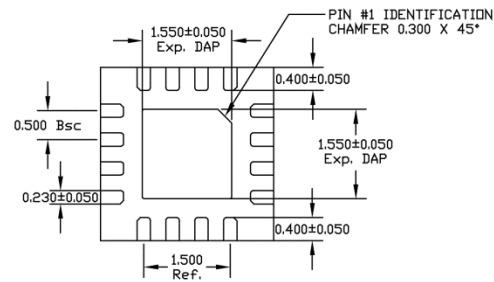
Related Product and Support Documents

Part Number	Function	Data Sheet Link
SY89830U	2.5V/3.3/5V 2.5GHz 1:4 PECL/ECL Clock Driver With 2:1 Differential Input MUX	http://www.micrel.com/_PDF/HBW/sy89830u.pdf
SY89831U	Ultra-Precision 1:4 LVPECL Fanout Buffer/Translator With Internal Termination	http://www.micrel.com/_PDF/HBW/sy89831u.pdf
SY89832U	2.5V Ultra-Precision 1:4 LVDS Fanout Buffer / Translator With Internal Termination	http://www.micrel.com/_PDF/HBW/sy89832u.pdf
SY89834U	2.5V/3.3V Two Input, 1GHz LVTTTL/CMOSTO-LVPECL 1:4 Fanout Buffer/Translator With 2:1 Input MUX	http://www.micrel.com/_PDF/HBW/sy89834u.pdf
HBW Solutions		http://www.micrel.com/index.php/en/products/clock-timing.html

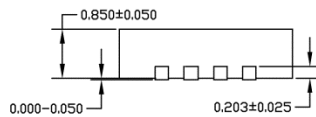
Package Information⁽¹⁴⁾



TOP VIEW

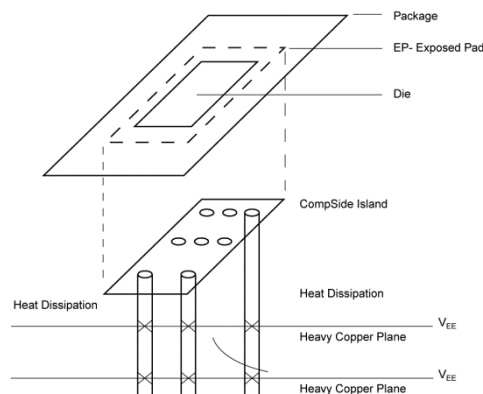


BOTTOM VIEW



SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. MAX. PACKAGE WARPAGE IS 0.05 mm.
 3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
 4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



PCB Thermal Consideration for 16-Pin QFN Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 moisture sensitivity classification, and are shipped in dry-pack form.
2. Exposed pads must be soldered to a ground for proper thermal management.

16-Pin QFN (code)

Note:

14. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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