LSI/CSI

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LS7183/LS7184

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QUADRATURE CLOCK CONVERTER

FEATURES:

- x1, x2 and x4 resolution
- Programmable output pulse width (200ns to 140µs)
- Excellent regulation of output pulse width
- TTL and low voltage CMOS compatible I/Os
- +3V to +5.5V operation (V_{DD}-V_{SS})
- LS7183, LS7184 (DIP)
  LS7183-S, LS7184-S (SOIC) - See Figure 1

DESCRIPTION:

The LS7183 and LS7184 are monolithic CMOS silicon gate quadrature clock converters. Quadrature clocks derived from optical or magnetic encoders, when applied to the A and B inputs of the LS7183/LS7184, are converted to strings of Up Clocks and Down Clocks (LS7183) or to a Clock and an Up/Down direction control (LS7184). These outputs can be interfaced directly with standard Up/Down counters for direction and position sensing of the encoder.

INPUT/OUTPUT DESCRIPTION:

RBIAS (Pin 1)
Input for external component connection. A resistor connected between this input and V_{SS} adjusts the output clock pulse width (Tow).

V_{DD} (Pin 2)
Supply Voltage positive terminal.

V_{SS} (Pin 3)
Supply Voltage negative terminal**.**

A, B (Pin 4, Pin 5)
Quadrature Clock inputs A and B. Directional output pulses are generated from the A and B clocks according to Fig. 2. A and B inputs have built-in immunity for noise signals less than 50ns duration (Validation delay, T_{VD}). The A and B inputs are inhibited during the occurrence of a directional output clock ($\overline{UPCK}$ or $\overline{DNCK}$), so that spurious clocks resulting from encoder dither are rejected.

MODE (Pin 6)
MODE is a 3-state input to select resolution x1, x2 or x4. The input quadrature clock rate is multiplied by factors of 1, 2 and 4 in x1, x2 and x4 mode respectively in producing the output UP/DN clocks (See Fig. 2). x1, x2 and x4 modes selected by the MODE input logic levels are as follows:

Mode = 0 : x1 selected
Mode = 1 : x2 selected
Mode = Float : x4 selected

PIN ASSIGNMENT - TOP VIEW

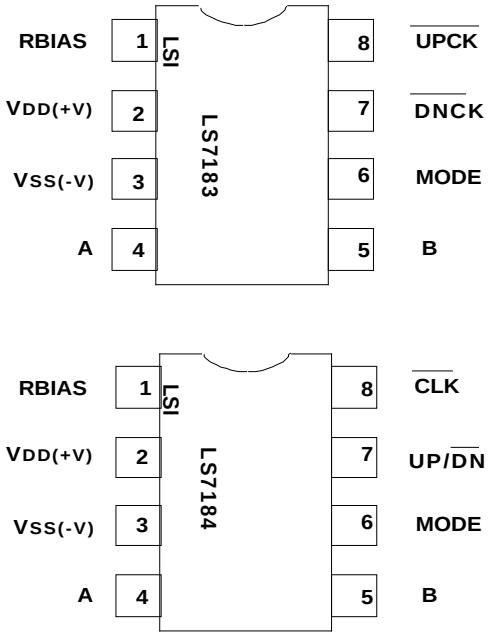


FIGURE 1

LS7183 - $\overline{DNCK}$ (Pin 7)
In LS7183, this is the DOWN Clock Output. This output consists of low-going pulses generated when A input lags the B input.

LS7184LV - UP/$\overline{DN}$ (Pin 7)
In LS7184, this is the count direction indication output. When A input leads the B input, the UP/$\overline{DN}$ output goes high indicating that the count direction is UP. When A input lags the B input, UP/$\overline{DN}$ output goes low, indicating that the count direction is DOWN.

LS7183 - $\overline{UPCK}$ (Pin 8)
In LS7083LV, this is the UP Clock output. This output consists of low-going pulses generated when A input leads the B input.

LS7184 - $\overline{CLK}$ (Pin 8)
In LS7184, this is the combined UP Clock and DOWN Clock output. The count direction at any instant is indicated by the UP/$\overline{DN}$ output (Pin 7).

NOTE: For the LS7184, the timing of $\overline{CLK}$ and UP/$\overline{DN}$ requires that the counter interfacing with LS7184 counts on the rising edge of the $\overline{CLK}$ pulses.

ABSOLUTE MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
DC Supply Voltage	V_{DD} - V_{SS}	7.0	V
Voltage at any input	V_{IN}	V_{SS} - .3 to V_{DD} + .3	V
Operating temperature	T_A	-20 to +85	°C
Storage temperature	T_{STG}	-55 to +150	°C

DC ELECTRICAL CHARACTERISTICS:

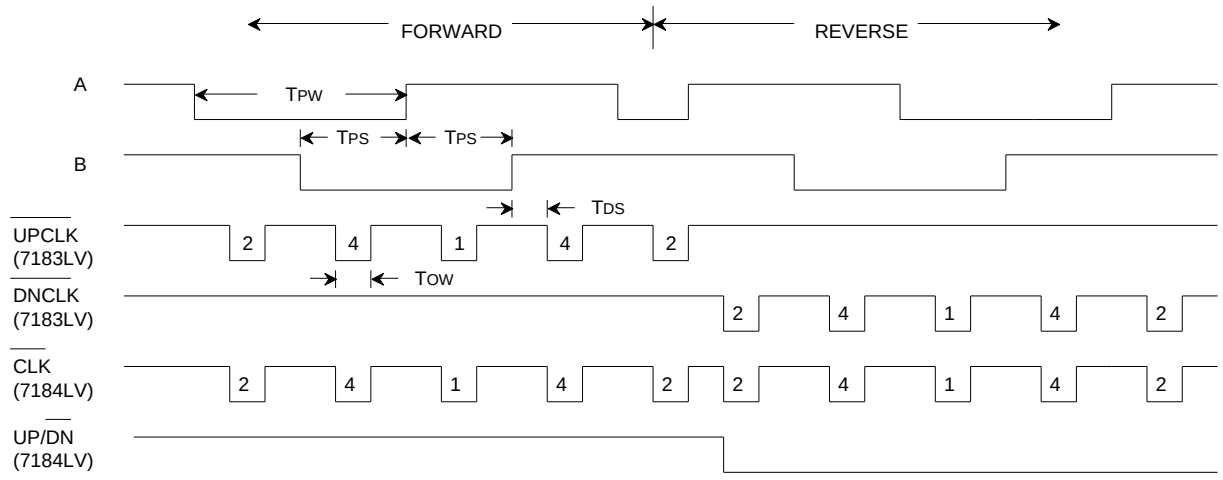
(Unless otherwise specified V_{DD} = 3V to 5V and TA = -20°C to 85°C)

PARAMETER	SYMBOL	MIN	TYPE	MAX	UNITS	CONDITON
Supply Voltage	V_{DD}	3.0	-	5.5	V	-
Supply current	I_{DD}	-	30	45	µA	V_{DD} = 3V
	I_{DD}	-	110	150	µA	V_{DD} = 5V
MODE input:						
Logic 0	V_{ml}	-	-	0.6	V	-
Logic 1	V_{mh}	V_{DD} -0.6	-	-	V	-
Logic float	V_{mf}	(V_{DD}/2) - 0.5	V_{DD}/2	(V_{DD}/2) + 0.5	V	-
Logic 0 input current	I_{ml}	-	3.0	5.0	µA	V_{DD} = 3V
	I_{ml}	-	12.0	16.0	µA	V_{DD} = 5V
Logic 1 input current	I_{mh}	-	-3.0	-5.0	µA	V_{DD} = 3V
	I_{mh}	-	-12.0	-16.0	µA	V_{DD} = 5V
A,B inputs:						
Logic 0	V_{ABl}	-	-	0.3V_{DD}	V	-
Logic 1	V_{ABh}	0.7V_{DD}	-	-	V	-
Input current	I_{ABlk}	-	0	10	nA	-
RBIAS input:						
External resistor	R_B	5k	-	10M	ohm	-
All outputs:						
Sink current	I_{ol}	-1.2	-1.8	-	mA	Vo = 0.5V, V_{DD} = 3V
	I_{ol}	-2.5	-3.5	-	mA	Vo = 0.5V, V_{DD} = 5V
Source current	I_{oh}	1.2	1.8	-	mA	Vo = 2.5V, V_{DD} = 3V
	I_{oh}	2.5	3.5	-	mA	Vo = 4.5V, V_{DD} = 5V

TRANSIENT CHARACTERISTICS

(TA = -20°C to 85°C)

PARAMETER	SYMBOL	MIN	TYPE	MAX	UNITS	CONDITON
Output Clock Pulse Width	T_{OW}	190	-	-	ns	See Fig. 2
A,B inputs:						
Validation Delay	T_{VD}	-	25	50	ns	V_{DD} = 5V
	T_{VD}	-	50	100	ns	V_{DD} = 3V
Phase Delay	T_{PS}	T_{VD} +T_{OW}	-	Infinite	s	-
Pulse Width	T_{PW}	2T_{PS}	-	Infinite	s	-
Frequency	$f_{A,B}$	-	-	1/(2T_{PW})	Hz	-
Inupt to Output Delay	T_{DS}	-	200	270	ns	V_{DD} = 3V
	T_{DS}	-	110	150	ns	V_{DD} = 5V



NOTE: Output clocks labelled 1, 2 and 4 have the following interpretations.
1: Generated in x1, x2 and x4 modes
2: Generated in x2 and x4 modes only
4: Generated in x4 mode only

FIGURE 2. LS7183, LS7184 INPUT/OUTPUT TIMING

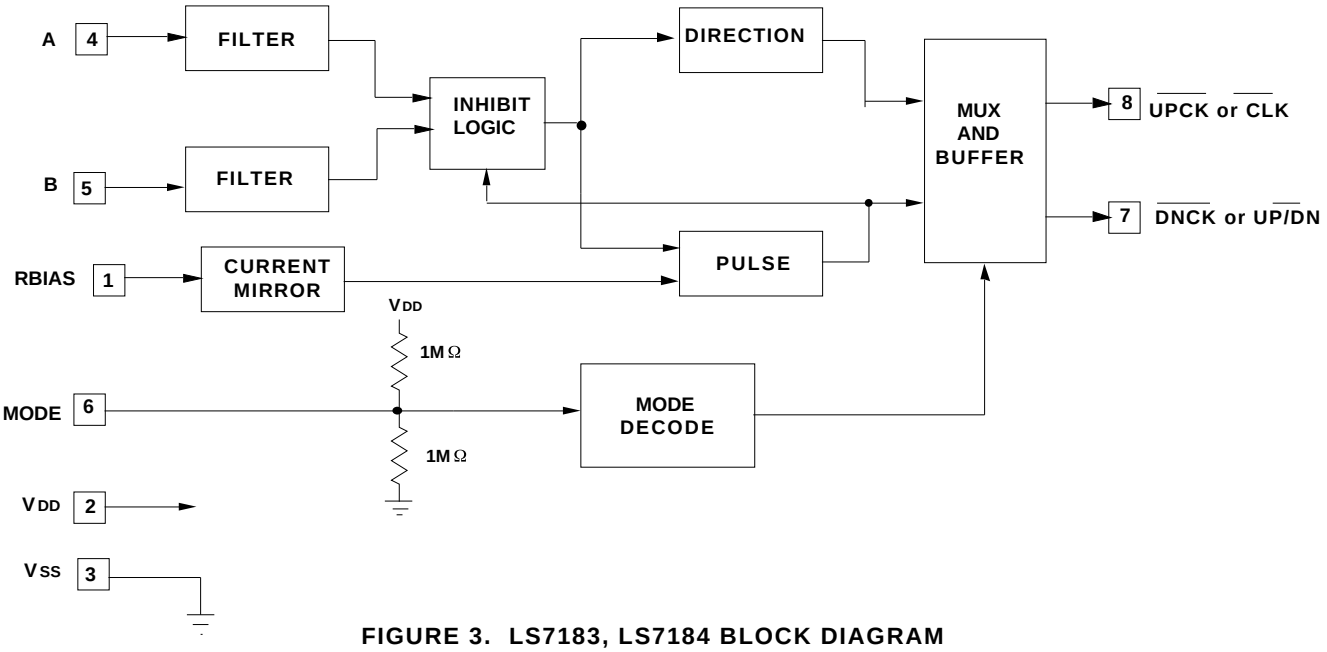


FIGURE 3. LS7183, LS7184 BLOCK DIAGRAM

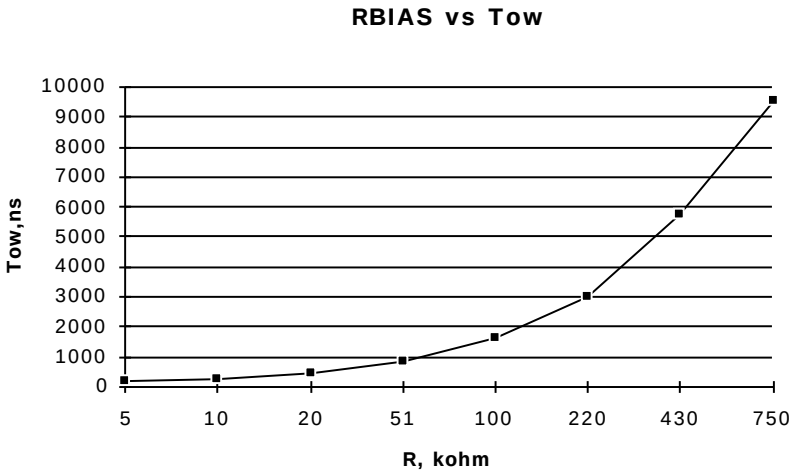


Figure 4. Bias resistance vs pulse width. R in kΩ.

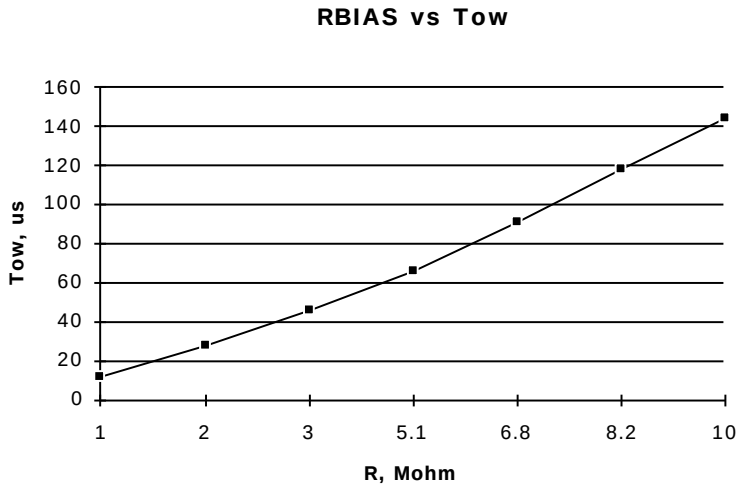


Figure 5. Bias resistance vs pulse width. R in MΩ.

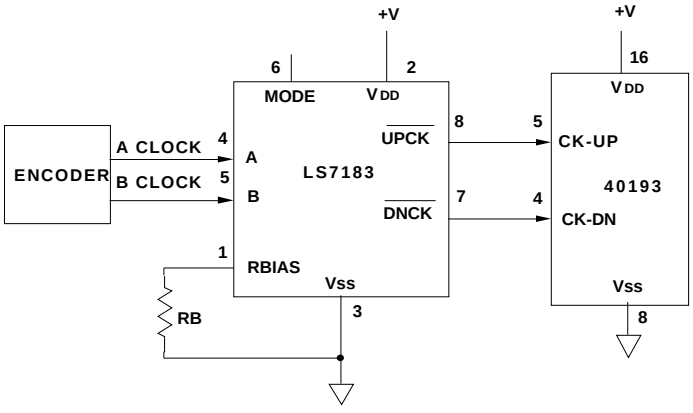


FIGURE 6A. TYPICAL APPLICATION FOR LS7183 IN x4 MODE

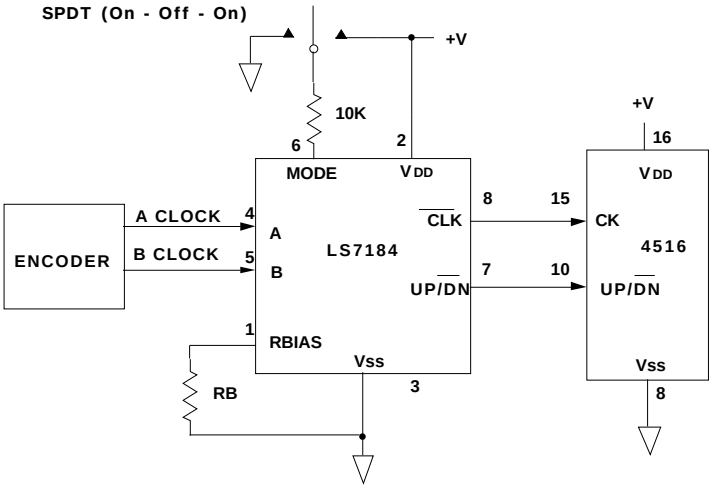


FIGURE 6B. TYPICAL APPLICATION FOR LS7184 WITH MODE SELECTION