TLV320AIC29EVM and TLV320AIC29EVM-PDK

This user's guide describes the characteristics, operation, and use of the TLV320AIC29EVM, both by itself and as part of the TLV320AIC29EVM-PDK. This evaluation module (EVM) is a complete stereo audio codec evaluation module, with several audio inputs and outputs, side tone, key click, and effects capabilities. A complete circuit description, schematic diagram and bill of materials are also included.

The following related documents are available through the Texas Instruments web site at www.ti.com.

EVM-COMPATIBLE DEVICE DATA SHEETS	
DEVICE	**LITERATURE NUMBER**
TLV320AIC29	SLAS494
TAS1020B	SLES025
REG1117-5	SBVS001
TPS767D301/318	SLVS209
SN74LVC125A	SCAS290
SN74LVC1G125	SCES223
SN74LVC1G07	SCES296

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1 EVM Overview

1.1 Features

- Full-featured evaluation board to evaluate/test the TLV320AIC29 functions and features
- Modular design for use with a variety of DSP and microcontroller interface boards

The TLV320AIC29EVM-PDK is a complete evaluation kit, which includes a TLV320AIC29EVM board, a universal serial bus (USB)-based motherboard, and the evaluation software for use with a personal computer running Microsoft Windows™ operating systems (Win2000 or XP).

1.2 Introduction

The TLV320AIC29 is an advanced analog interface circuit. It communicates with a host processor through a standard SPI serial interface. A mono-input/stereo-output audio codec is included in the TLV320AIC29, and audio data is communicated to the device over an I^2S bus. The TLV320AIC29 also offers two auxiliary analog inputs and one battery voltage measurements. The battery measurement is capable of reading battery voltages up to 6 V while operating with only a 2.7-V supply. It also has an on-chip temperature sensor capable of 1°C resolution. For more detail about the device, refer to the TLV320AIC29 data sheet.

The TLV320AIC29EVM is in Texas Instruments' modular EVM form factor, which allows direct evaluation of the TLV320AIC29 performance and operating characteristics, and eases software development and system prototyping. This EVM is compatible with the Texas Instruments 5-6K DSP Interface Board (SLAU104) from Texas Instruments and additional third party boards such as the HPA449 demonstration board from SoftBaugh, Inc. and the Speedy33™ from Hyperception, Inc.

The TLV320AIC29EVM-PDK is a complete evaluation/demonstration kit, which includes the TLV320AIC29 EVM and a USB-based motherboard called the USB-MODEVM Interface Board. Also included with TLV320AIC29EVM-PDK is the evaluation software for use with a personal computer running Microsoft Windows operating systems.

2 Getting Started

This chapter guides you through unpacking and configuring your EVM.

2.1 Unpacking the EVM or EVM-PDK

The EVM kit includes the following:

- TLV320AIC29EVM board, PWB 6451250
- USBMODEVM board, PWM 6463995 (for TLV320AIC29EVM-PDK only)
- CD–ROM, 645125

If any of these components is missing, contact Texas Instruments for a replacement.

2.2 Default Configuration

The default settings of the TLV320AIC29EVM board are shown in Table 1, and the default settings of the USBMODEVM board are shown in Table 2. When you unpack your TLV320AIC29EVM-PDK, ensure that both boards are configured as listed in the two tables.

Table 1. TLV320AIC29EVM Board Default Configuration Settings

Board Identifier	Description		Default Settings
SW1	Headset (SPK1/SPK2) Output Mode Selection		*Capless* mode
JMP1	AGND and DGND connection	Installed: Connect AGND to DGND	Installed
		Removed: Disconnect AGND to DGND	
JMP2	FW Boot source selection	Installed: boot from daughtercard EEPROM	Installed
		Removed: boot from motherboard EEPROM	
JMP3	AUX2 resistance measurement(1)		Removed
JMP4	AUX1 resistance measurement(1)		Removed
JMP5	+1.8VD to TLV320AIC29 DVDD pin connection(2)		Installed
JMP6	+3.9VA to TLV320AIC29 BVDD pin connection (2)		Installed
JMP7	+3.3VA to TLV320AIC29 DRVDD pin connection(2)		Installed
JMP8	+3.3VA to TLV320AIC29 AVDD1 pin connection(2)		Installed
JMP9	+3.3VA to TLV320AIC29 AVDD2 pin connection(2)		Installed
JMP10	IOVDD power selection	Connect 1 ~ 2: IOVDD = +5VD	Connect 3 ~ 4
		Connect 3 ~ 4: IOVDD = +3.3VD	
		Connect 5 ~ 6: IOVDD = +1.8VD	
JMP11	Reset connection	Installed: RESET from J4-GPIO2 and GPIO4	Removed
		Removed: RESET from J4-GPIO2	
JMP12	IOVDD to TLV320AIC29 IOVDD pin connection(2)		Installed
JMP13	MIC BIAS source selection	Connect 1 ~ 2: from +3.3 VA	Connect 2 ~ 3
		Connect 2 ~ 3: from TLV320AIC29 MICBIAS_HND pin	
JMP14	VGND mode Selection	Connect 1 ~ 2: TLV320AIC29 VGND pin as VGND	Connect 1 ~ 2
		Connect 2 ~ 3: TLV320AIC29 VGND pin as CP_OUT–	
JMP15	Differential MICIN selection	Removed: Single-ended MINCIN only	Removed
		Connect 1 ~ 3: MICIN_HND and AUX2 diff	
		Connect 3 ~ 5: MICIN_HND and AUX1 diff	
		Connect 2 ~ 4: MICIN_HED and AUX2 diff	
		Connect 4 ~ 6: MICIN_HED and AUX1 diff	

(1) Refer to the note on the TLV320AIC29 EVM schematic for the details of these jumpers.
(2) JMP5, JMP6, JMP7, JMP8, JMP9 and JMP12 are installed by default. These jumpers can be replaced by current meters for evaluating or testing the corresponding power consumption.

Table 2. USBMODEVM Board Default Configuration Settings

Board Identifier	Description		Default Settings
SW1	Onboard power supply enable	SW1-1: +1.8VD Enable	On: Enabled
		SW1-2: +3.3VD Enable	
SW2	On/Off board control selection	SW2-1: Onboard EEPROM address bit A0	On: A0=0
		SW2-2: Onboard EEPROM address bit A1	Off: A1=1
		SW2-3: Onboard EEPROM address bit A2 On: A2=0	On: A2=0
		SW2-4: Onboard I^2S	On: Onboard
		SW2-5: Onboard MCLK	On: Onboard
		SW2-6: Onboard SPI	On: Onboard
		SW2-7: Onboard RESET	On: Onboard
		SW2-8: External MCLK from J10 (EXT MCK) Off: Not EXT	Off: Not EXT
JMP1	+5VA and +5VD connection	Installed: Connect +5VA to +5VD	Installed
		Removed: Disconnect +5VA to +5VD	
JMP2	AGND and DGND connection	Installed: Connect AGND to DGND	Removed
		Removed: Disconnect AGND to DGND	
	JMP3 Connect I2C SDA pull-up to IOVDD		Removed
	JMP4 Connect I2C SCL pull-up to IOVDD		Removed
JMP5	SPI /SS select	Connect 1 ~ 2: /SS from CNTL	Connect 2 ~ 3 (FSX)
		Connect 2 ~ 3: /SS from FSX	
JMP6	Board power selection	Connect 1 ~ 2: +5VD from USB	Connect 1 ~ 2 (USB)
		Connect 2 ~ 3: +5VD from U2	
JMP7	IOVDD power selection	Connect 1 ~ 2: IOVDD = +5VD	Connect 3 ~ 4 (+3.3VD)
		Connect 3 ~ 4: IOVDD = +3.3VD	
		Connect 5 ~ 6: IOVDD = +1.8VD	
JMP8	TAS1020B P1.3 GPIO connection		Removed
JMP9	TAS1020B P1.2 GPIO connection		Removed
JMP10	TAS1020B P1.1 GPIO connection		Removed
JMP11	TAS1020B P1.0 GPIO connection		Removed
JMP12	TAS1020B P3.5 GPIO connection		Removed
JMP13	TAS1020B P3.4 GPIO connection		Removed
JMP14	TAS1020B P3.3 GPIO connection		Removed

2.3 Connection

The TLV320AIC29 EVM-PDK allows direct evaluation of the TLV320AIC29 device with a personal computer. The TLV320AIC29EVM board, as the daughtercard, is installed on the top of the USBMODEVM motherboard, as shown in Figure 1.

Use a USB cable to connect the PC to the EVM system through the J7 USB connector on the USBMODEVM card.

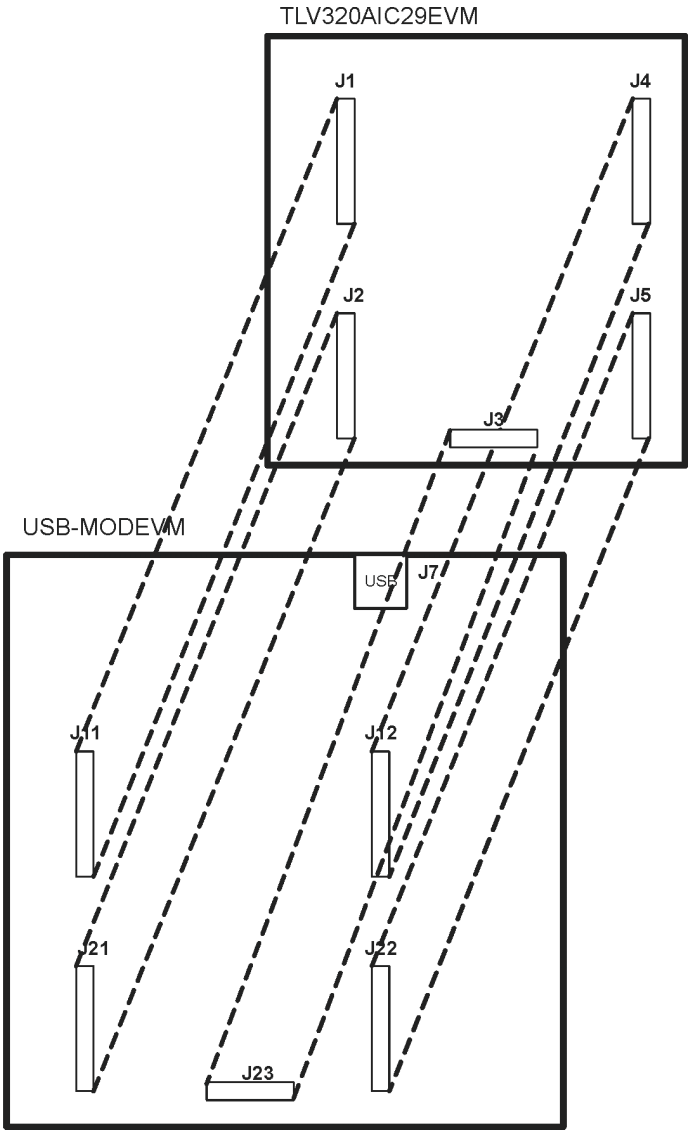

Figure 1. Mount TLV320AIC29EVM Board on Top of USBMODEVM Board

2.4 Quick Start

Once the TLV320AIC29EVM-PDK has been unpacked, and you have verified that both the daughter board (TLV320AIC29EVM) and the motherboard (USBMODEVM) had been configured as shown in Table 1 and Table 2, and connected as shown in Figure 1, install the TLV320AIC29EVM software from the included CD-ROM, following the instructions provided by the installer.

When the installation is complete, connect a USB cable from the PC to the J7 on the motherboard. When the TLV320AIC29EVM-PDK is connected to the PC the first time, the user may see a message that a Human Interface/Audio Device has been connected. When this connection has been made, launch the TLV320AIC29EVM software on the PC. The software should automatically find the TLV320AIC29EVM. If the board is found, the screen shown in Figure 2 appears.

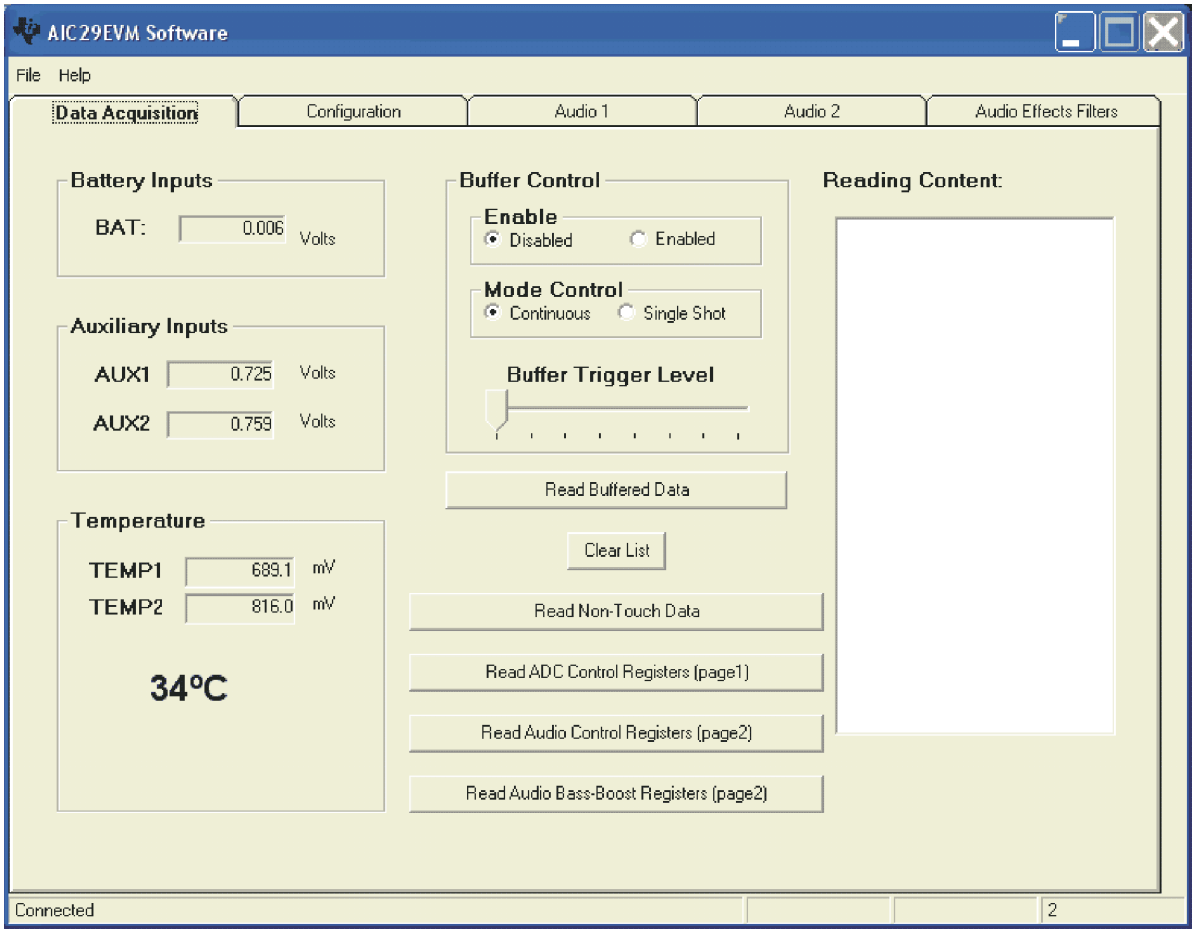

Figure 2. TLV320AIC29 EVM-PDK Software – Data Acquisition Tab

With the firmware/software default configuration, the TLV320AIC29 audio output OUT8 is powered up, and the side tone and the key click functions enabled. To verify proper function of the EVM system, a speaker (8-Ω or above) can be connected to J13 (the loudspeaker connection terminal or OUT8) on the TLV320AIC29EVM daughter-card. A 'ding' sound is heard when the USB cable from the PC is plugged into the motherboard (J7). Additional dings are heard when launching the software. Tapping or talking through the onboard microphone (MK1) on the daughter board is audible through the speaker.

3 Program Description

After installing the software for the TLV320AIC29EVM, the user can begin to evaluate the functions of the TLV320AIC29 device using the evaluation-software graphic user interface (GUI).

The user interface is a simple, five-tab interface. Clicking on a tab takes you to the functions associated with that tab. The program begins on the Data Acquisition (the default) as shown in Figure 2.

3.1 Data Acquisition Screen

The status bar at the bottom of the screen is divided into four sections showing the communication status between the PC and the EVM-PDK. Starting from the left, the first section shows the connection status. If an error in communication occurs, an error message appears here; otherwise, it displays *Connected*, as shown in Figure 2. The final section, on the right side of the status bar, shows the number of readings per second being taken.

3.1.1 Data Acquisition

At this screen and with the buffer mode NOT enabled, the TLV320AIC29 automatically performs the battery and auxiliary input voltage readings, and then TEMP1 and TEMP2 measurements. These measurements are all repeated twice per second, and the results are displayed on the three boxes at the left side of this screen.

3.1.2 Buffer Function

In the middle of the screen, the buffer mode settings can be accessed. By default, the buffer function is disabled, and the BAT, AUX1, AUX2, TEMP1 and TEMP2 data are converted and stored to the corresponding registers. When the *buffer* function is enabled by checking the *Enable* option, the data is converted and saved to the *buffer* registers in page 3 of the TLV320AIC29 memory space. Refer to the data sheet for the details of the *buffer function*.

When the buffer function is enabled by clicking on the *Read Buffered Data* button, the TLV320AIC29 is put into host-controlled mode. The TLV320AIC29 then enters *auto-scan* mode to poll AUX1, AUX2, and TEMP1. The raw data displays in the *Reading Content* on the right side of the Data Acquisition tab, as shown in Figure 3. The data in Figure 3 is listed in this order: AUX1, AUX2, TEMP1, AUX1, AUX2, TEMP1, AUX1, etc.

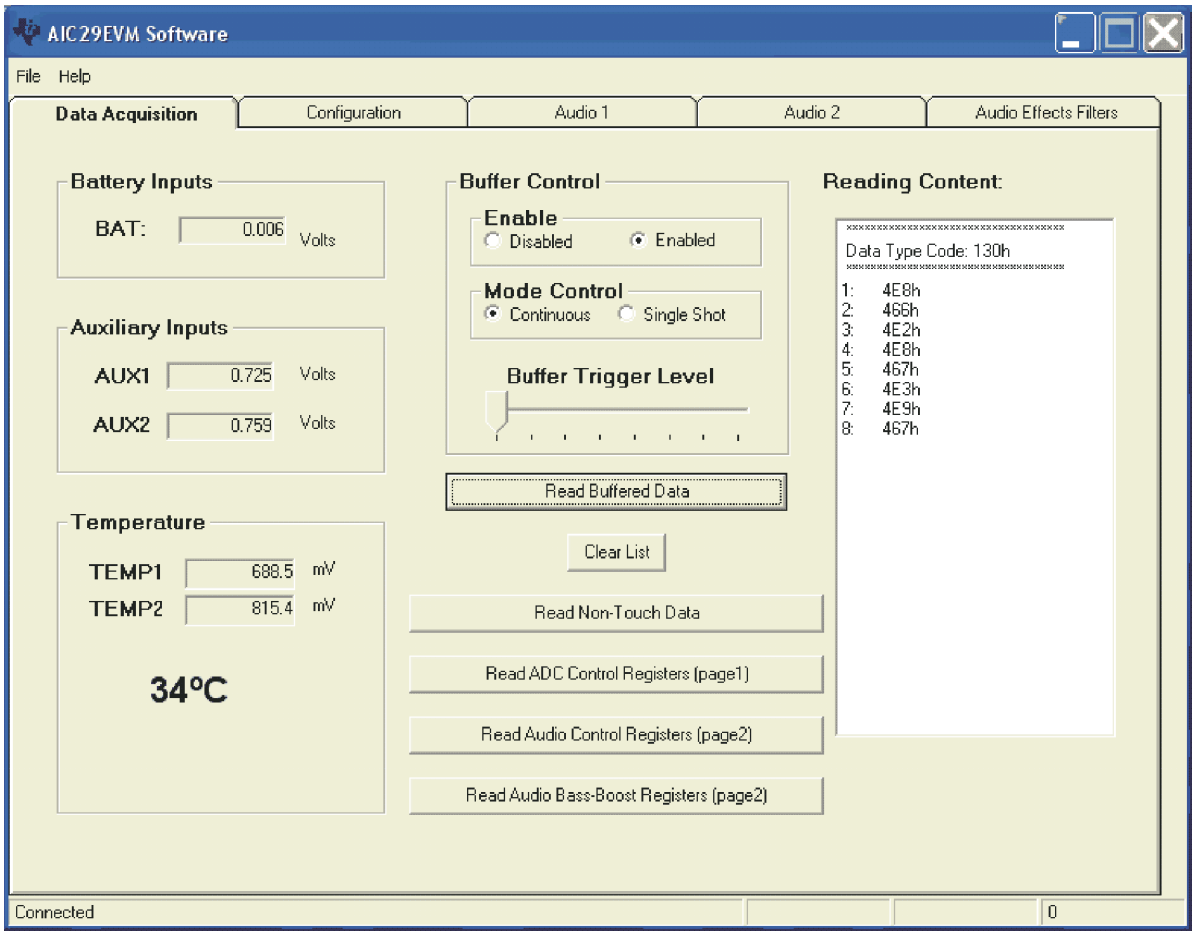

Figure 3. Data Acquisition Screen, *Reading Content* Box

With this EVM version, the buffer trigger level can be set to either 8 or 16, selected by the *Buffer Trigger Level* selection slide. Even though the TLV320AIC29 can be set to a higher trigger level up to 64, this EVM allows only 8 or 16. The buffer function can be set to Continuous or Single Shot mode using the mode-control option box. Refer to the data sheet for more on TLV320AIC29 buffer function. The data in the list is cleared by clicking on the *Clear List* button on this screen.

3.1.3 Register Content Display

Four additional buttons display the corresponding register contents in the list. This is helpful for testing and debugging.

3.2 Configuration Screen

This screen accesses the configurable settings for the TLV320AIC29 analog-to-digital converter (ADC) and reference as shown in Figure 4.

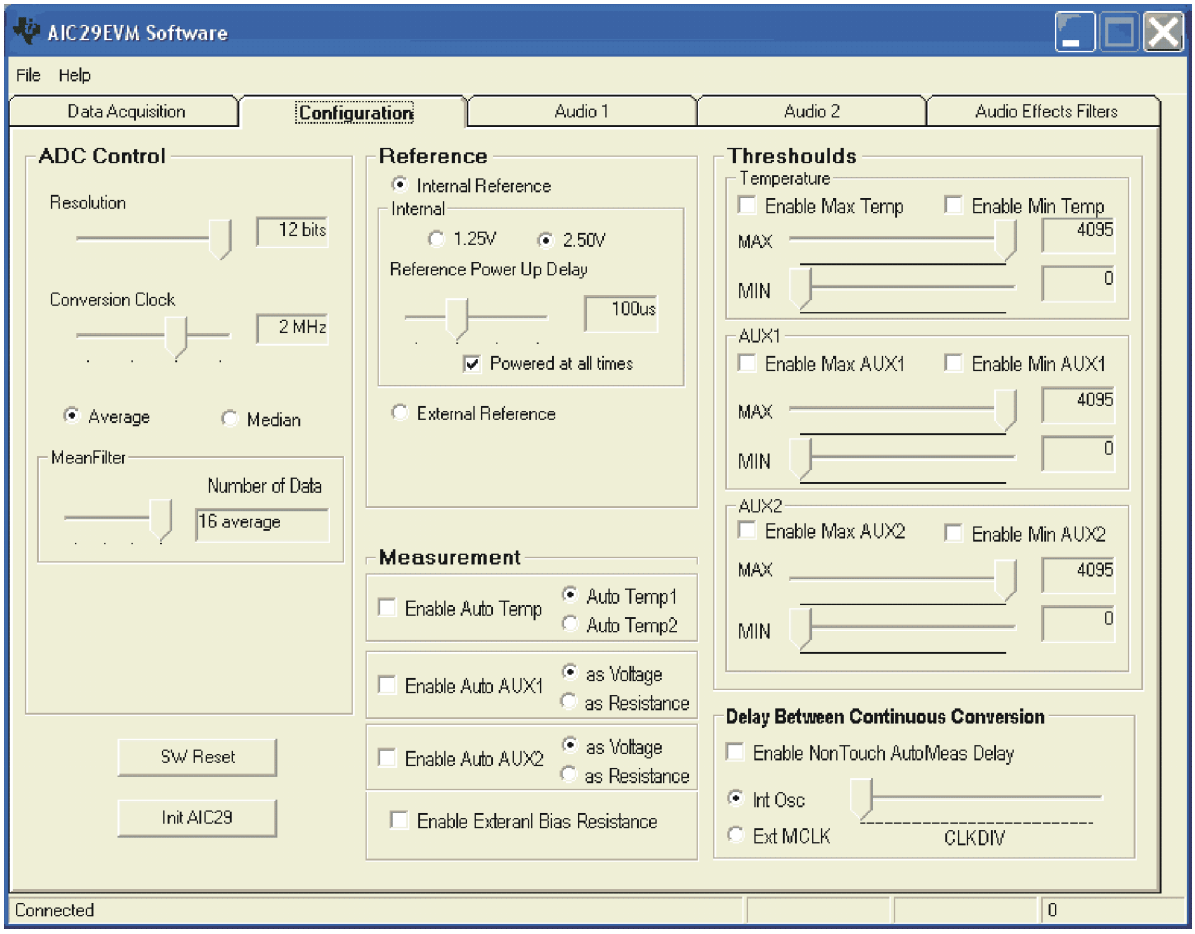

Figure 4. Configuration Screen

3.2.1 ADC Control Section

The sliders in this section control all of the parameters of the A/D converter for BAT, AUX1, AUX2, TEMP1, and TEMP2 data. Each slider controls one parameter, whose value is shown next to the slider.

- **Resolution —** Selects between 8–, 10–, and 12–bit resolution.
- **Conversion Clock —** The internal clock that runs the ADC can run at 8, 4, 2, or 1 MHz. When running at 8 MHz, only 8-bit resolution is possible; when running at 4 MHz, only 8- or 10-bit resolution is possible. Only 1- or 2-MHz clock rates allow 12-bit resolution to be chosen.
- **Average/Median —** There are two ways to reduce noise effect to the ADC result. One is averaging, where 4, 8, or 16 readings are averaged; another option is to find the median value among 5, 9, or 15 readings. The default is the average mode, as shown in Figure 4. Median mode can be selected with the corresponding button.

Note that these settings apply to all operations of the A/D converter and, thus, resolution and averaging can be changed to increase accuracy in the data acquisition functions.

3.2.2 Reference Section

A reference voltage is needed for ADC measurements.

The internal reference voltage can be set to either 1.25 V or 2.5 V. The internal reference powers down between conversions to save power. The *Powered at all times* checkbox overrides this feature, and the reference does not power down. If the reference is allowed to power down, the TLV320AIC29 must allow a delay time for the reference to power up when a conversion is to take place. This delay time can be set using the slider in this section.

If an external reference is to be used, it can be selected as shown in Figure 5. The value of the external reference is entered in the text box shown.

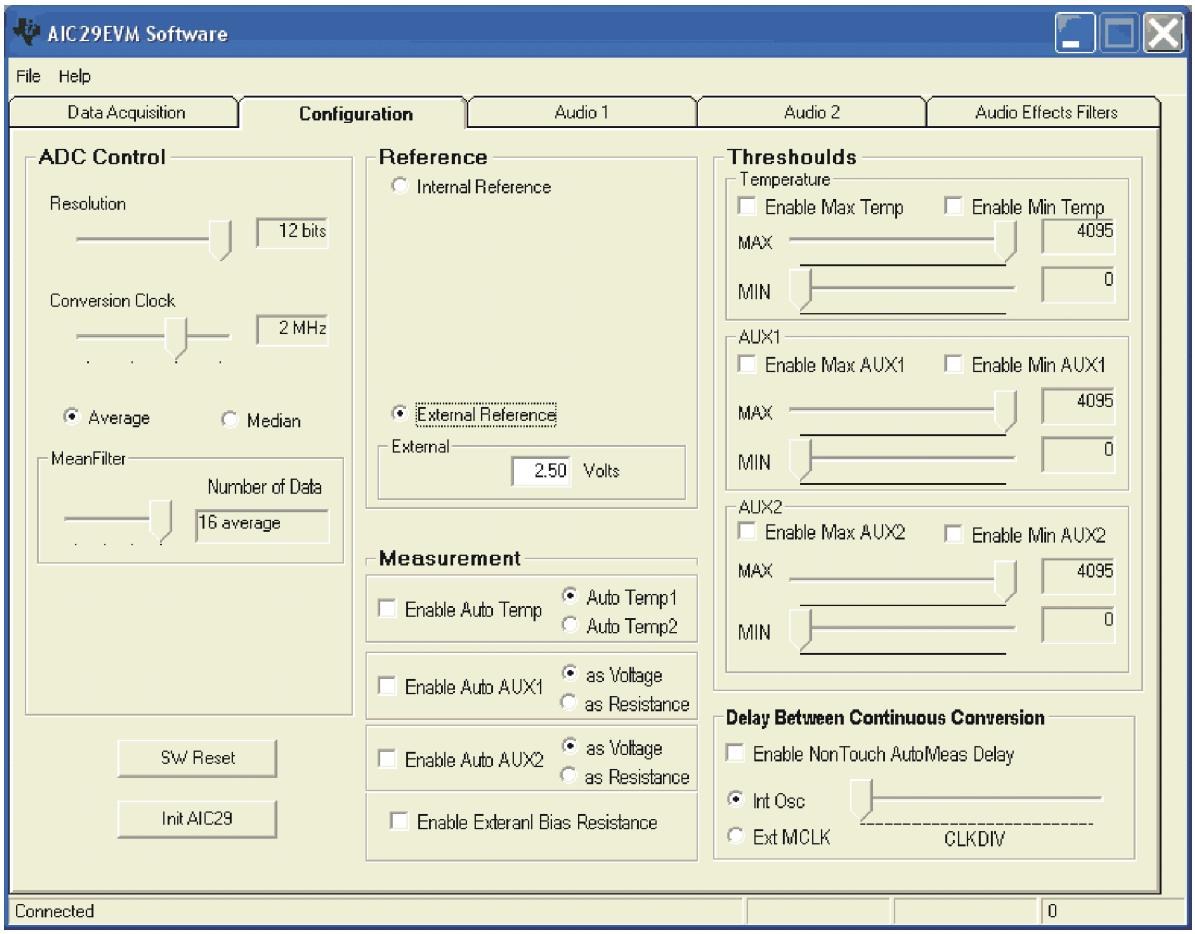

Figure 5. Configuration Screen With External Reference Selection

3.2.3 Measurement Section

The TLV320AIC29 supports programmable, automatic temperature and auxiliary-input measurements. In the auto measurement mode, the TLV320AIC29 can auto start the TEMP1, TEMP2, AUX1, and/or AUX2 measurement after a programmable interval. The checkboxes and sliders in the Measurement section provide choices.

Additionally, the AUX1 and AUX2 can be configured to measure voltage or resistance. Under the resistance measurement, the bias can be configured as external or internal by checking or unchecking the *Enable External Bias Resistance* box.

3.2.4 Threshold Section

The TLV320AIC29 monitor the temperature and the auxiliary inputs and set corresponding flags if an input exceeds the bounds set in the threshold registers.

In this section, if the threshold function has not been enabled (*Enable* checkbox has not been checked), the corresponding MAX/MIN slider does not move. Also note that the MAX value must be greater than or equal to the MIN value.

3.2.5 Continuous Conversion Delay Section

In the auto measurement mode, the delays between the conversions are programmable. This section can be used to program to delays between the continuous conversions.

By clicking on the Enable checkbox, the auto measurement delay is enabled. The delay-time option allows selection of delay clock source and divider.

The clock used can be the internal oscillator or the external MCLK. The clock divider (CLKDIV) is used to derive the 1-MHz clock for the programmable delay. This sets the CLKDIV so that MCLK/CLKDIV = 1 MHz.

3.2.6 Reinitialization and Reset

Two buttons on this screen allow the user to reset and reinitialize the TLV320AIC29. By clicking the *SW Reset* button, a software device reset is issued to the TLV320AIC29. By clicking the *Init TLV320AIC29* button, the control registers (for ADC and audio) revert back to the startup (firmware) default settings.

To restore the TLV320AIC29 EVM to its power-up state, click *SW Reset*, followed by *Init TLV320AIC29*.

3.3 Audio Screens

Three tabs control the TLV320AIC29 audio functions: *Audio 1*, *Audio 2*, and *Audio Effects Filters* tabs.

Figure 6 shows the default condition of the Audio 1 tab with the following sections:

- INTERFACE: Audio I^2S port
- PLL: PLL parameters to get the desired FSref frequency
- ADC: Audio ADC, and select the ADC input source
- DAC/Outputs: Audio DAC and the all analog output features
- GPIO1: GPIO1 function/status
- GPIO2: GPIO2 function/status

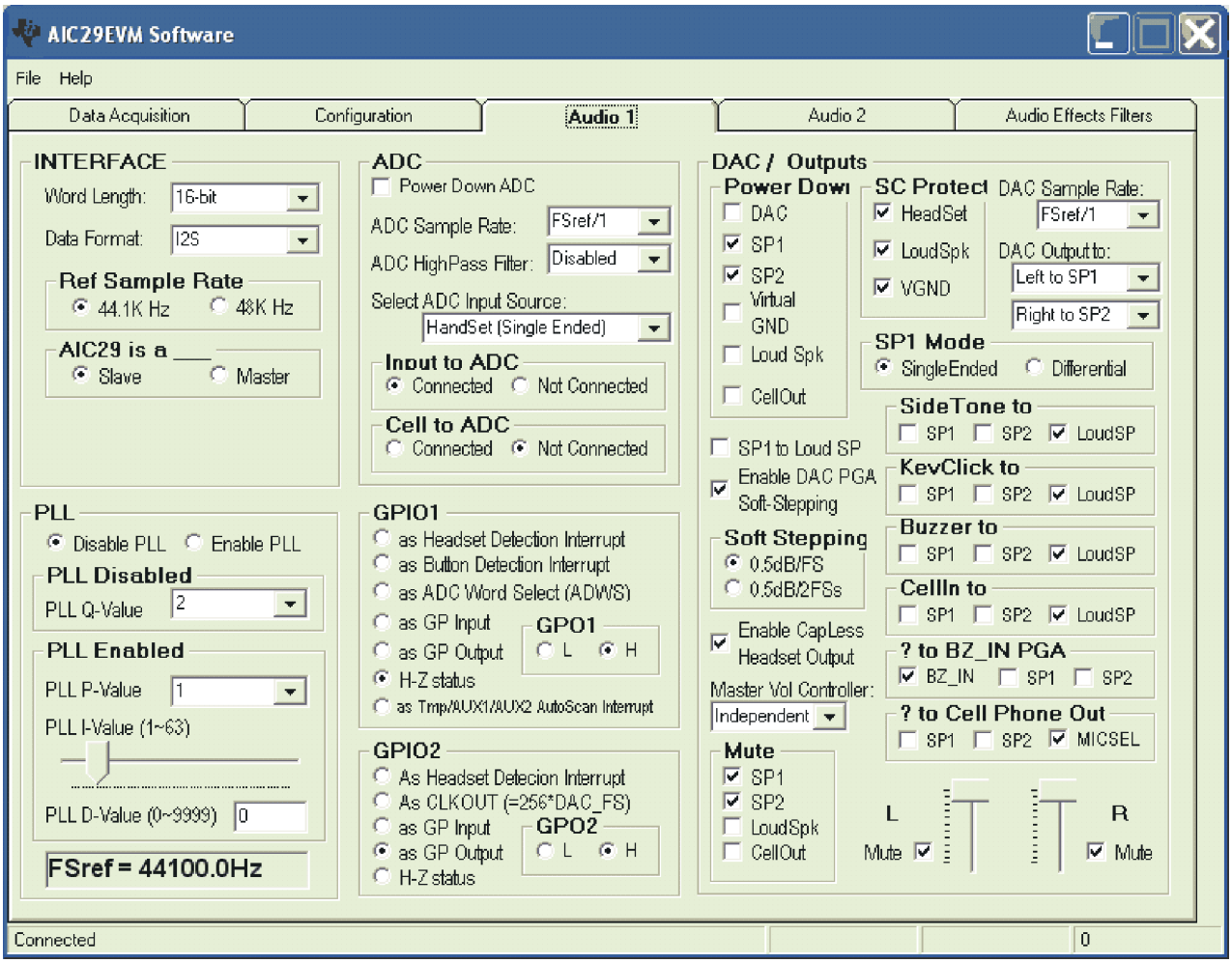

Figure 6. Audio 1 Screen at Default

Figure 7 shows the default condition of the Audio 2 tab. The functions and setting on Audio 2 mainly control the audio analog inputs with the following sections:

- HeadSet: Headset input power and gain control (PGA or AGC) function and other headset specified functions.
- HandSet: Handset input power and gain control (PGA or AGC) function and other handset specified functions.
- Cell Phone: Cell-phone input power and gain control (PGA or AGC) function.
- SideTone: Sidetone power and gain.
- KeyClick: Key-click tone.
- Buzz Input: Power and gain for the BUZZ_IN input pin.

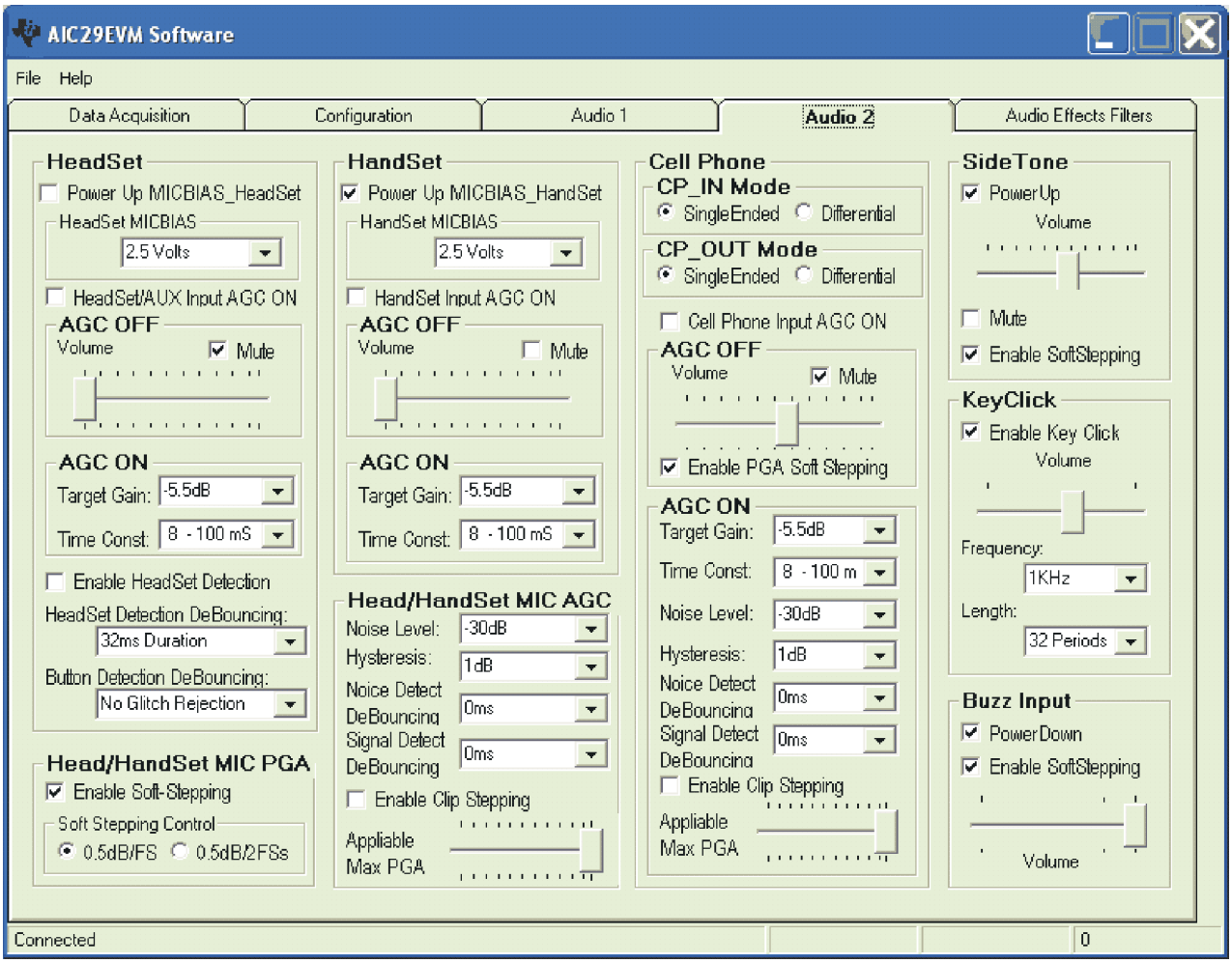

Figure 7. Audio 2 Screen at Default

Figure 8 shows the default configuration of the AudioEffects Filters tab. This tab displays the boost filters, the de-emphasis filter, and the DAC and output driver pop-noise reduction functions.

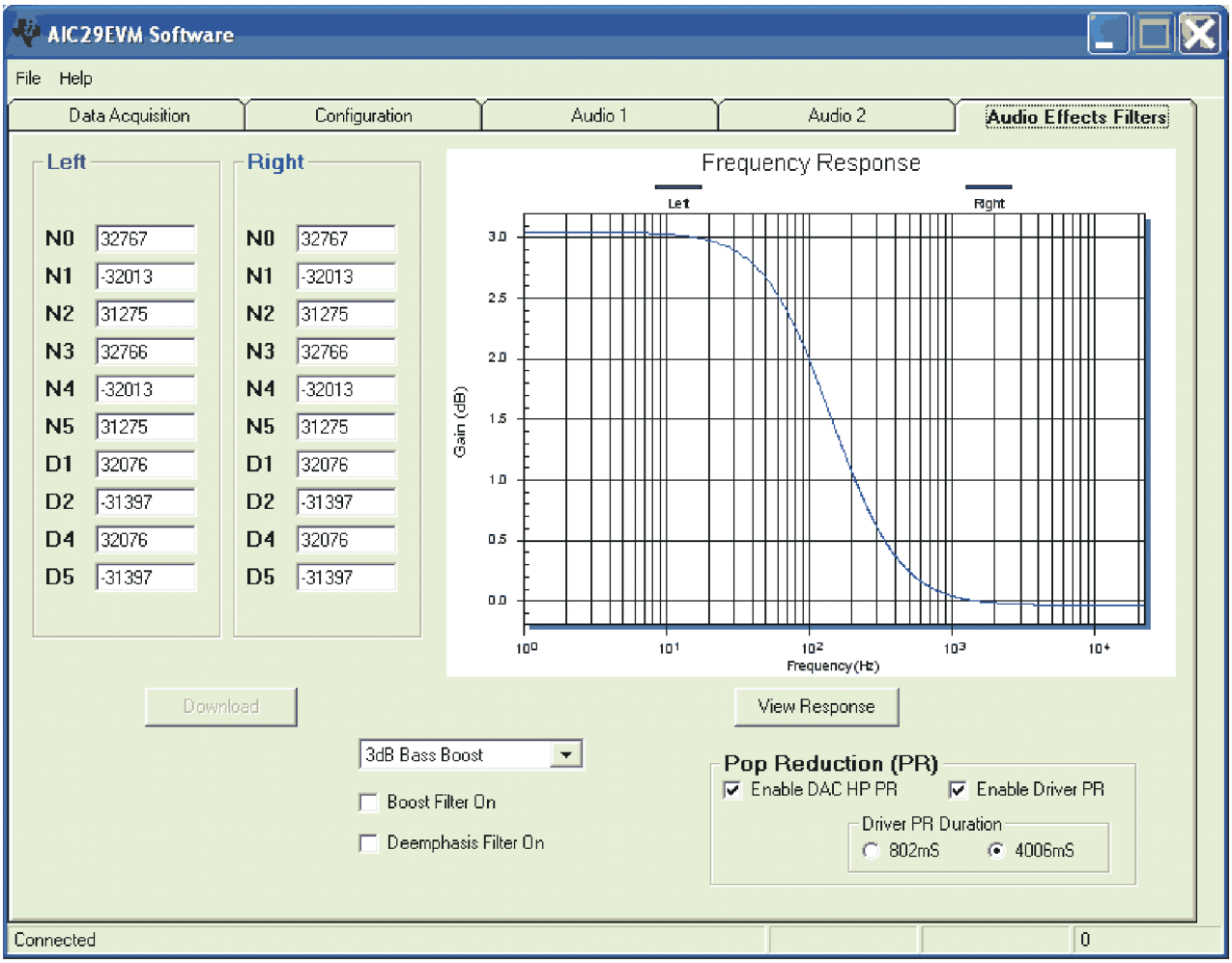

Figure 8. Bass Boost Filter Screen at Default

3.3.1 Interface Section

This section (refer to Figure 6) controls the behavior of the I^2S port (BCLK, LRCLK, DIN, and DOUT pins). In this EVM, the audio port transfers the 16 bit data in I^2S format, and the codec reference sample rate is at 44.1 kHz.

The TLV320AIC29 is programmed as a slave by default. The onboard processor TAS1020B is the master, which generates the BCLK and LRCLK signal. If the TLV320AIC29 is used as a master, the onboard processor must be disabled and the I^2S port must be detached from the processor by turning OFF the onboard I^2S interface. Refer to Table 2 for more information about hardware settings.

3.3.2 PLL Section

There is an on-chip phase-locked loop (PLL) on the TLV320AIC29. The PLL can be enabled or disabled, based on the given master clock (MCLK) to the TLV320AIC29 and the required reference frequency (FSref) for the codec. For more details on the PLL, refer to the TLV320AIC29 data sheet.

The PLL can be configured in the PLL Secton of Audio 1 screen (Figure 6).

The default frequencies for this EVM board are

- MCLK = 11.2896 MHz
- Reference sample rate = 44.1 kHz

At the bottom of the section, the corresponding FSref frequency is shown based on the selection of:

1. the Q-value if the PLL has not been enabled, or
2. the P, J, D values if the PLL has been enabled.

3.3.3 ADC Section

This section (Audio 1 Tab, Figure 6) configures the audio ADC power and the analog input source.

By default, the audio ADC is powered up so that the audio-recording function can start to run at the default settings. By checking *Power Down ADC*, audio ADC power is disabled.

The ADC sample rate can be set as a divider frequency from the reference frequency, FSref. For example, when FSref = 44.1 kHz (set at the INTERFACE section of the same tab), an 8-K sample rate is achieved by setting the divider to 5.5 (44100/5.5 = 8018 Hz).

The audio ADC also has a high-pass filter, which is a sub-multiple of the sample rate, to remove dc or low frequency components from the input signal.

The input signal to the audio ADC can be selected from different analog resources and under different modes using the *Select ADC Input Source* option list. The microphone input from the headset or the handset can be selected; the single-ended or the differential input (paired with AUX1 or AUX2) can be used.

The cell-phone input can also be connected to the audio ADC.

3.3.4 DAC/Outputs Section

This section configures the audio DAC power and all functions of the analog outputs, such as power, gain, mode, and destination, which identifies the analog output pin or pins where the analog output signal is sent.

In the *Power Down* subsection, the DAC and the output driver circuits can be powered up/down individually. By checking a checkbox, the corresponding TLV320AIC29 circuit is powered down.

In the *SC Protect* subsection, the short-circuit (SC) protection function can be enabled or disabled. When the short-circuit protection function is enabled and a short-circuit occurs, all analog outputs are disabled and the corresponding flag is set. For example, to set the headset SC protection, check the box. In the event of a headset short circuit, all analog outputs are disabled, and D1 of control registers in page 2 address 0x1D is set. The TLV320AIC29 requires hardware or software reset to return to normal operation.

Similar to the ADC, the DAC sample rate can be set as a divider frequency from the reference FSref frequency, through the *DAC Sample Rate* option list.

The TLV320AIC29 has the capability to route the stereo DAC output signals to the selected analog output. To route the signals to the headset drivers (SP1 and SP2 pins), select from the *DAC Output* to lists. By default, the left channel DAC output is routed to SP1 and the right channel to SP2.

The signal routed to SP1 can also be output to the loud speaker (OUT8P/OUT8N), if the *SP1* to *Loud SP* checkbox is checked.

SP1 can be used in single-ended or differential mode. In single-ended mode, it is driven as one channel of the stereo headset outputs, and the audio sound is output through a headset at J11 on the TLV320AIC29EVM daughtercard. In differential mode, the SP1 is paired with the OUT32N pin as the *receiver driver*, and the audio sound is output through a speaker connected to the terminal block J2 on the TLV320AIC29EVM. By default, the SP1 is set to single-ended mode.

Other signals, such as the SideTone, KeyClick, CP_IN, and BUZZ_IN can be routed to speaker 1 (SP1), speaker 2 (SP2), and/or the loud speaker (LoudSP). Signal selection can be done in this section by checking the corresponding checkbox.

The signals to SP1, SP2, or the ADC can be output to the TSC's cellphone output pin. And the BUZZ_IN, SP1 and SP2 signals can also be output the BUZZ_IN PGA.

The DAC PGA gain, can be set to soft-stepping mode. Under the soft-stepping mode, the soft stepping can be set to either 0.5–dB per one sample, or 0.5–dB per two samples.

The stereo DAC audio volume is controlled by the left (L) and right ®) volume control slides, selectable through setting the master volume controller, in three different ways:

- Independent,
- Right channel controlled, or
- Left channel controlled.

In addition to the left and right DAC channel volume controls and mutes, the analog signals from the SPK1, SPK2, OUT8P/OUT8N (loud speaker), and CP_OUT pins can be individually muted or unmuted.

The TLV320AIC29 supports both capacitor-coupled (cap) and capacitorless (capless) headset interfaces through settings in software and hardware. To use the capless outputs, Check the box *Enable Capless Headset Output*, and select the CAPLESS setting on SW1 on the TLV320AIC29EVM daughter board.

Note: The settings of SW1 and *Enable Capless Headset Output* must match for proper EVM operation.

3.3.5 GPIO1 and GPIO2 Sections

The two GPIO pins on the TLV320AIC29 are programmed for several different functions, selectable through the GPIO1 or GPIO2 section. Refer to the data sheet for more information. When a GPIO pin is used as a digital output, its status can be controlled by the *GPO Command* to either logic high or low. When not being used, the GPIO pin should be set to high impedance (Hi-Z) status.

3.3.6 Headset Section

The headset section is in the Audio 2 tab, which is used mainly to select the headset-amplifier input gain control between the headset PGA or the AGC, using the *Headset/AUX Input AGC ON* checkbox.

By default, the AGC is OFF and the programmable gain amplifier (PGA) on the headset circuit is selected for the gain control, allowing analog input gain control from 0 dB to 59.5 dB. When the AGC is OFF, moving the volume slide on the *AGC OFF* subsection adjusts the PGA on the MICIN_HED path and checking the Mute box mutes the headset input signal.

When the PGA changes from the current value to a newly programmed value, the change rate can be controlled if the *PGA Soft Stepping* box is checked in the *Head/Handset MIC PGA* section, where the PGA changes 0.5 dB at either 1 step per sample or one step per two samples.

When the box by AGC ON is checked, the AGC is enabled. Refer to the TLV320AIC29 data sheet and the appreciated application note(s) for setting and using the AGC.

In addition to the input gain control, the headset microphone bias can be selected. The programmable de-bounce features for the headset and button detect are also configured in this section. Refer to data sheet for the details on detection and de-bounce.

3.3.7 Handset Section

Similar to the headset section, the handset section is used mainly to configure the handset input gain through the handset PGA or the AGC, selectable by the Handset Input *AGC ON* checkbox.

By default, when the handset AGC is OFF, and the programmable gain amplifier (PGA) is selected for the input gain control, allowing analog input gain control from 0 dB to 59.5 dB. Under the case (AGC OFF), moving the volume slide on the *AGC OFF* subsection adjusts the PGA on the MICIN_HND path and checking the Mute box mutes the handset input signal.

The handset and headset share the soft-stepping settings. Refer to the explanation in the *Headset Section* for the feature and settings.

Similar to the headset, when the *AGC ON* box is checked, the handset AGC is enabled.

In addition to the handset input gain control, the handset microphone bias can be selected inside the Handset Section, similar to that in the *Headset Section*.

3.3.8 Cell-Phone Section

The cell-phone section is used to configure the cell-phone input gain, by using the CP_IN PGA or AGC.

When the *Cell Phone Input AGC ON* checkbox is not checked, the PGA controls the gain, from –34.5 dB to 12 dB, and in 0.5 dB steps if the soft-stepping option was selected. The cell-phone input is muted when the Mute box under the slider is checked.

When the *AGC ON* box is checked, the cell-phone input AGC is enabled. Refer to the TLV320AIC29 data sheet or the appropriate application report(s) for setting and using the AGC.

At the TLV320AIC29 device, both CP_IN and CP_OUT signals can be at single-ended or differential mode.

3.3.9 Sidetone Section

The TLV320AIC29 has an analog sidetone circuit. The audio outputs of theTLV320AIC29 include a mixer so that the sidetone can be mixed with the audio output signals, in proportion to their respective volume settings.

The sidetone is enabled when the *PowerUp* box is checked. Its volume can be adjusted by the analog volume control slider, ranging from –34.5 dB to 12 dB, in 0.5-dB steps if the soft-stepping option is used. The sidetone is muted when the *Mute* box under the slider is checked.

At the EVM power up, the sidetone is powered-up by default.

3.3.10 Keyclick Section

When the *Enable Key Click* box is checked, a clicking sound is heard when an audio-related setting is selected or checked in the Audio 1, Audio 2 and the Audio Effects Filters screens.

The volume, frequency, and duration (length) of this keyclick can be adjusted using the corresponding slider and selectors.

At the EVM power up, the keyclick is enabled by default.

3.3.11 Buzz Input Section

The buzzer input from the cell phone can be routed to TLV320AIC29 through the BUZZ_IN pin, if the *PowerDown* checkbox is not selected. This input path supports the PGA range of from –45 dB to 0 dB, in 3 dB steps if the soft-stepping option is selected.

3.3.12 Audio Effects

The programmable Audio Effects filters coefficients of the TLV320AIC29 can be accessed at the *Audio Effect Filters* screen, as shown at the above Figure 8.

Different filter coefficients can be loaded for left and right channels, although typically they are set to the same values.

If changes are made to coefficient values directly, the response can be viewed on the graph by pressing the *View Response* button. It is recommended that the user view the response before downloading values to the TLV320AIC29, as some values can cause clipping or oscillation of the filter. The filter equation is described in the TLV320AIC29 data sheet. When the data entered is outside the acceptable range, a warning window appears to indicate the improper coefficient entered, as shown in Figure 9.

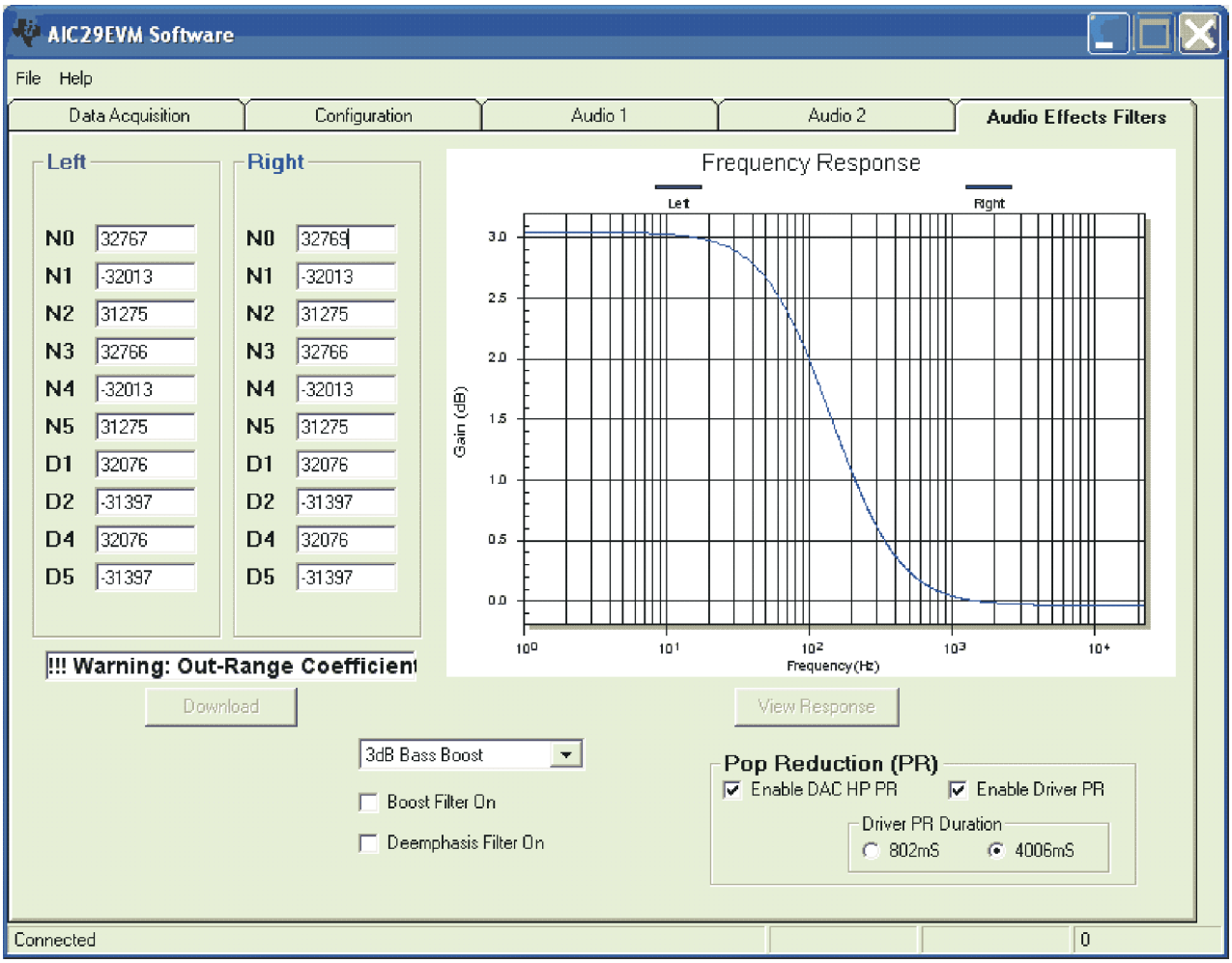

Figure 9. Audio Effect Screen With Bad Data

In addition to the direct coefficient settings previously described, there are six preconfigured filters designed with the EVM software, selectable using the drop-down list of this screen. On selection, the coefficients are updated along with the graph of the filter response to the selection. However, nothing is loaded into the TLV320AIC29 until the *Download* button is pressed. Checking the *Boost Filter* box enables the filter selected.

3.3.13 De-emphasis Filter

In addition to the boost filter, a de-emphasis filter is provided by TLV320AIC29 for the audio DAC. Checking the *Deemphasis Filter On* box enables the filter.

3.3.14 Power-Up Pop Reductions

Settings on this tab can reduce the pop noise heard at the moment the power is brought up to the output circuit of the TLV320AIC29. The pop noise reduction can be set on the DAC or the analog output driver circuit. Click on the *Enable DAC HP PR* checkbox to enable the DAC pop-reduction feature, and the *Enable Driver PR* checkbox to enable the output driver pop-reduction feature. Change the *Driver PR Duration* to set and optimize the noise reduction effects.

4 Other board Level Connections

This chapter describes the connectors of the TLV320AIC29 EVM-PDK. Using these board level connections, the TLV320AIC29 EVM can work stand-alone or as the daughter-board of the USBMODEVM.

4.1 Analog Interface

For maximum flexibility, the TLV320AIC29EVM is designed for easy interface to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 2x10-pin dual row header/socket combination at J1 and J2. These headers/sockets provide access to the analog input and output pins of the device. Table 3 summarizes the analog interface pinout for the TLV320AIC29EVM.

Table 3. Analog Interface Pinout

Pin Number	Signal	Description
J1.1	CP_IN+	Input from cell-phone module (+)
J1.2	NC	Not connected
J1.3	CP_IN–	Input from cell-phone module (–)
J1.4	NC	Not connected
J1.5	CP_OUT+	Output to cell-phone module (+)
J1.6	NC	Not connected
J1.7	CP_OUT–	Output to cell-phone module (–)
J1.8	NC	Not connected
J1.9	AGND	Analog ground
J1.10	VBAT	Battery monitor input
J1.11	AGND	Analog ground
J1.12	AUX1	First auxiliary input
J1.13	AGND	Analog ground
J1.14	NC	Not connected
J1.15	NC	Not connected
J1.16	AUX2	Second auxiliary input
J1.17	AGND	Analog ground
J1.18	AGND	Analog ground
J1.19	AGND	Analog ground
J1.20	REF+	Reference Voltage
J2.1	OUT32N	Receiver driver output (–)
J2.2	SPK1	Headset driver output (1) /receiver driver output (+)
J2.3	VGND	Virtual ground for audio outputs
J2.4	SPK2	Headset driver output (2)
J2.5	OUT8N	Loudspeaker driver output (–)
J2.6	OUT8P	Loudspeaker driver output (+)
J2.7	MICBIAS_HED	Headset microphone bias voltage
J2.8	MICIN_HED	Headset microphone input

Table 3. Analog Interface Pinout (continued)

Pin Number	Signal	Description
J2.9	AGND	Analog ground
J2.10	MIC_DETECT_IN	Microphone detect input
J2.11	AGND	Analog ground
J2.12	SPKFC	Driver feedback/speaker detect input
J2.13	AGND	Analog ground
J2.14	MICIN_HND	Handset microphone input
J2.15	NC	Not connected
J2.16	MICBIAS_HND	Handset microphone bias voltage
J2.17	AGND	Analog ground
J2.18	NC	Not connected
J2.19	AGND	Analog ground
J2.20	NC	Not connected

In addition to the analog headers, the analog inputs and outputs may also be accessed through alternate connectors, either screw terminals or audio jacks, listed in Table 4.

Table 4. Analog Connectors

	Description	Pin1	Pin2	Pin3	Pin4	Pin5
J7	External Inputs	VBAT	AUX1	AUX2	AGN	–
J9	Cell-phone In/Out	CP_IN/CP_IN+	BZ_IN/CP_IN–	CP_OUT+	CP_OUT–	AGND
J10	External MIC Input	MICIN_HND	Onboard MIC	Onboard MIC	MICBIAS_HND	AGND
J11	Headset	MICIN_HED	SPK2	SPK1	VGND/GND	–
J12	Receiver (OUT32)	OUT32N	OUT32P	–	–	–
J13	Loud-speaker (OUT8)	OUT8N	OUT8P	–	–	–

4.2 Digital Interface

The TLV320AIC29EVM is designed to easily interface with multiple control platforms. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 2x10-pin dual row header/socket combination at J4 and J5. These headers/sockets provide access to the digital control and serial data pins of the device. Table 5 summarizes the digital interface pinout for the TLV320AIC29EVM.

Table 5. Digital Interface Pinout

Pin Number	Signal	Description
J4.1	NC	Not Connected
J4.2	GPIO1	General purpose I/O 1
J4.3	SCLK	SPI Interface serial clock input
J4.4	DGND	Digital ground
J4.5	NC	Not Connected
J4.6	GPIO2	General purpose I/O 2
J4.7	/SS	SPI Interface slave select input
J4.8	/RESET	Selectable to TLV320AIC29 reset
J4.9	NC	Not Connected
J4.10	DGND	Digital ground
J4.11	MOSI	SPI serial data mater-OUT-slave-IN
J4.12	NC	Not Connected
J4.13	MISO	SPI serial data mater-IN-slave-OUT
J4.14	/RESET	TLV320AIC29 reset

Table 5. Digital Interface Pinout (continued)

Pin Number	Signal	Description
J4.15	/DAV	/data-available output
J4.16	SCL	I2C interface clock line
J4.17	NC	Not Connected
J4.18	DGND	Digital ground
J4.19	/PWR_DN	Hardware power down input
J4.20	SDA	I2C interface data line
J5.1	NC	Not Connected
J5.2	NC	Not Connected
J5.3	BCLK	I2S interface audio bit clock
J5.4	DGND	Digital ground
J5.5	NC	Not Connected
J5.6	NC	Not Connected
J5.7	WCLK	I2S interface audio word clock
J2.8	NC	Not Connected
J5.9	NC	Not Connected
J5.10	DGND	Digital ground
J5.11	DIN	I2S interface data input
J5.12	NC	Not Connected
J5.13	DOUT	I2S interface data output
J5.14	NC	Not Connected
J5.15	NC	Not Connected
J5.16	SCL	I2C interface clock line
J5.17	MCLK	Master clock
J5.18	DGND	Digital ground
J5.19	NC	Not Connected
J5.20	SDA	I2C interface data line

4.3 Power Supplies

J3 provides power connection to the TLV320AIC29. Power is supplied on the pins listed in Table 6.

Table 6. Power Supply Pin Out

Signal	Pin Number		Signal
NC	J3.1	J3.2	NC
+5VA	J3.3	J3.4	NC
DGND	J3.5	J3.6	AGND
+1.8VD	J3.7	J3.8	NC
+3.3VD	J3.9	J3.10	+5VD

The TLV320AIC29EVM-PDK motherboard (the USB-MODEVM Interface board) supplies power to J3 of the TLV320AIC29EVM. Power for the motherboard is supplied either through its USB connection or via terminal blocks on that board.

4.3.1 Stand-Alone Operation

When used as a stand-alone EVM, power can be applied to J3 directly. The user must reference the supplies to the appropriate grounds on that connector.

CAUTION

Verify that all power supplies are within the safe operating limits shown on the TLV320AIC29 data sheet before applying power to the EVM.

4.3.2 USB-MODEVM Interface Power

The USB-MODEVM Interface board can be powered from several different sources:

- USB
- 6 VDC - 10 VDC AC/DC external wall supply (not included)
- Lab power supply

When powered from the USB connection, JMP6 must have a shunt from pins 1–2 (this is the default factory configuration). When powered from 6 V-10 VDC, either through the J8 terminal block or the J9 barrel jack, JMP6 must have a shunt installed on pins 2-3. If power is applied in any of these ways, onboard regulators generate the required supply voltages, and no additional power supplies are necessary.

If lab supplies are used to provide the individual voltages required by the USB-MODEVM Interface, JMP6 must have no shunt installed. Voltages are then applied to J2 (+5VA), J3 (+5VD), J4 (+1.8VD), and J5 (+3.3VD). The +1.8VD and +3.3VD can also be generated on the board by the onboard regulators from the +5VD supply; to enable this configuration, the switches on SW1 need to be set to enable the regulators by placing them in the ON position (lower position, looking at the board with text reading right-side up). If +1.8VD and +3.3VD are supplied externally, disable the onboard regulators by placing SW1 switches in the OFF position.

Each power supply voltage has an LED (D1–D7) that illuminates when the power supply is active.

4.4 External Voltage Reference

If the external voltage reference is used, the reference can be input to the TLV320AIC29 device through the J8 terminal block.

5 Physical Description

This chapter contains the bill of materials, the TLV320AIC29 EVM board layout, and the schematics.

5.1 Bill of Materials

Table 7. TLV320AIC29EVM Bill of Materials

Item	Qty	Value	Ref. Des.	Description	Vendor	Part number
1	2	0 Ω	R13, R14	1/8 W 5% Chip Resistor	Panasonic	ERJ-6GEY0R00V
Not Installed	4	0 Ω	R9-R12	1/8 W 5% Chip Resistor	Panasonic	ERJ-6GEY0R00V
2	1	0 Ω	R25, R27	1/4 W 5% Chip Resistor	Panasonic	ERJ-8GEY0R00V
3	1	220 Ω	R15	1/8 W 5% Chip Resistor	Panasonic	ERJ-6GEYJ221V
4	1	2.2 KΩ	R26	1/4 W 5% Chip Resistor	Panasonic	ERJ-8GEYJ222V
5	3	2.7 KΩ	R7, R28, R29	1/10 W 5% Chip Resistor	Panasonic	ERJ-3GEYJ272V
6	1	2.7 KΩ	R8	1/4 W 5% Chip Resistor	Panasonic	ERJ-8GEYJ272V
7	1	30.1 KΩ	R6	1/16 W 1% Chip Resistor	Panasonic	ERJ-3EKF3012V
8	1	69.8 KΩ	R5	1/16 W 1% Chip Resistor	Panasonic	ERJ-3EKF6982V
9	4	100 KΩ	R1, R2, R3, R4	1/10 W 5% Chip Resistor	Panasonic	ERJ-3GEYJ104V
Not Installed	9	NI	R16-R24			
10	12	0.1 µF	C7-C9, C11-C19	25 V Ceramic Chip Capacitor, +/ - 10%, X7R	TDK	C1608X7R1E104KT
Not Installed	7	0.1 µF	C20-C26	25 V Ceramic Chip Capacitor, +/ - 10%, X7R	TDK	C2012X7R1E104KT
11	2	0.1 µF	C10, C35	100 V Ceramic Chip Capacitor, +/ - 10%, X7R	TDK	C3216X7R2A104KT
12	1	0.33 µF	C1	10 V Ceramic Chip Capacitor, +/ - 10%, X5R	TDK	C1608X5R1A334KT
13	10	10 µF	C2-C6, C27-C31	6.3 V Ceramic Chip Capacitor, +/ - 10%, X5R	TDK	C3216X5R0J106KT
14	2	47 µF	C36, C37	6.3 V Ceramic Chip Capacitor, +/ - 20%, X5R	TDK	C3225X5R0J476MT
Not Installed	3	NI	C32, C33, C34			
15	1		U3	Audio Codec	Texas Instruments	TLV320AIC29IRGZ
16	1		U2	64K, I2C EEPROM	Microchip	24AA64-I/SN
17	1		U1	Dual Output LDO Voltage Regulator	Texas Instruments	TPS767D301PWPG4
18	1		J7	Screw Terminal Block, 4 Position	On Shore Technology	ED555/4DS
Not Installed	1		J6	Screw Terminal Block, 4 Position	On Shore Technology	ED555/4DS
19	1		J9	Screw Terminal Block, 5 Position	On Shore Technology	ED555/5DS
20	3		J8, J12, J13	Screw Terminal Block, 2 Position	On Shore Technology	ED555/2DS
21	1		J10	3.5 mm Audio Jack, T-R-S, SMD	CUI Inc.	SJ1-3515-SMT
22	1		J11	3.5 mm Audio Jack, T-R-S-G, Thru-Hole	CUI Inc.	SJ-43514
23	4		J1A, J2A, J4A, J5A	20 Pin SMT Plug	Samtec	TSM-110-01-L-DV-P
24	4		J1B, J2B, J4B, J5B	20 pin SMT Socket	Samtec	SSW-110-22-F-D-VS-K

Table 7. TLV320AIC29EVM Bill of Materials (continued)

Item	Qty	Value	Ref. Des.	Description	Vendor	Part number
25	1		J3A	10 Pin SMT Plug	Samtec	TSM-105-01-L-DV-P
26	1		J3B	10 pin SMT Socket	Samtec	SSW-105-22-F-D-VS-K
27	1		N/A	TLV320AIC29EVM PWB (must be RoHS compliant)	Texas Instruments	6478197
Not Installed	4	NI	D1, D2, D3, D4	Schottky Barrier Diode, Series Configuration	Diodes Inc.	BAT54S-7-F
28	3		JMP1, JMP2, JMP11	2 Position Jumper , 0 .1" spacing	Samtec	TSW-102-07-L-S
Not Installed	2		JMP3, JMP4	2 Position Jumper , 0 .1" spacing	Samtec	TSW-102-07-L-S
29	2		JMP13, JMP14	3 Position Jumper , 0 .1" spacing	Samtec	TSW-103-07-L-S
30	2		JMP10, JMP15	3 X 2 Position Header, 0 .1" spacing	Samtec	TSW-103-07-L-D
31	6		JMP5-JMP9, JMP12	Bus Wire, 18-22 Gauge		
32	1		MK1	Omnidirectional Microphone Cartridge	Knowles Acoustics	MD9745APZ-F
33	1		SW1	4PDT Right Angle Switch	E-Switch	EG4208
Not Installed	42		TP3-TP19, TP21-TP33, TP35-TP46	Miniature Test Point Terminal	Keystone Electronics	5000
34	4		TP1, TP2, TP20, TP34	Miniature Test Point Large Loop Terminal	Keystone Electronics	5011
35	10		N/A	Jumper Top	Samtec	SNT-100-BK-T

5.2 TLV320AIC29 EVM (Daughter) Board Layout

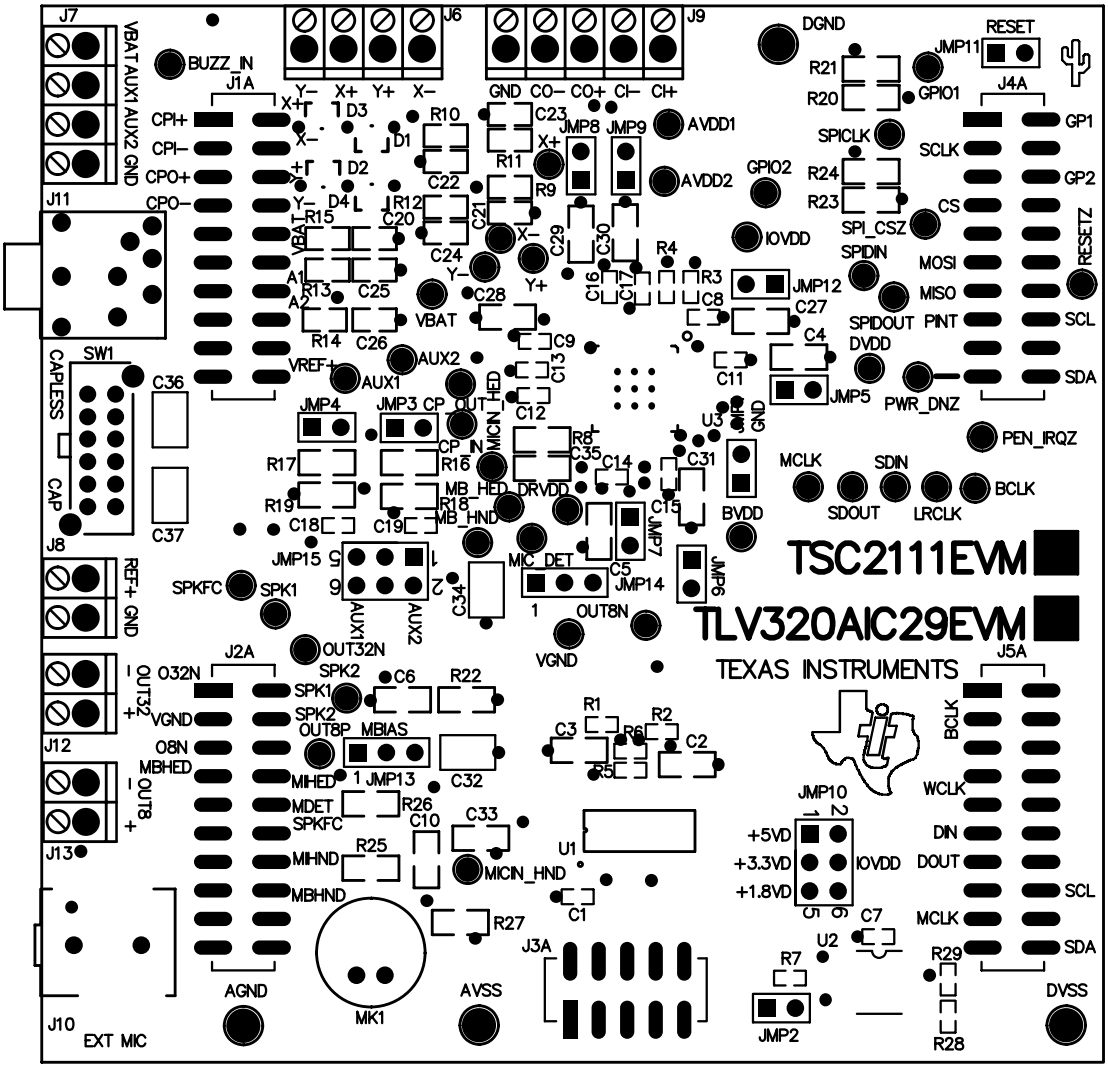

Figure 10. Component Layout

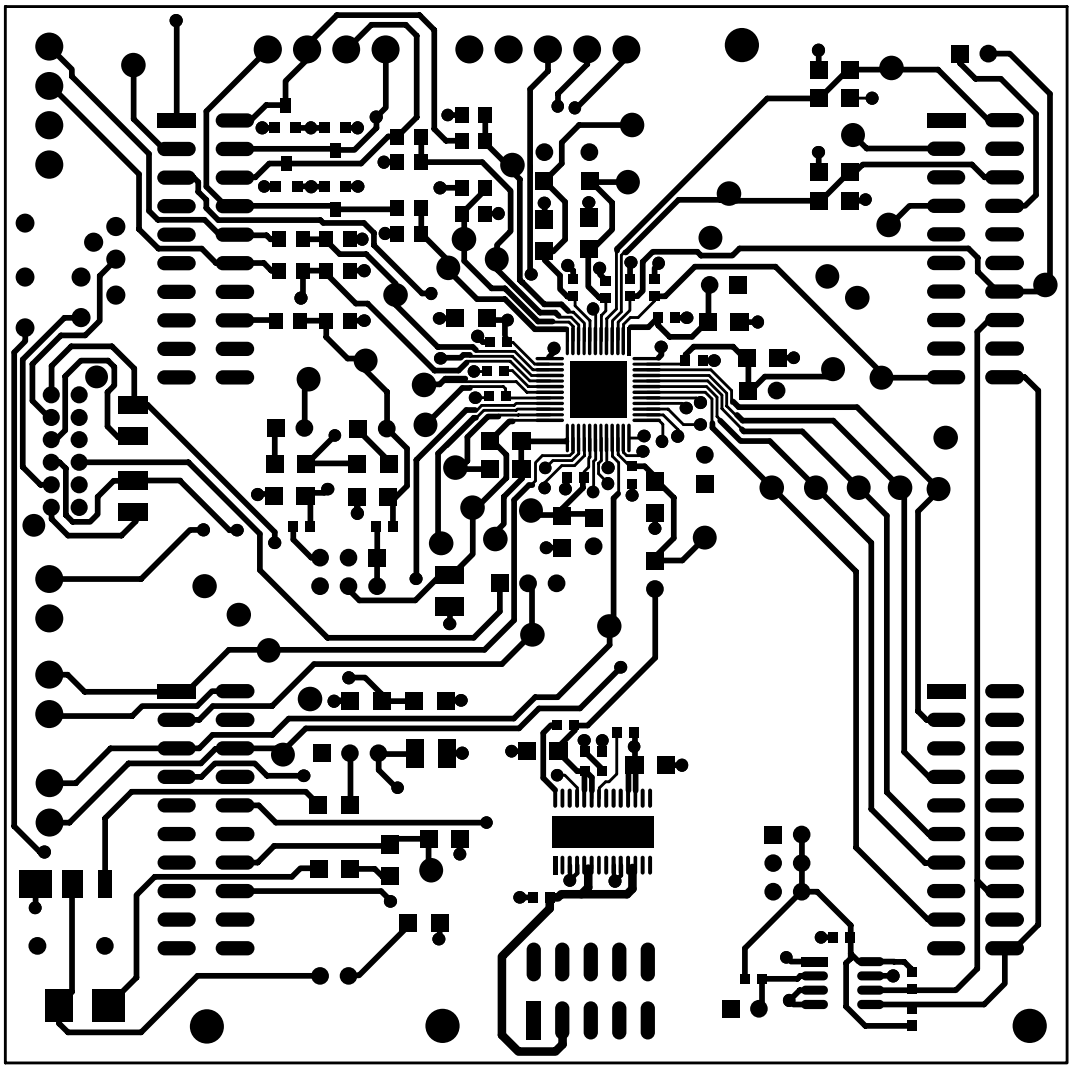

Figure 11. Top PCB Layer

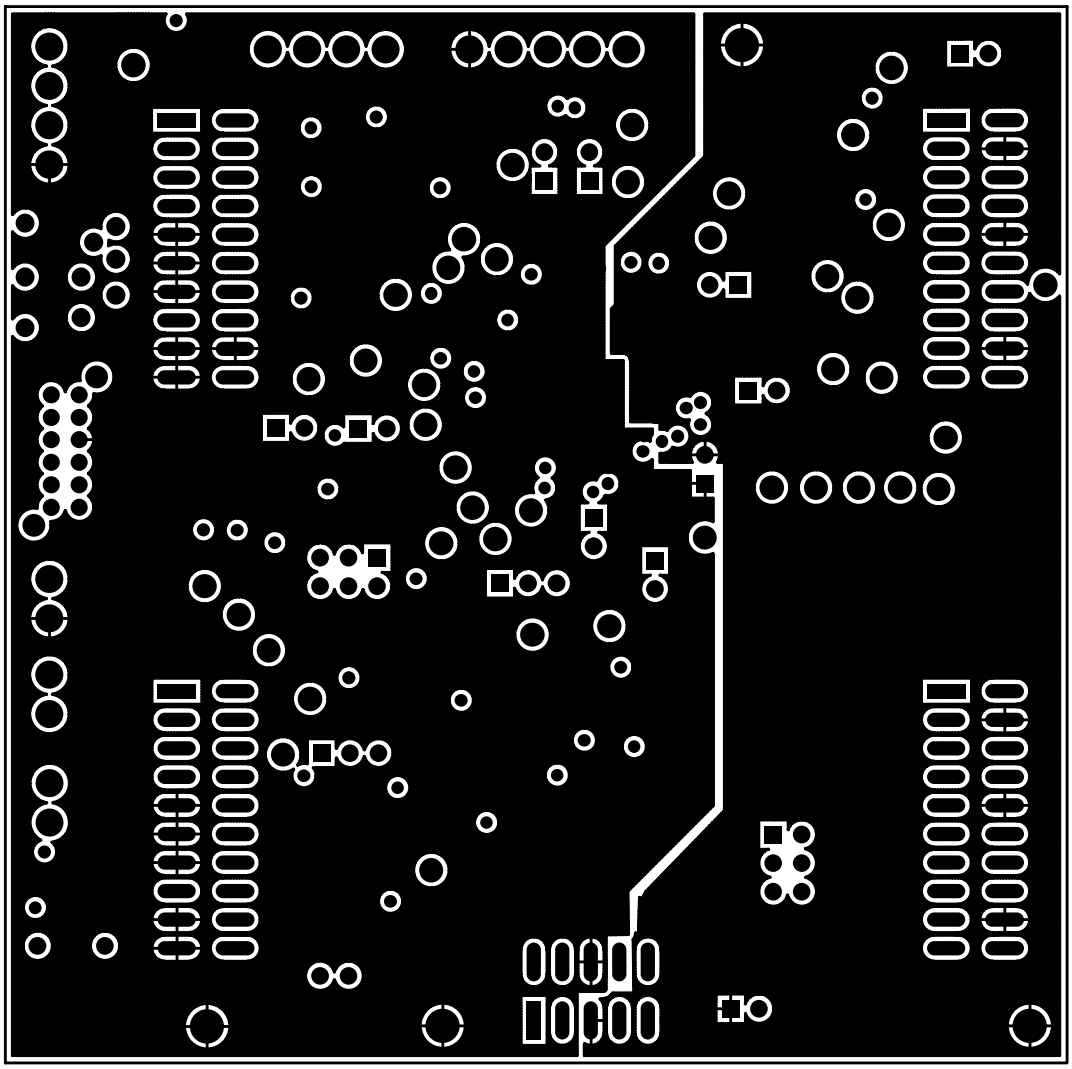

Figure 12. Power/Ground Plane 1

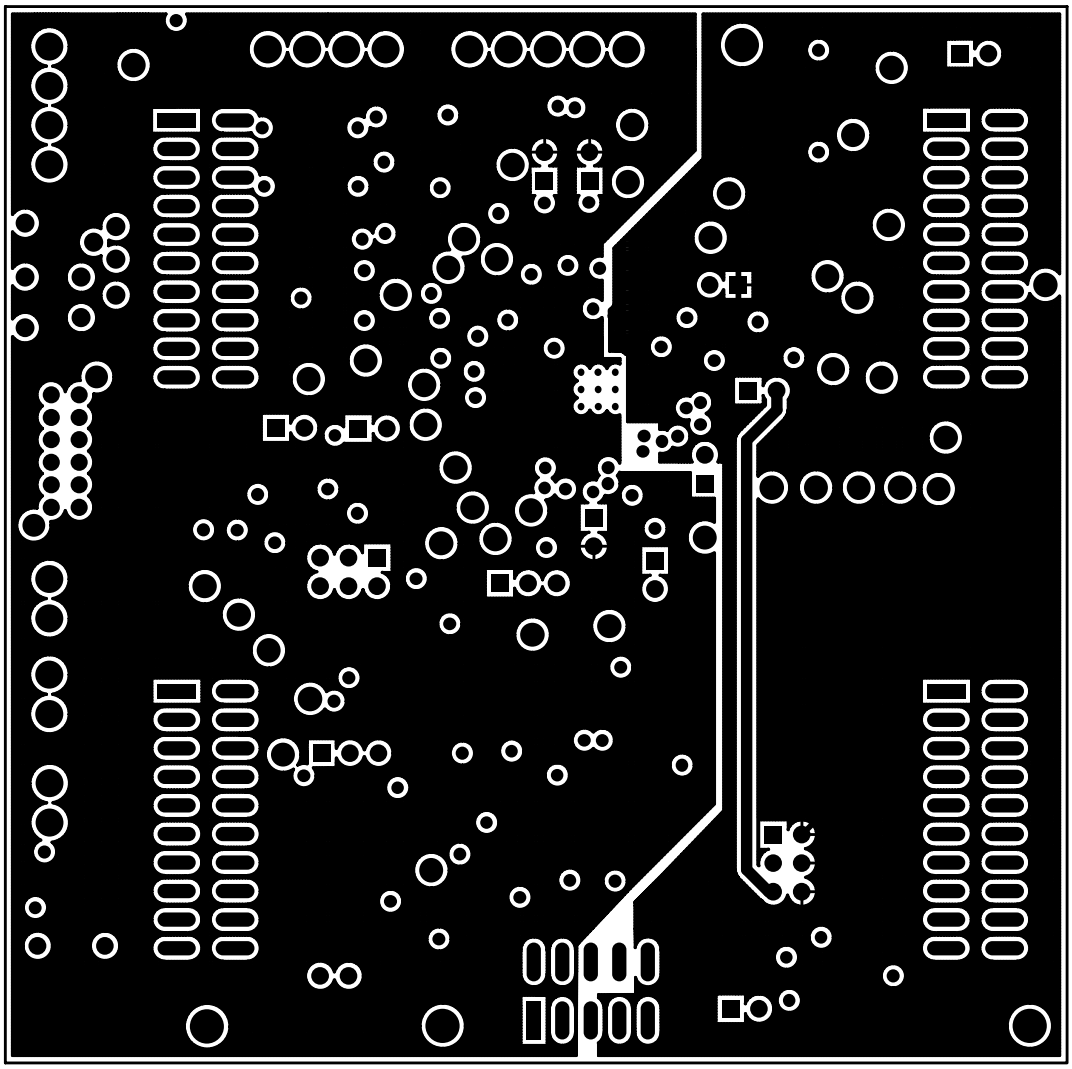

Figure 13. Power/Ground Plane 2

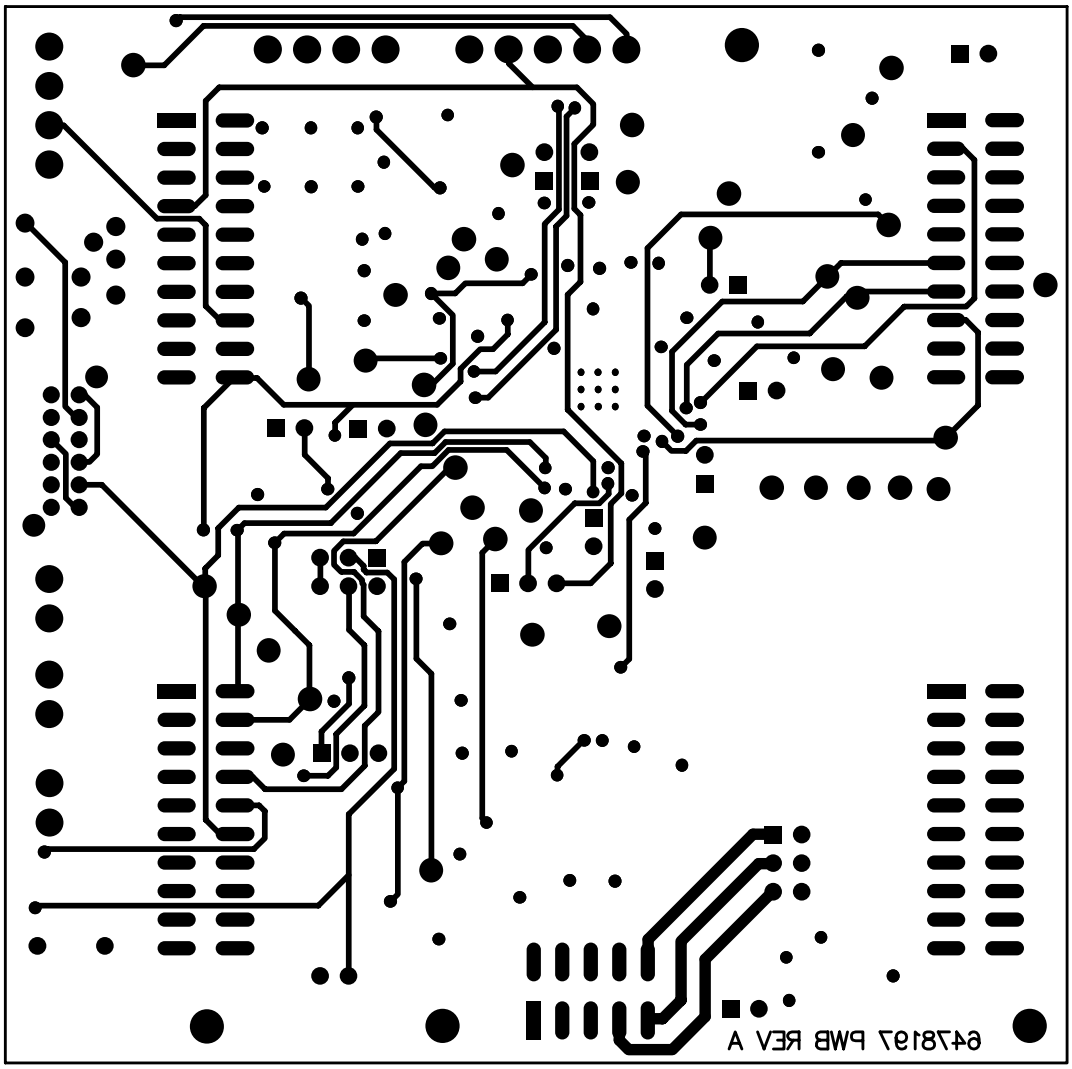

Figure 14. Bottom PCB Layer

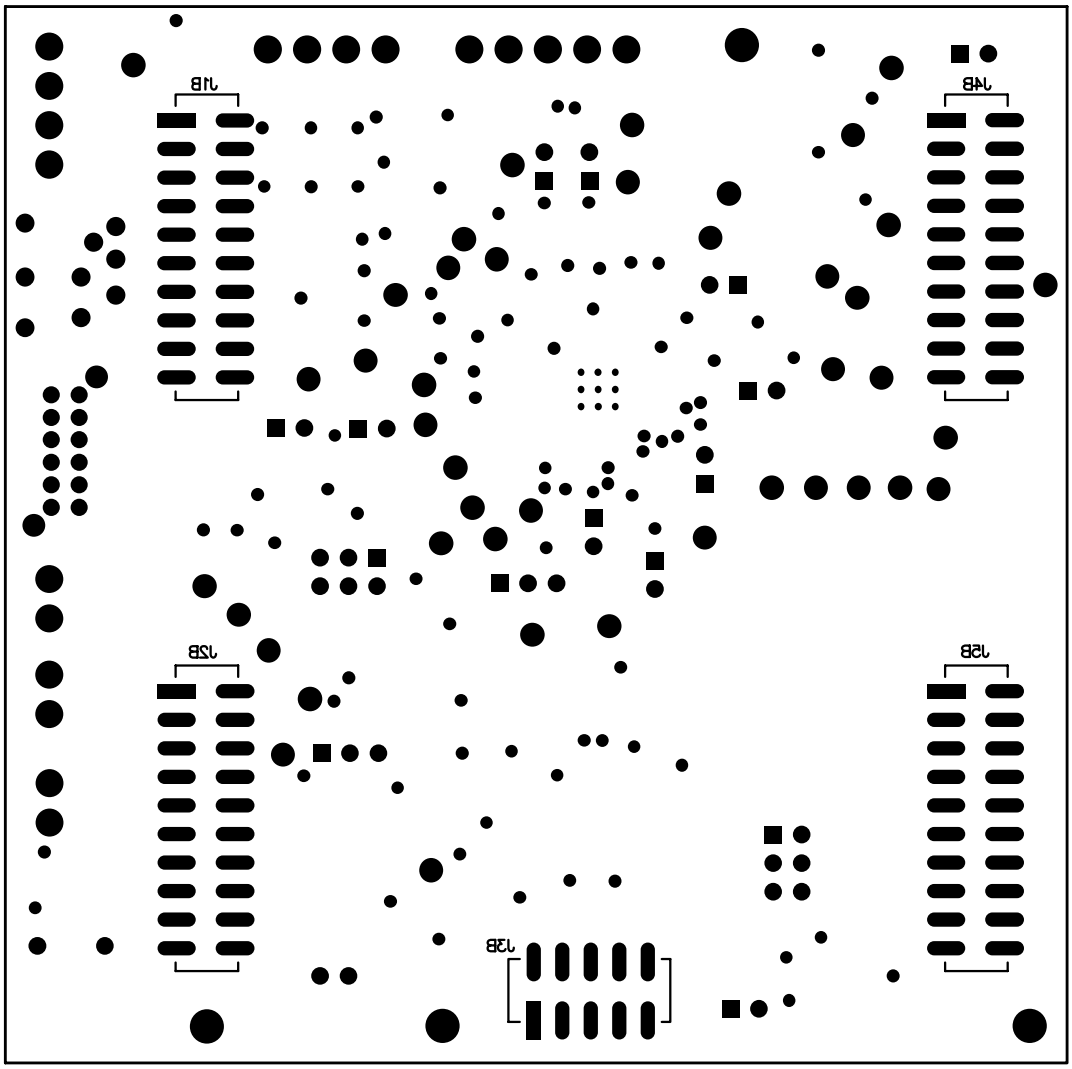

Figure 15. Bottom Silkscreen and Solder Mask

5.3 Schematics

Schematic diagrams of the TSC2111EVM/TLV320AIC29EVM daughter board show the TLV320AIC29 analog connections to the external Input/output devices (such as the headphone, or microphone); and the digital connections to the USB-MODEVM board and other external digital devices through its connectors.

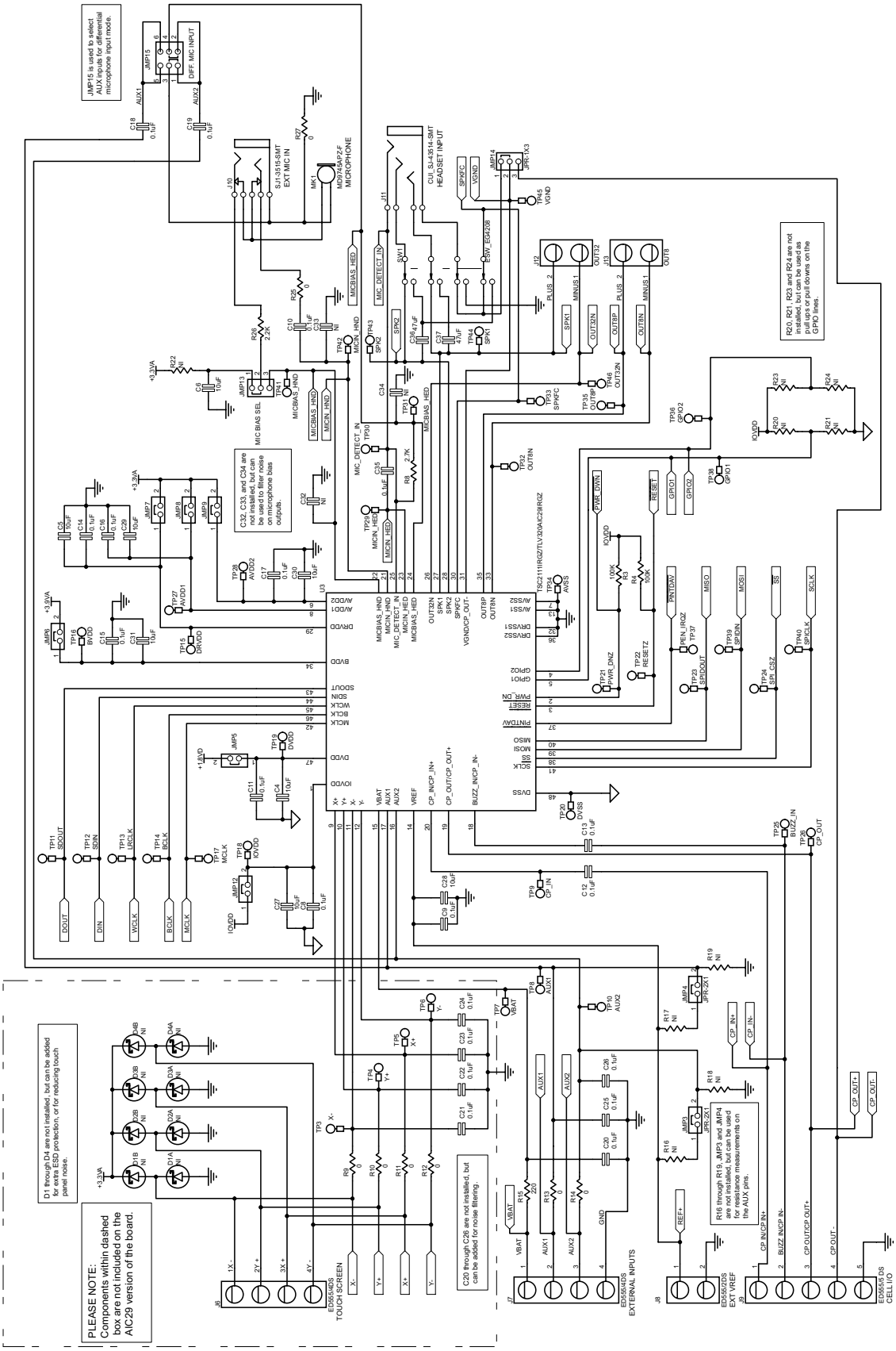

Figure 16. TSC2111EVM/TLV320AIC29EVM Schematic, Page 1

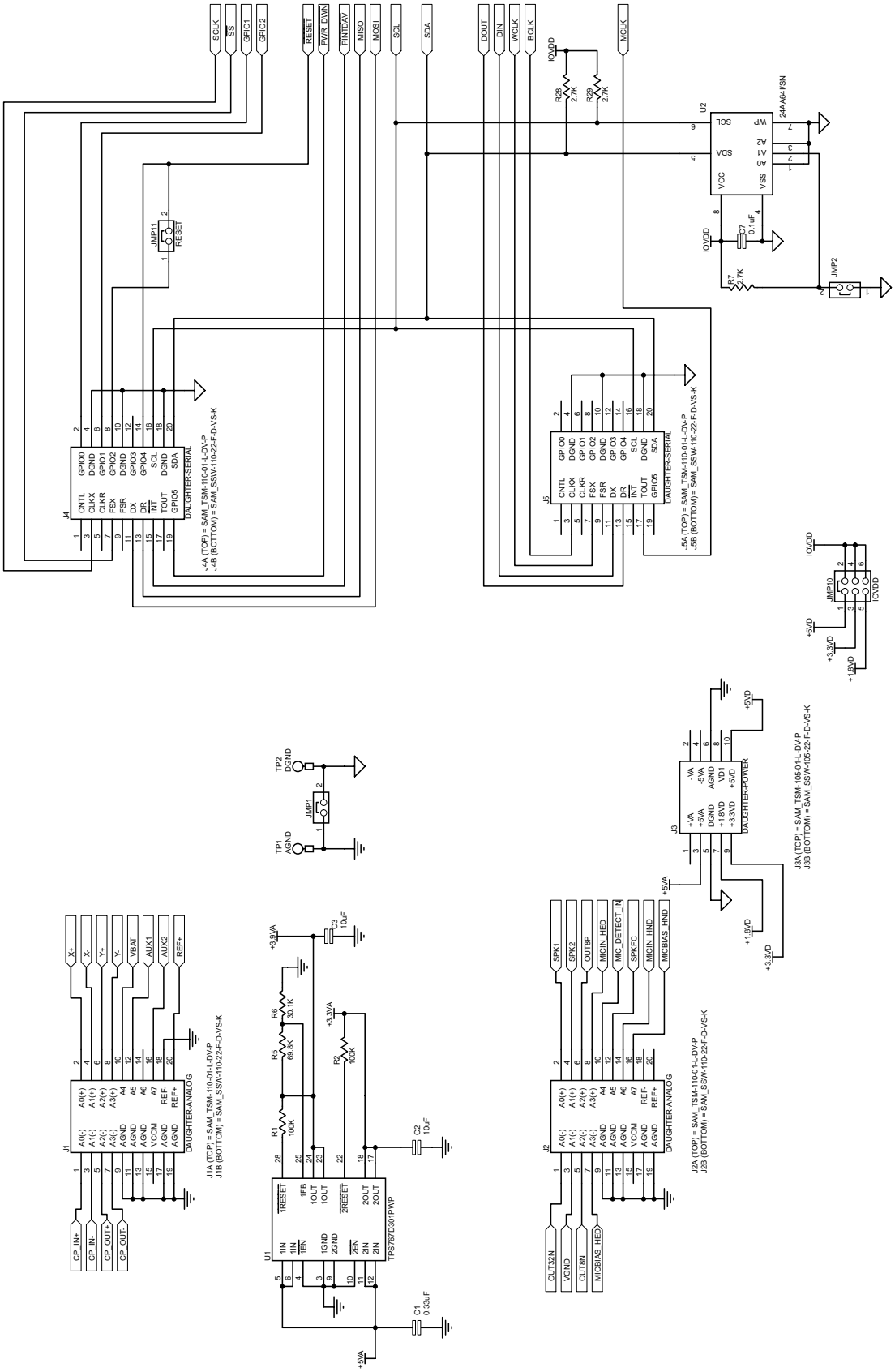

Figure 17. TSC2111EVM/TLV320AIC29EVM Schematic, Page 2

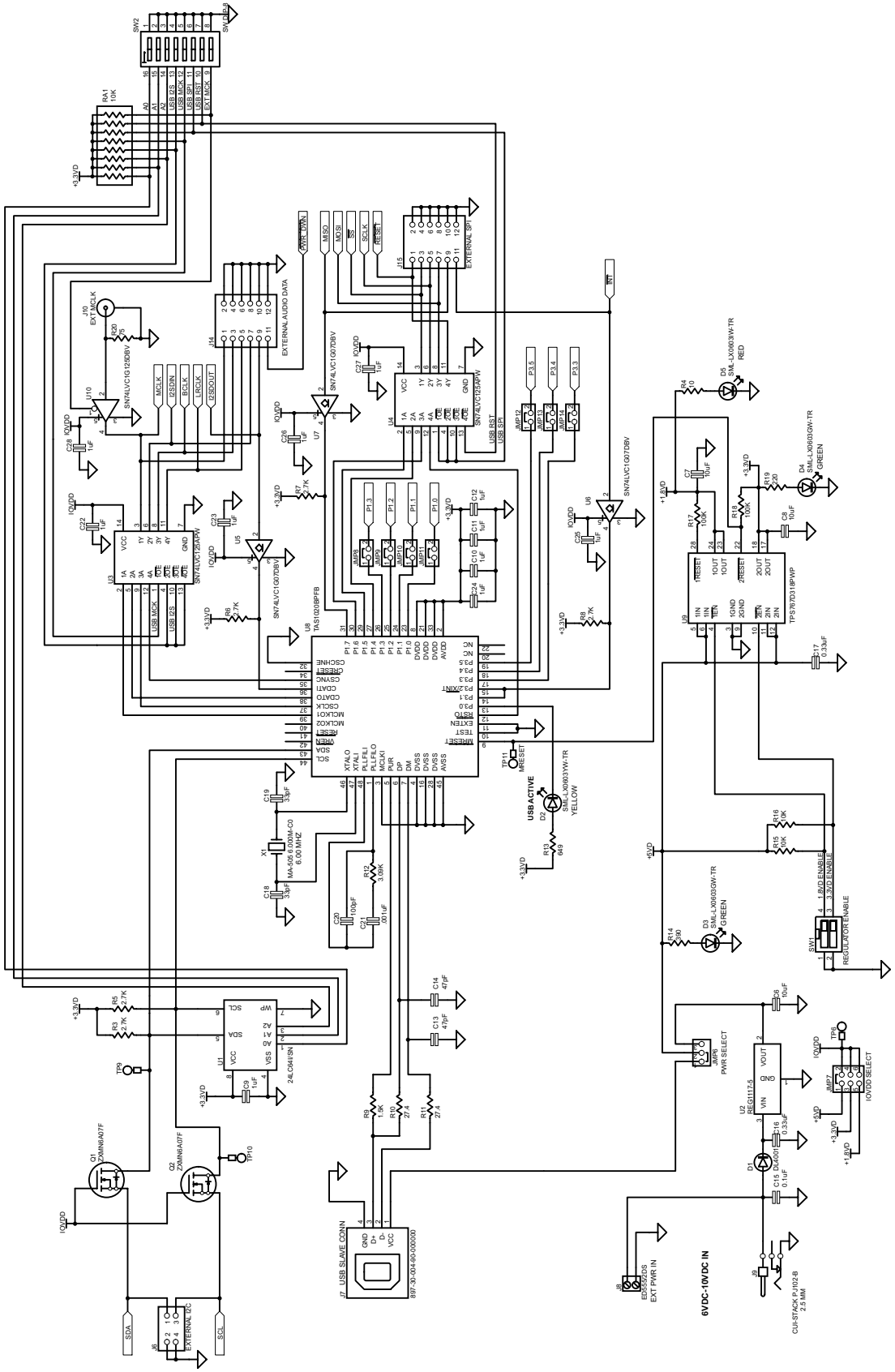

Figure 18. USB Board Schematic, Page 1

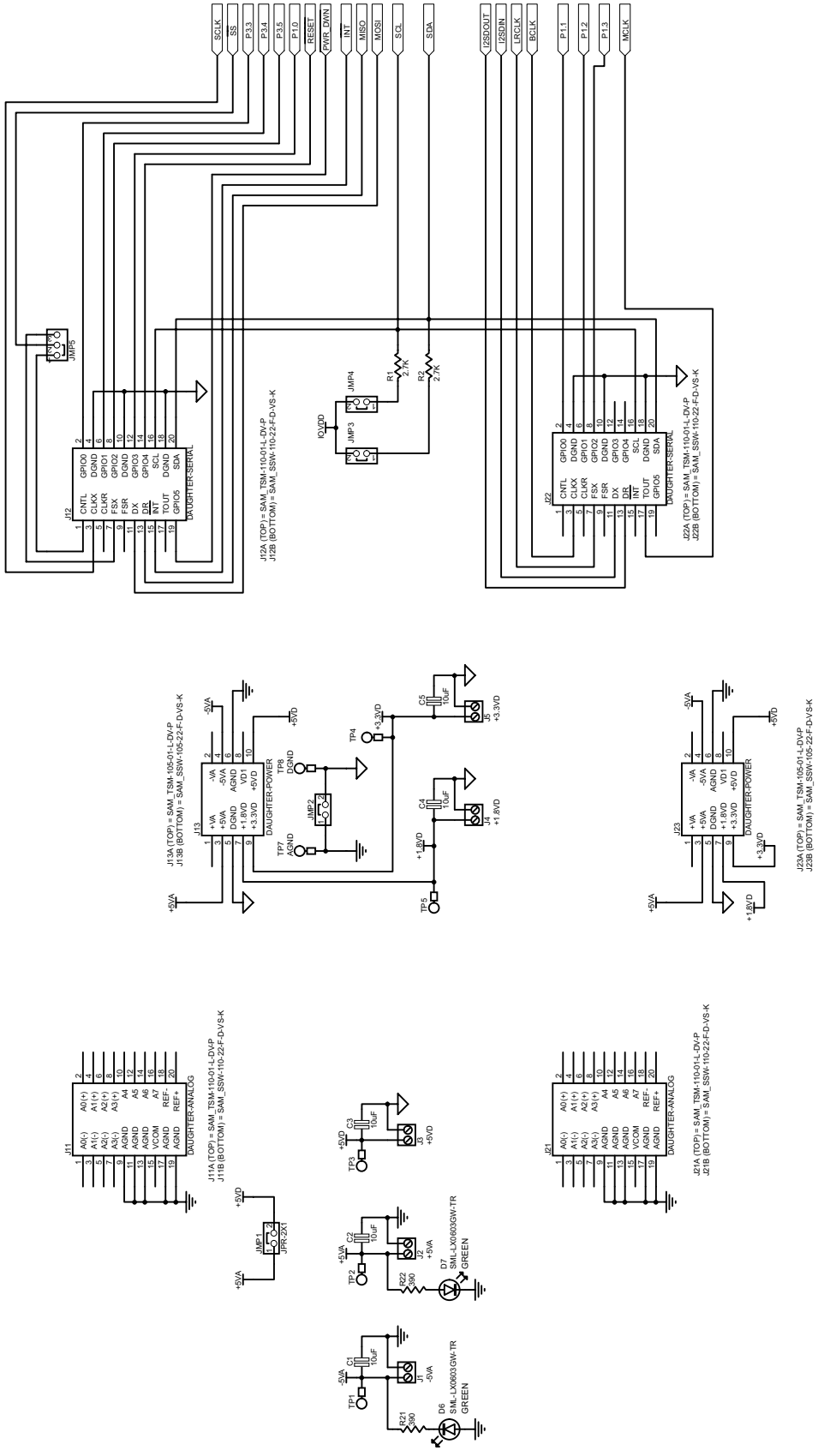

Figure 19. USB Board Schematic, Page 2

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