

TPS61120EVM-205

TPS61121EVM-205

TPS61122EVM-205

For Dual Output, Single-Cell Boost Converter

User's Guide

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

EVM IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation kit being sold by TI is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not considered by TI to be fit for commercial use. As such, the goods being provided may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety measures typically found in the end product incorporating the goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may not meet the technical requirements of the directive.

Should this evaluation kit not meet the specifications indicated in the EVM User's Guide, the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Please be aware that the products received may not be regulatory compliant or agency certified (FCC, UL, CE, etc.). Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive**.

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein**.

Please read the EVM User's Guide and, specifically, the EVM Warnings and Restrictions notice in the EVM User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact the TI application engineer.

Persons handling the product must have electronics training and observe good laboratory practice standards.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V to 5.5 V and the output voltage range of 2.5 V to 5.5 V at the dc-dc output and 0.9 V to 5.5 V at the LDO output.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 100°C. The EVM is designed to operate properly with certain components above 100°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Contents

1	Introduction	1-1
2	Setup of the EVMs	2-1
2.1	Evaluation With the TPS6112x EVM	2-2
2.1.1	Enable (EN)	2-2
2.1.2	LDO Enable (LDOEN) Jumper	2-2
2.1.3	Power Save Mode Enable (SKIPEN) Jumper	2-2
2.1.4	LBI/LBO Comparator	2-2
2.1.5	Power Good Output	2-2
3	Bill of Materials, PCB Layout and Schematic	3-1
3.1	Bill of Materials	3-2
3.2	PCB Layout	3-3
3.3	Schematic	3-4

Figures

3-1	Component Placement	3-3
3-2	Top Layer	3-3
3-3	Bottom Layer	3-4
3-4	TPS6112x EVM Circuit Diagram	3-4

Tables

1-1	Orderable EVMs	1-1
3-1	Bill of Materials	3-2

Introduction

The Texas Instruments TPS61120 to TPS61122 evaluation modules (EVM) for high-efficiency boost converters help designers to evaluate the different operating modes and the performance of the device. Refer to Table 1–1 for the various EVMs available in this family.

If any other output voltage configuration is to be evaluated, the TPS61120 adjustable output voltage version can be set up to provide an output voltage between 2.5 V and 5.5 V at the output of the boost converter and between 0.9 V and 5.5 V at the LDO. Only the appropriate feedback resistor divider has to be adjusted. Also, other fixed output voltage versions of the devices can be easily evaluated using the EVM. Refer to the data sheet (SLVS427) for the various fixed output voltage options available in the TPS6112x device family. The TPS6112x has an input voltage range between 1.8 V and 5.5 V. For proper operation the maximum input voltage should not exceed the output voltage. The maximum output current is at least 100 mA, depending on the input voltage.

Table 1–1. Orderable EVMs

EVM Number	Description	
TPS61120EVM-205	Adjustable boost output voltage, set to 3.3 V	Adjustable LDO output voltage, set to 1.5 V
TPS61121EVM-205	Boost output voltage fixed at 3.3 V	LDO output voltage fixed at 1.5 V
TPS61122EVM-205	Boost output voltage fixed at 3.6 V	LDO output voltage fixed at 3.3 V



Setup of the EVMs

It is important to establish all connections to the EVM before the power supply for the EVM is turned on.

- ☐ Connect a power supply (1.8 V to V_{OUT} , depending on the output voltage of the EVM) to the INPUT header
- ☐ Connect a voltmeter to the OUTPUT header
- ☐ Verify that all jumpers are set to their desired value (EN, SKIPEN, LDOEN). Default setting is EN, SKIPEN, and LDOEN to V_{BAT} .
- ☐ Turn on the power supply and verify the output voltage

Topic	Page
2.1 Evaluation With the TPS6112x EVM	2-2

2.1 Evaluation With the TPS6112x EVM

This chapter details the evaluation process and features of the EVM. For this evaluation, a load is connected to the output terminal in order to adjust the load current between 0 mA and 250 mA.

For accurate output voltage and input voltage measurements, it is important to measure the voltage on the input and output voltage terminals with Kelvin contacts or with a voltmeter connected directly to the input voltage or output voltage terminals. This eliminates any measurement errors related to voltage drops along the input and output terminal wires connected to the power supply or load.

2.1.1 Enable (EN) Jumper

This jumper is used to enable the device. Connecting the enable pin (EN) to V_{BAT} enables the part. The device is disabled when EN is set to GND. For more details refer to the data sheet.

2.1.2 LDO Enable (LDOEN) Jumper

This jumper is used to enable the integrated LDO of the device. Connecting the LDO enable pin (LDOEN) to V_{LDOIN} enables the LDO section of the part. Disabling the integrated LDO can be done by setting this jumper to GND.

2.1.3 Power Save Mode Enable (SKIPEN) Jumper

This jumper enables the device to enter into power save mode at light load, when it is set to V_{BAT} . The device automatically stops switching when the output voltage reached its upper threshold, and starts switching again, when the lower threshold of the output voltage is reached.

When disabling the power save function by setting the jumper to GND, the device stays operating in fixed frequency mode, regardless of the load current value. In this mode, however reverse current flows back to the input during light load operation, increasing power losses. The operating frequency stays constant, which implies low output voltage ripple.

2.1.4 LBI/LBO Comparator

The LBO terminal is an open drain output and has a pullup resistor, R7, connected to the output. The signal on this pins can go low as soon as the input voltage at LBI falls below the threshold of 500 mV. Refer to the more detailed description in the data sheet. The LBO output stays at high-impedance when the input voltage at LBI is above the appropriate threshold. A resistor divider (R1, R2) is used on the EVM to monitor the supply voltage.

More details about setting the low battery threshold voltage can be found in the data sheet (literature number SLVS427).

2.1.5 Power Good Output

The PG pin is an open drain output with a pullup resistor, R9, connected to the output. The signal on this pin goes high as soon as the output voltage is greater than typically 92% of the nominal voltage. The signal goes low as soon as the output voltage falls below this typical threshold. There is an implemented delay time of 30 μ s to prevent the power good output from ringing.

Bill of Materials, PCB Layout and Schematic

This chapter contains bill of materials, PCB layout of the EVM, and schematic.

Topic	Page
3.1 Bill of Materials	3-2
3.2 PCB Layout	3-3
3.3 Schematic	3-4

3.1 Bill of Materials

The bill of materials for the TPS6112x EVM is shown in Table 3–1 with adjustable and fixed output voltage versions.

More details about the design and component selection for the dc-dc converter can be found in the data sheet.

Table 3–1. Bill of Materials

Reference	Description	Manufacturer	Comments
C3	100 μ F 10 V, Low ESR tantalum size D	Vishay	591D–107X0010U2T
C1	10 μ F X5R 6.3 V, capacitor SMD1206	TDK	C3216X5R0J106M
C2, C5	2.2 μ F X5R 6.3 V, capacitor SMD0805	TDK	C2012X5R1A225M
C4			Not assembled
L1	10 μ H, WE–PD Type S	Würth Elektronik	744 778 10 Also possible: Sumida CDRH73–100 or Coiltronics DR73-100
R10	0 Ω , resistor SMD0805		
R4	180 k Ω , 1%, resistor SMD0805		TPS61120EVM
R6	180 k Ω , 1%, resistor SMD0805		TPS61120EVM
R3	1 M Ω , 1%, resistor SMD0805		TPS61120EVM
R7, R8	1 M Ω , 1%, resistor SMD0805		
R1	470 k Ω , 1%, resistor SMD0805		
R5	390 k Ω , 1%, resistor SMD0805		TPS61120EVM
	0 Ω , resistor SMD0805		TPS61121EVM and TPS61122EVM
R2	180 k Ω , 1%, resistor SMD0805		
R9			Not assembled
LDOOUT	Header 1 $\times$ 4, 0.1" pitch		
OUTPUT	Header 1 $\times$ 4, 0.1" pitch		
INPUT	Header 1 $\times$ 4, 0.1" pitch		
J7	Header 1 $\times$ 2, 0.1" pitch		
EN	Header 1 $\times$ 3, 0.1" pitch		With jumper set to VBAT
LDOEN	Header 1 $\times$ 3, 0.1" pitch		With jumper set to LDOIN
SKIPEN	Header 1 $\times$ 3, 0.1" pitch		With jumper set to VBAT
GND	Header 1 $\times$ 2, 0.1" pitch		
U1	TPS61120PW, TSSOP16	TI	TPS61120EVM–205
	TPS61121PW, TSSOP16	TI	TPS61121EVM–205
	TPS61122PW, TSSOP16	TI	TPS61122EVM–205

3.2 PCB Layout

For all switch mode power supplies the PCB layout is a critical step in the power supply design process. The figures below show the layout for the adjustable and fixed output voltage EVMs. Please refer to the data sheet for further layout guidelines. The required board area for the complete dc-to-dc converter solution takes up less than 320 mm² (16 mm × 20 mm) on a double sided PCB, as it is indicated by the rectangular on the component placement plot.

Figure 3–1. Component Placement

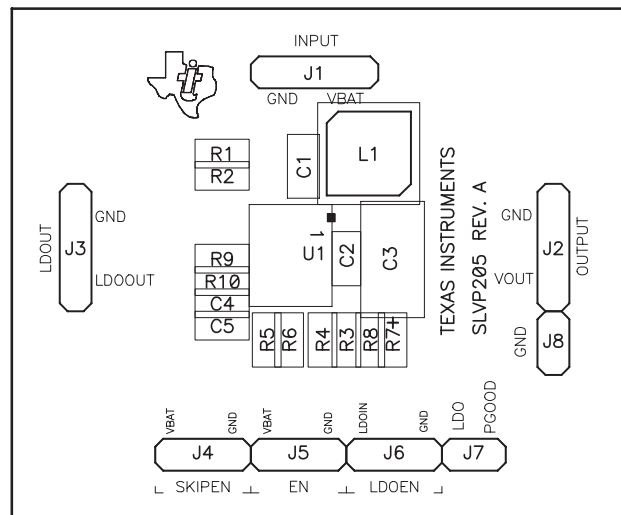


Figure 3–2. Top Layer

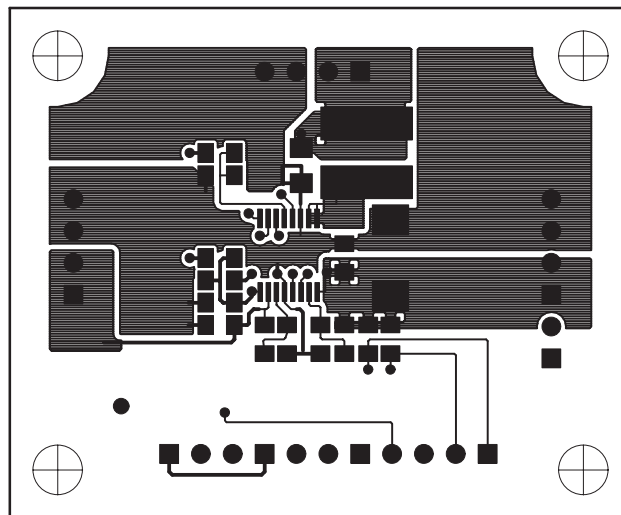
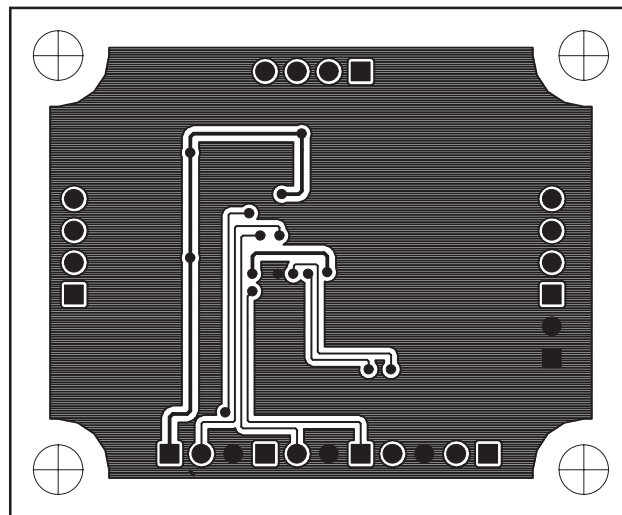


Figure 3–3. Bottom Layer



3.3 Schematic

Figure 3–4. TPS6112x EVM Circuit Diagram

