

## Low-Level Video Detector

The MC1330A is an integrated circuit featuring very linear video characteristics and wide bandwidth. Designed for color and monochrome television receivers, replacing the third IF, detector, video buffer and AFC buffer.

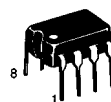
- Conversion Gain: 33 dB (Typ)
- Excellent Differential Phase and Gain
- High Rejection of IF Carrier Feedthrough
- High Video Output: 8.0 V(p-p)
- Fully Balanced Detector
- Output Temperature Compensated
- Improved Version of the MC1330

### MAXIMUM RATINGS

Rating	Value	Unit
Power Supply Voltage	24	Vdc
DC Video Output Current	5.0	mAdc
DC AFT Output Current	2.0	
Junction Temperature	150	°C
Operating Ambient Temperature Range	0 to 75	°C
Storage Temperature Range	-65 to +150	°C

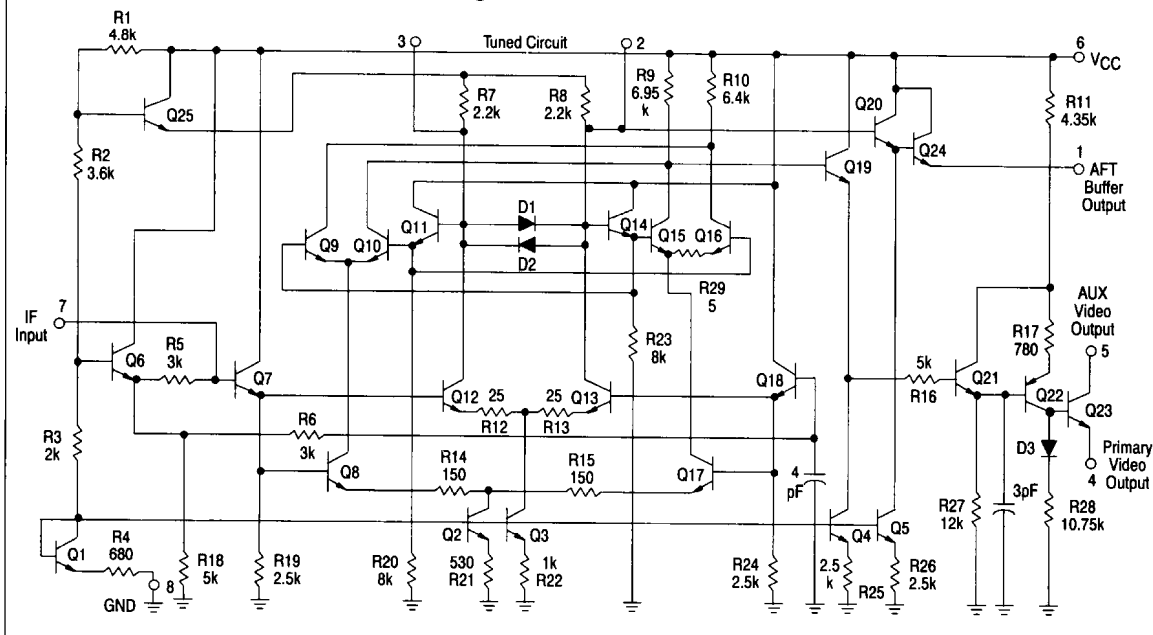
### LOW-LEVEL VIDEO DETECTOR

**SILICON MONOLITHIC  
INTEGRATED CIRCUIT**



**P SUFFIX**  
**PLASTIC PACKAGE**  
**CASE 626**

**Figure 1. Circuit Schematic**



## 9

Characteristics	Pin	Min	Typ	Max	Unit
Zero Signal DC Output Voltage	4	7.0	—	8.7	Vdc
Supply Current	5, 6	11	17.5	24	mA
Maximum Signal DC Output Voltage	4	—	0	0.5	Vdc
Conversion Gain for 1.0 Vp-p Output (30% Modulation)	7	25	36	65	mVrms
AFT Buffer Output at Carrier Frequency	1	300	475	650	mVp-p

Characteristics	Pin	Typ	Unit	
Input Resistance	7	4.9	kΩ	
Input Capacitance	7	1.5	pF	
Internal Resistance (Across Tuned Circuit)	2, 3	4.4	kΩ	
Internal Capacitance (Across Tuned Circuit)	2, 3	1.0	pF	
Negative Video Output Bandwidth (Figure10)	4	10.8	MHz	
Positive Video Output Bandwidth (Figure10)	5	2.2	MHz	
Differential Phase @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video Pin 5 Tied to Pin 6	4	7.0	Degrees	
Differential Gain @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video Pin 5 Tied to Pin 6	4	4.0	%	
Differential Phase @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video, R Pin 5 = 4.3 kΩ	4	8.0	Degrees	
Differential Gain @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video, R Pin 5 = 4.3 kΩ	4	6.0	%	
920 kHz Beat Output (dB Below 100% Modulated Video, see Figure 11) 45.75 MHz = Reference 42.17 MHz = -6.0 dB 41.25 MHz = -20 dB	4	-38	dB	
Video Output Resistance @ 1.0 MHz, 2.0 mA	4	94	Ω	
Input Overload (Carrier Level at Input to Pin 4, Primary Output to go Positive 0.1 Vdc from Ground.)	V <sub>CC</sub> = 12 Vdc V <sub>CC</sub> = 15 Vdc V <sub>CC</sub> = 20 Vdc V <sub>CC</sub> = 24 Vdc	7	2.0 2.6 3.6 4.6	V
Power Supply Voltage Range	5	10 to 24	V	

MOTOROLA LINEAR/INTERFACE ICs DEVICE DATA

# MC1330A

Figure 3. Input Admittance

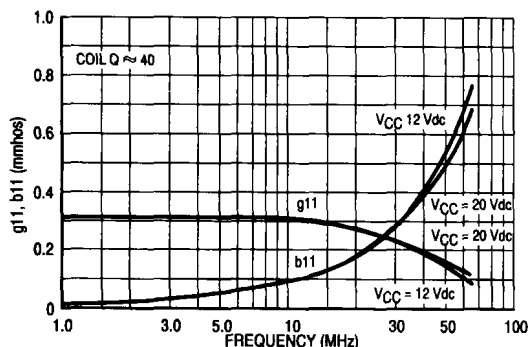
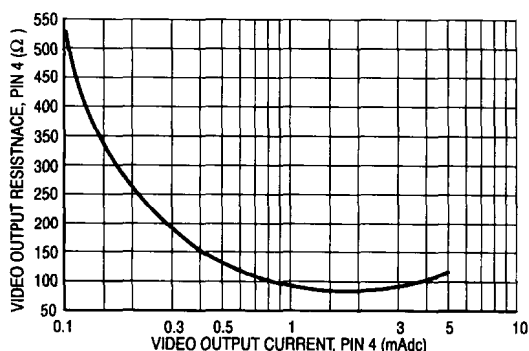


Figure 4. Video Detector Output Resistance



## CIRCUIT DESCRIPTION

The MC1330A video detector is a fully balanced multiplier detector circuit that has linear amplitude and phase characteristics. The signal is divided into two channels, one a linear amplifier and the other a limiting amplifier that provides the switching carrier for the detector.

The switching carrier has a buffered output for use in providing the AFT function.

The video amplifier output is an improved design that reduces the differential gain and phase distortion associated with previous video output systems. The output is wideband, > 8.0 MHz, with normal negative polarity.

A separate narrow bandwidth, positive video output is also provided.

Figure 5. Differential Phase and Gain Test Set Up

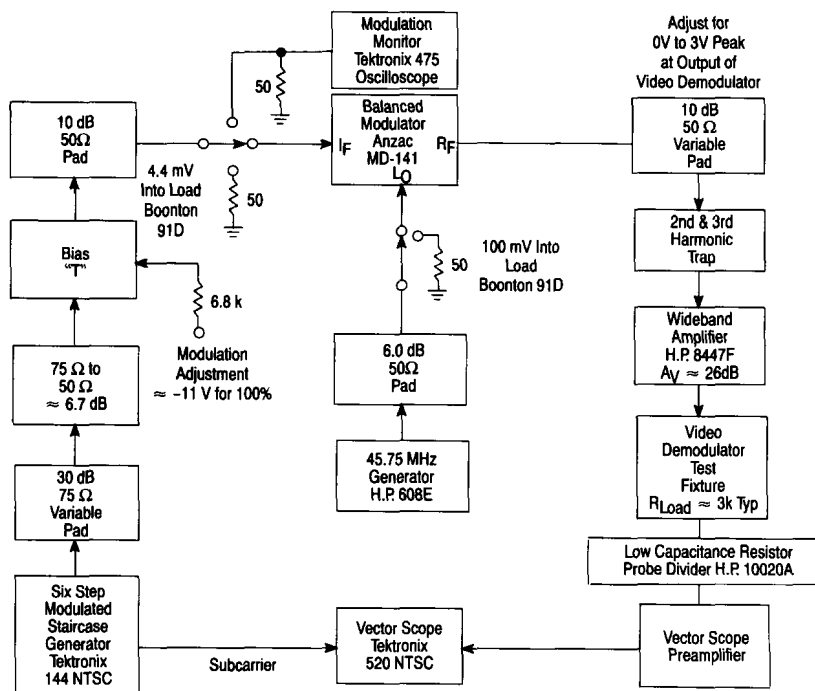


Figure 6. Output Voltage Transfer Function

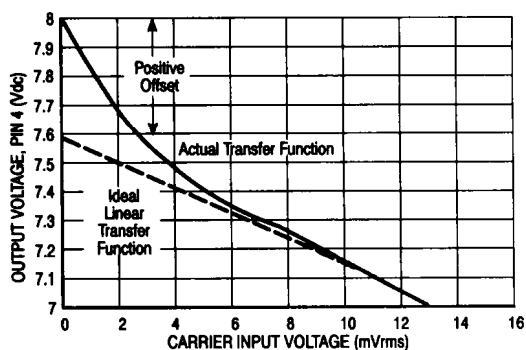


Figure 7. Output Voltage Transfer Function

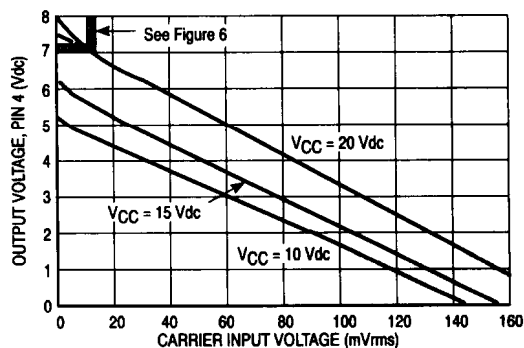


Figure 8. Output Voltage, Supply Current

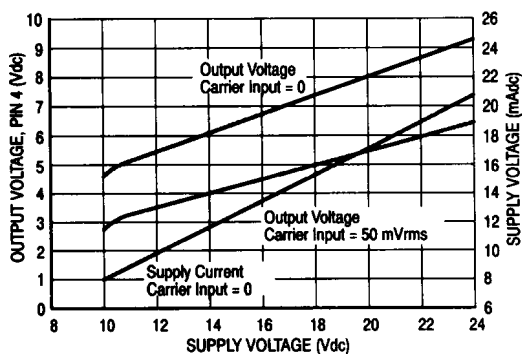


Figure 9. AFT Limiting

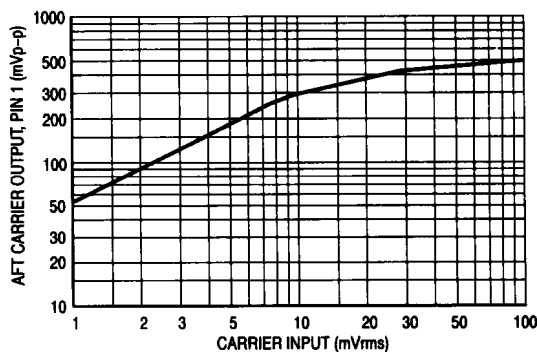


Figure 10. Video Output Response

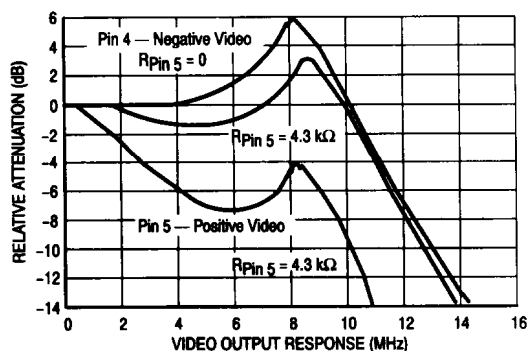
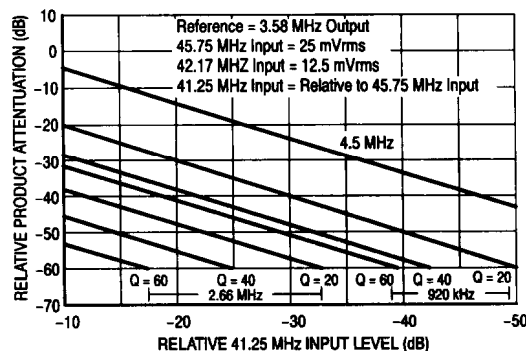


Figure 11. Video Output Products



## GENERAL INFORMATION

The MC1330A offers the designer a new approach to an old problem. Now linear detection can be performed at much lower power signal levels than possible with a detector diode.

Offering a number of distinct advantages, its easy implementation should meet with ready acceptance for television designs. Some specific features and information on systems design with this device are given below:

1. The device provides excellent linearity of output versus input, as shown in Figures 6 and 7. These graphs also show that video peak-to-peak amplitude (AC) does not change with supply voltage variation. (Slopes are parallel. Visualize a given variation of input CW and use the figure as a transfer function.)

2. The DC output level does change linearly with supply voltage shown in Figure 8. This can be accommodated by regulating the supply or by referencing the subsequent video amplifier to the same power supply.

3. The choice of Q for the tuned circuit of Pin 2 and 3 is not critical. The higher the Q, the better the rejection of 920 kHz products by the more critical the tuning accuracy required (see

Figure 11). Values of Q from 20 to 50 are recommended. (Note the internal resistance.)

4. A video output with positive-going sync is available at Pin 5 if required. This signal has a higher output impedance than Pin 4 so it must be handled with greater care. If not used, Pin 5 may be connected directly to the supply voltage (Pin 6). The video response will be altered somewhat (see Figure 10).

5. An AFT output (Pin 1) provides 460 mV of IF carrier output, sufficient voltage to drive an AFT ratio detector, with only one additional stage.

6. AGC lockout can occur if the input signal presented in the MC1330A is greater than that shown in the input overload section of the design characteristics shown on Page 3. If these values are exceeded, the turns ratio between the primary and secondary of  $T_1$  should be increased. Another solution to the problem is to use an input clamp diode  $D_1$  shown in Figure 14.

7. The total I.F. noise figure at high gain reductions can be improved by reflecting  $\approx 1.0$  k source impedance to the input of the MC1330A. This will cause some loss in overall IF voltage gain.

## TV-IF AMPLIFIER INFORMATION

A very compact high performance IF amplifier constructed as shown in Figure 14 minimizes the number of overall components and alignment adjustments. It can be readily combined with normal tuners and input tuning-trapping circuitry to provide the performance demanded of high quality receivers. This configuration will provide approximately 93 dB voltage gain and can accommodate the usual low impedance input network or, if desired, can take advantage of an impedance step-up from tuner to MC1350 input.

The burden of selectivity, formerly found between the third IF and detector, must now be placed at the interstage. The nominal 3.0 V peak-to-peak output can be varied from 0 V to 7.0 V with excellent linearity and freedom from spurious output products.

Alignment is most easily accomplished with an AM generator, set at a carrier frequency of 45.75 MHz, modulated with a video frequency sweep. This provides the proper realistic

conditions necessary to operate to low-level detector (LLD). The detector tank is first adjusted for maximum detected DC (with a CW input). Next, the video sweep modulation is applied and the interstage and input circuits aligned, step by step, as in a standard IF amplifier.

Note: A normal IF sweep generator, essentially an FM generator, will not serve properly without modification. The LLD tank attempts to "follow" the sweep input frequency, and results in variations of switching amplitude in the detector. Hence, the apparent overall response becomes modified by the response of the LLD tank, which a real signal doesn't do.

This effect can be prevented by resistively adding a 45.75 MHz CW signal to the output of the sweep generator approximately 3.0 dB greater than the sweep amplitude. See Figures 12 and 13 below. For a more detailed description of the MC1330A see application note AN545A.

Figure 12. Band Pass Displayed by Conventional Sweep

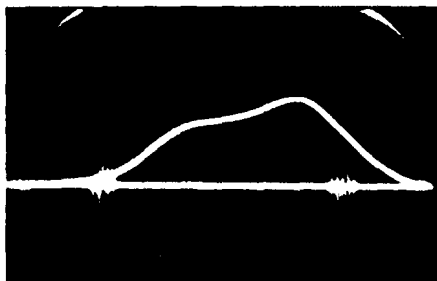
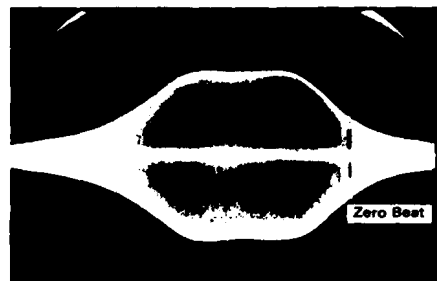
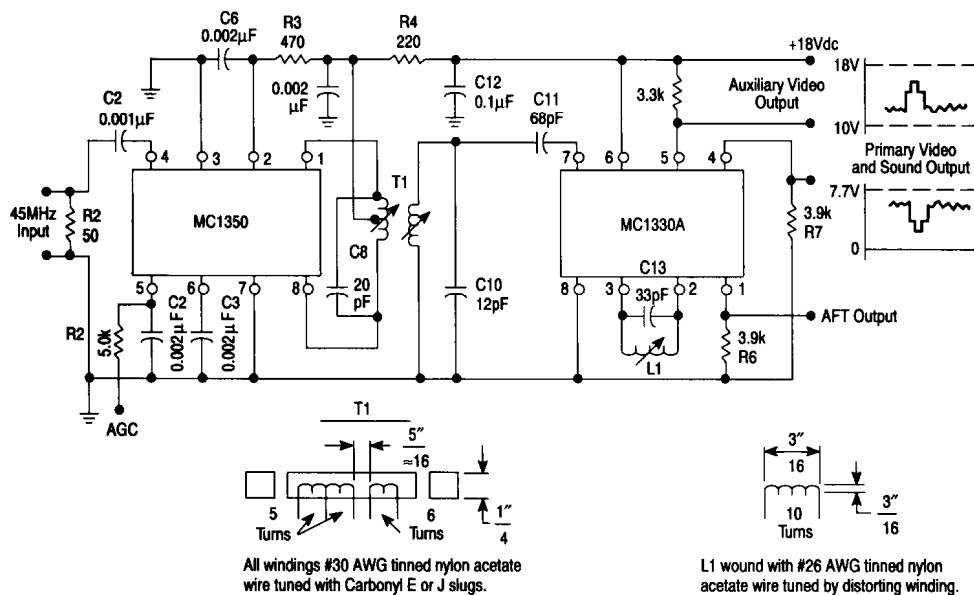


Figure 13. Band Pass Display with the Addition of Carrier Injection

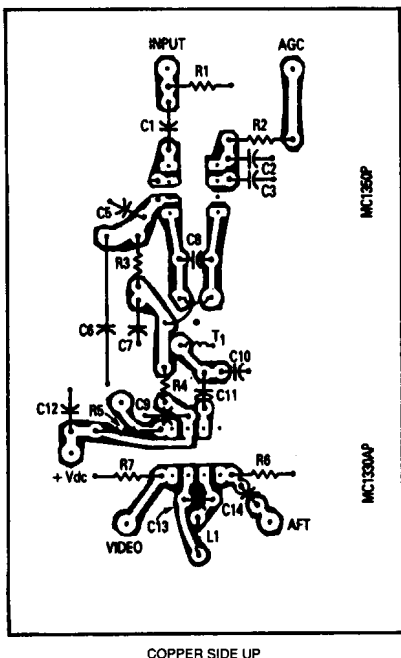


## MC1330A

**Figure 14. Typical Application of MC1350P Video IF Amplifier and MC1330A Low-Level Video Detector Circuit**



**Figure 15. Printed Circuit Board (Parts Layout)**



**Figure 16. Printed Circuit (Board Layout)**

