# **BLP7G07S-140P**

# Power LDMOS transistor Rev. 5 — 8 January 2016

**AMMPLEON** 

Product data sheet

#### **Product profile** 1.

### 1.1 General description

140 W LDMOS power transistor for base station applications at frequencies from 700 MHz to 1000 MHz.

Table 1. Typical performance

| Test signal      | f          | V <sub>DS</sub> | P <sub>L(AV)</sub> | Gp   | $\eta_D$ | ACPR <sub>5M</sub> |
|------------------|------------|-----------------|--------------------|------|----------|--------------------|
|                  | (MHz)      | (V)             | (W)                | (dB) | (%)      | (dBc)              |
| 2-carrier W-CDMA | 724 to 769 | 28              | 35                 | 20.9 | 29.6     | -36.3 [ <u>1</u> ] |
|                  | 790 to 821 | 28              | 35                 | 20.2 | 29.0     | -35.5 [1]          |

<sup>[1]</sup> Test signal: 3GPP test model 1; 64 DPCH; PAR = 7.5 dB at 0.01 % probability on CCDF per carrier; carrier spacing 5 MHz.

#### 1.2 Features and benefits

- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (700 MHz to 1000 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

## 1.3 Applications

RF power amplifiers for W-CDMA base stations and multi carrier applications in the 700 MHz to 1000 MHz frequency range.

# 2. Pinning information

Table 2. Pinning

| Pin | Description | Simplified outline | Graphic symbol  |
|-----|-------------|--------------------|-----------------|
| 1   | gate 1      | 4 0                | ,               |
| 2   | gate 2      | 4 3                | 4               |
| 3   | drain 2     |                    | 1 1             |
| 4   | drain 1     | pin 1 index        | 5               |
| 5   | source [1]  | ₹ <b> </b>         | 3<br>aaa-003574 |

[1] Connected to flange.

# 3. Ordering information

Table 3. Ordering information

| Type number   | Package | ckage   |           |  |  |  |  |
|---------------|---------|---|-----------|--|--|--|--|
|               | Name    | Description   | Version   |  |  |  |  |
| BLP7G07S-140P | HSOP4F  | plastic, heatsink small outline package; 4 leads (flat) | SOT1223-2 |  |  |  |  |

# 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol           | Parameter            | Conditions | Min  | Max  | Unit |
|------------------|----------------------|------------|------|------|------|
| $V_{DS}$         | drain-source voltage |            | -    | 65   | V    |
| $V_{GS}$         | gate-source voltage  |            | -0.5 | +13  | V    |
| T <sub>stg</sub> | storage temperature  |            | -65  | +150 | °C   |
| Tj               | junction temperature | [1]        | -    | 225  | °C   |

<sup>[1]</sup> Continuous use at maximum temperature will affect the reliability.

## 5. Thermal characteristics

Table 5. Thermal characteristics

| Symbol                  | Parameter                                | Conditions  | Тур   | Unit |
|-------------------------|--|---|-------|------|
| R <sub>th(j-case)</sub> | thermal resistance from junction to case | $T_{case}$ = 80 °C; $P_L$ = 35 W; $V_{DS}$ = 28 V; $I_{Dg}$ = 1200 mA | 0.455 | K/W  |

## 6. Characteristics

#### Table 6. DC characteristics

 $T_i$  = 25 °C per section; unless otherwise specified.

| Symbol              | Parameter                        | Conditions   | Min | Тур  | Max | Unit |
|---------------------|----------------------------------|--|-----|------|-----|------|
| $V_{(BR)DSS}$       | drain-source breakdown voltage   | $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$                         | 65  | -    | -   | V    |
| $V_{GS(th)}$        | gate-source threshold voltage    | $V_{DS}$ = 10 V; $I_{D}$ = 100 mA                                  | 1.5 | 1.9  | 2.3 | V    |
| $V_{GSq}$           | gate-source quiescent voltage    | $V_{DS}$ = 28 V; $I_{D}$ = 600 mA                                  | 1.7 | 2.1  | 2.5 | V    |
| $I_{DSS}$           | drain leakage current            | $V_{GS} = 0 \text{ V}; V_{DS} = 28 \text{ V}$                      | -   | -    | 1.4 | μΑ   |
| I <sub>DSX</sub>    | drain cut-off current            | $V_{GS} = V_{GS(th)} + 3.75 \text{ V};$<br>$V_{DS} = 10 \text{ V}$ | -   | 18   | -   | Α    |
| I <sub>GSS</sub>    | gate leakage current             | V <sub>GS</sub> = 11 V; V <sub>DS</sub> = 0 V                      | -   | -    | 140 | nA   |
| 9 <sub>fs</sub>     | forward transconductance         | $V_{DS}$ = 10 V; $I_{D}$ = 3.5 A                                   | -   | 6.5  | -   | S    |
| R <sub>DS(on)</sub> | drain-source on-state resistance | $V_{GS} = V_{GS(th)} + 3.75 V;$<br>$I_D = 3.5 A$                   | -   | 0.19 | -   | Ω    |

#### Table 7. RF characteristics

Test signal: 2-carrier W-CDMA; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1-64 DPCH;  $f_1$  = 724 MHz;  $f_2$  = 729 MHz;  $f_3$  = 764 MHz;  $f_4$  = 769 MHz; RF performance at  $V_{DS}$  = 28 V;  $I_{Dq}$  = 1200 mA;  $T_{case}$  = 25 °C; unless otherwise specified; in a broadband class-AB production test circuit from 724 MHz to 821 MHz.

| Symbol             | Parameter                            | Conditions                | Min  | Тур   | Max   | Unit |
|--------------------|--------------------------------------|---------------------------|------|-------|-------|------|
| Gp                 | power gain                           | P <sub>L(AV)</sub> = 35 W | 19.8 | 20.9  | -     | dB   |
| RLin               | input return loss                    | P <sub>L(AV)</sub> = 35 W | -    | -14   | -7.5  | dB   |
| $\eta_{D}$         | drain efficiency                     | P <sub>L(AV)</sub> = 35 W | 26.9 | 29.6  | -     | %    |
| ACPR <sub>5M</sub> | adjacent channel power ratio (5 MHz) | P <sub>L(AV)</sub> = 35 W | -    | -36.3 | -32.4 | dBc  |

# 7. Test information

## 7.1 Ruggedness in class-AB operation

The BLP7G07S-140P is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS}$  = 28 V;  $I_{Dq}$  = 1200 mA;  $P_L$  = 140 W; f = 724 MHz to 821 MHz.

# 7.2 Test circuit information

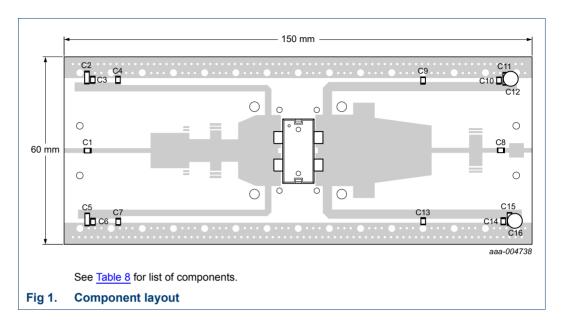


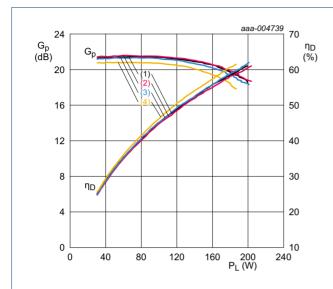
Table 8. List of components

See Figure 1 for component layout.

| Component               | Description                       | Value        | Remarks |
|-------------------------|-----------------------------------|--------------|---------|
| C1, C4, C7, C8, C9, C13 | multilayer ceramic chip capacitor | 82 pF        | ATC800  |
| C2, C5, C11, C15        | multilayer ceramic chip capacitor | 10 μF        | TDK     |
| C3, C6, C10, C14        | multilayer ceramic chip capacitor | 1 μF         | Murata  |
| C12, C16                | electrolytic capacitor            | 470 μF, 63 V |         |

# 7.3 Graphical data

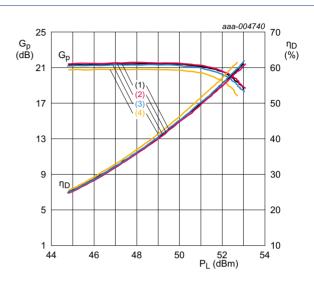
## 7.3.1 CW pulsed



 $V_{DS}$  = 28 V;  $I_{Dq}$  = 1200 mA;  $t_p$  = 10  $\mu$ s;  $\delta$  = 10 %.

- (1) f = 724 MHz
- (2) f = 769 MHz
- (3) f = 790 MHz
- (4) f = 821 MHz

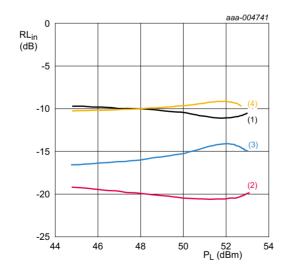
Fig 2. Power gain and drain efficiency as function of load power; typical values



 $V_{DS}$  = 28 V;  $I_{Dq}$  = 1200 mA;  $t_p$  = 10  $\mu s; \, \delta$  = 10 %.

- (1) f = 724 MHz
- (2) f = 769 MHz
- (3) f = 790 MHz
- (4) f = 821 MHz

Fig 3. Power gain and drain efficiency as function of load power; typical values

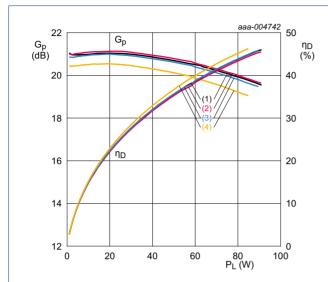


 $V_{DS}$  = 28 V;  $I_{Dq}$  = 1200 mA;  $t_p$  = 10  $\mu$ s;  $\delta$  = 10 %.

- (1) f = 724 MHz
- (2) f = 769 MHz
- (3) f = 790 MHz
- (4) f = 821 MHz

Fig 4. Input return loss as a function of load power; typical values

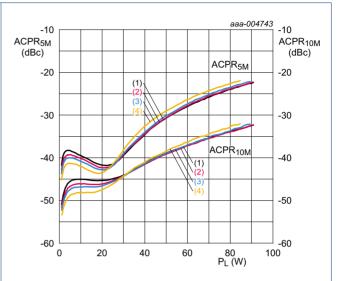
#### 7.3.2 2-Carrier W-CDMA



 $V_{DS} = 28 \text{ V}; I_{Dq} = 1200 \text{ mA}.$ 

- (1) f = 726.5 MHz
- (2) f = 766.5 MHz
- (3) f = 793.5 MHz
- (4) f = 818.5 MHz

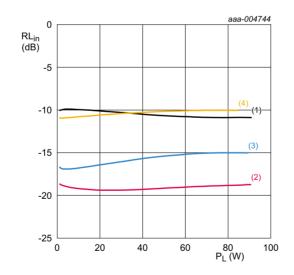
Fig 5. Power gain and drain efficiency as function of load power; typical values



 $V_{DS} = 28 \text{ V}; I_{Dq} = 1200 \text{ mA}.$ 

- (1) f = 726.5 MHz
- (2) f = 766.5 MHz
- (3) f = 793.5 MHz
- (4) f = 818.5 MHz

Fig 6. Adjacent channel power ratio (5 MHz) and adjacent channel power ratio (10 MHz) as function of load power; typical values



 $V_{DS}$  = 28 V;  $I_{Dq}$  = 1200 mA.

- (1) f = 726.5 MHz
- (2) f = 766.5 MHz
- (3) f = 793.5 MHz
- (4) f = 818.5 MHz

Fig 7. Input return loss as a function of load power; typical values

# 8. Package outline

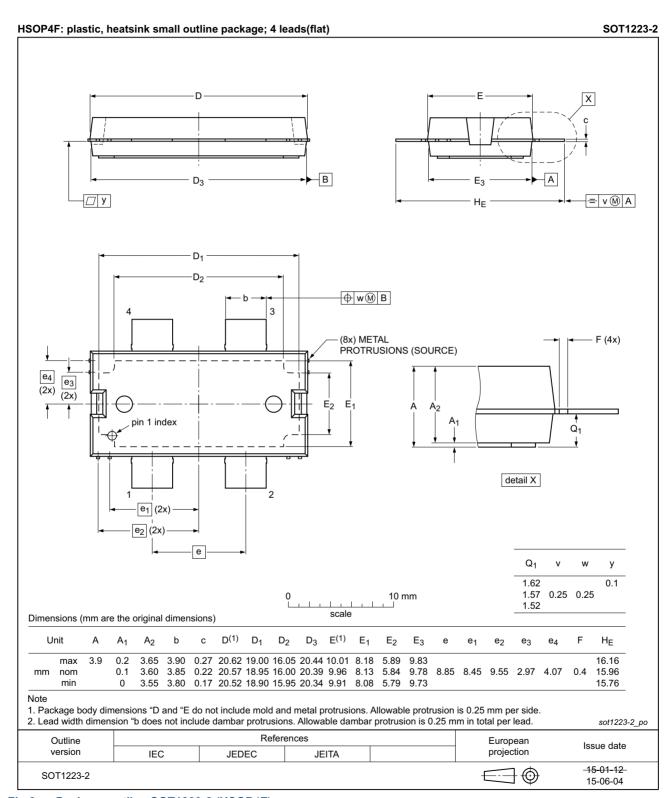


Fig 8. Package outline SOT1223-2 (HSOP4F)

# 9. Handling information

#### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

# 10. Abbreviations

Table 9. Abbreviations

| Acronym | Description                                    |
|---------|--|
| 3GPP    | 3rd Generation Partnership Project             |
| CCDF    | Complementary Cumulative Distribution Function |
| CW      | Continuous Wave                                |
| DPCH    | Dedicated Physical CHannel                     |
| ESD     | ElectroStatic Discharge                        |
| LDMOS   | Laterally Diffused Metal Oxide Semiconductor   |
| PAR     | Peak-to-Average Ratio                          |
| VSWR    | Voltage Standing-Wave Ratio                    |
| W-CDMA  | Wideband Code Division Multiple Access         |

# 11. Revision history

Table 10. Revision history

| Document ID       | Release date  | Data sheet status    | Change notice | Supersedes        |  |  |
|-------------------|---|----------------------|---------------|-------------------|--|--|
| BLP7G07S-140P v.5 | 20160108  | Product data sheet   | -             | BLP7G07S-140P v.4 |  |  |
| Modifications:    | <u>Table 3 on page 2</u> : table updated                                  |                      |               |                   |  |  |
|                   | • Figure 8 on page 7: package outline changed from SOT1223-1 to SOT1223-2 |                      |               |                   |  |  |
| BLP7G07S-140P v.4 | 20150901  | Product data sheet   | -             | BLP7G07S-140P v.3 |  |  |
| BLP7G07S-140P v.3 | 20130329  | Product data sheet   | -             | BLP7G07S-140P v.2 |  |  |
| BLP7G07S-140P v.2 | 20121009  | Objective data sheet | -             | BLP7G07S-140P v.1 |  |  |
| BLP7G07S-140P v.1 | 20120621  | Objective data sheet | -             | -                 |  |  |

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|--------------------------------|-------------------|---|
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- [2] The term 'short data sheet' is explained in section "Definitions"
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# **BLP7G07S-140P**

#### **Power LDMOS transistor**

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