CY7C1069BV33

16-Mbit (2M x 8) Static RAM

Features

- **High speed**
  - **— t_{AA} = 10 ns**
- **Low active power**
  - **— 990 mW (max.)**
- **Operating voltages of 3.3 ± 0.3V**
- **2.0V data retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Available in Pb-free and non Pb-free 54-pin TSOP II package**

Functional Description

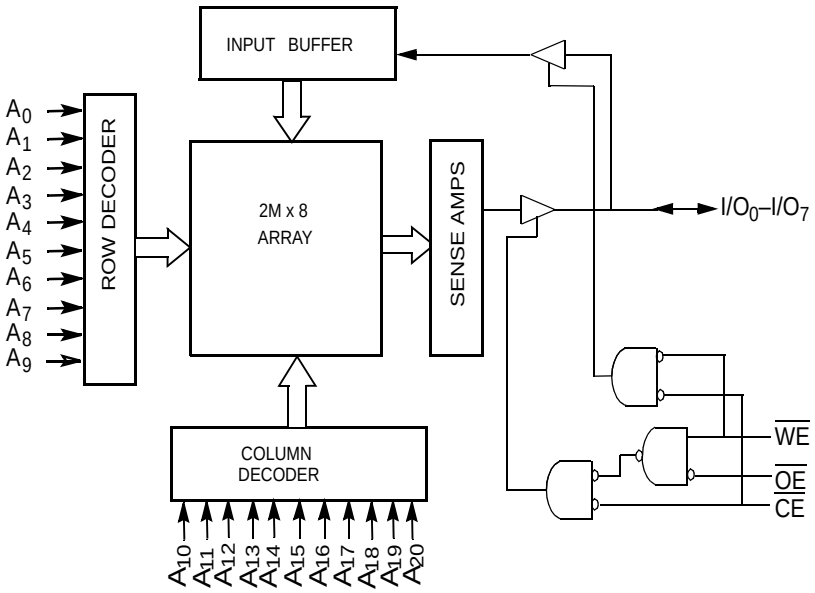
The CY7C1069BV33 is a high-performance CMOS Static RAM organized as 2,097,152 words by 8 bits. Writing to the device is accomplished by enabling the chip (by taking CE LOW) and Write Enable (WE) inputs LOW.

Reading from the device is accomplished by enabling the chip (CE LOW) as well as forcing the Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. See the truth table at the back of this data sheet for a complete description of Read and Write modes.

The input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected (CE HIGH), the outputs are disabled (OE HIGH), or during a Write operation (CE LOW and WE LOW).

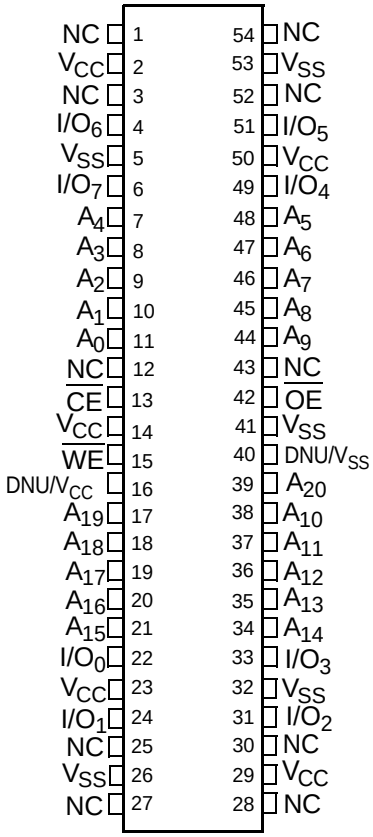
The CY7C1069BV33 is available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout.

Logic Block Diagram



Pin Configurations[1, 2]

54-pin TSOP II (Top View)



Notes:
1. DNU/V_{CC} Pin (#16) has to be left floating or connected to V_{CC} and DNU/V_{SS} Pin (#40) has to be left floating or connected to V_{SS} to ensure proper application.
2. NC - No Connect Pins are not connected to the die.

Selection Guide

		–10	–12	Unit
Maximum Access Time		10	12	ns
Maximum Operating Current	Commercial	275	260	mA
	Industrial	275	260	
Maximum CMOS Standby Current	Commercial/Industrial	50	50	mA

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[3] .... –0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State[3] .....–0.5V to V_{CC} + 0.5V

DC Input Voltage[3] .....–0.5V to V_{CC} + 0.5V

Current into Outputs (LOW)..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		–10 Min.	–10 Max.	–12 Min.	–12 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[3]			–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–1	+1	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., f = f_{MAX} = $1/t_{RC}$	Comm'l		275		260	mA
			Ind'l		275		260	mA
I_{SB1}	Automatic CE Power-down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			70		70	mA
I_{SB2}	Automatic CE Power-down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0	Comm'l/ Ind'l		50		50	mA

Capacitance[4]

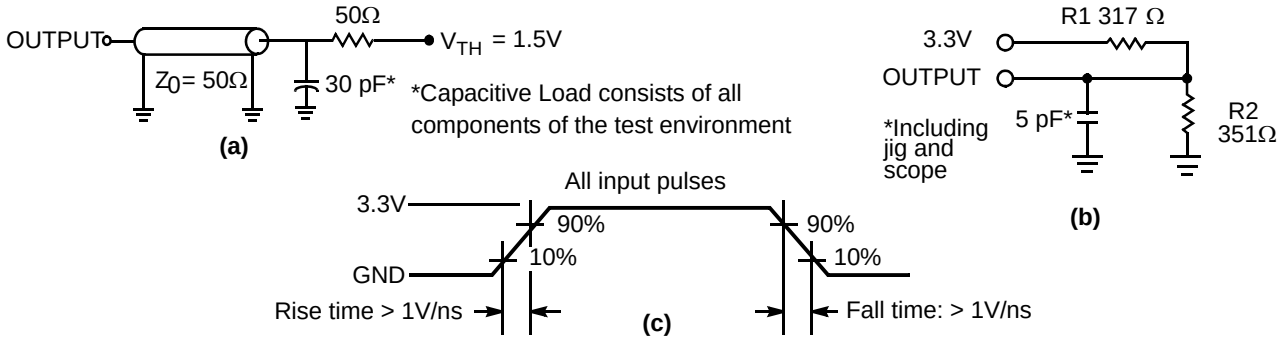
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	6	pF
C_{OUT}	I/O Capacitance		8	pF

Thermal Resistance[4]

Parameter	Description	Test Conditions	TSOP-II	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	49.95	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		3.34	°C/W

Notes:
3. V_{IL} (min.) = –2.0V and V_{IH}(max) = V_{CC} + 0.5V for pulse durations of less than 20 ns.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[5]



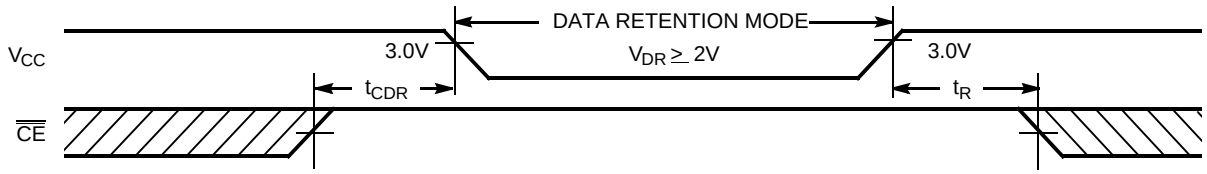
AC Switching Characteristics Over the Operating Range [6]

Parameter	Description	–10		–12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{power}	V_{CC}(typical) to the First Access[7]	1		1		ms
t_{RC}	Read Cycle Time	10		12		ns
t_{AA}	Address to Data Valid		10		12	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[8]	1		1		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[8]		5		6	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[8]	3		3		ns
t_{HZCE}	$\overline{CE}$ to High-Z[8]		5		6	ns
t_{PU}	$\overline{CE}$ to Power-up[9]	0		0		ns
t_{PD}	$\overline{CE}$ to Power-down[9]		10		12	ns
Write Cycle[10, 11]						
t_{WC}	Write Cycle Time	10		12		ns
t_{SCE}	$\overline{CE}$ to Write End	7		8		ns
t_{AW}	Address Set-up to Write End	7		8		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		ns
t_{SD}	Data Set-up to Write End	5.5		6		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[8]	3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[8]		5		6	ns

Notes:

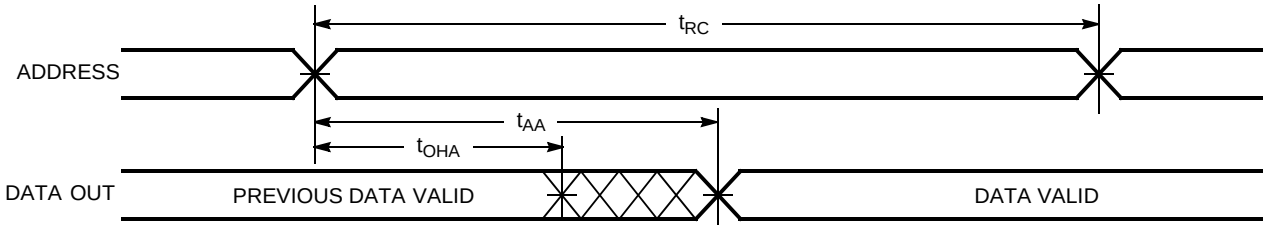
5. Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0V). As soon as 1ms (T_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation can begin including reduction in V_{DD} to the data retention (V_{CCDR}, 2.0V) voltage.
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and transmission line loads. Test conditions for the Read cycle use output loading shown in part a) of the AC test loads, unless specified otherwise.
7. t_{POWER} gives the minimum amount of time that the power supply should be at typical VCC values until the first memory access can be performed.
8. t_{HZOE}, t_{HZSCE}, t_{HZWE} and t_{LZOE}, t_{LZCE}, and t_{LZWE} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
9. These parameters are guaranteed by design and are not tested.
10. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a Write, and the transition of any of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
11. The minimum Write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Waveform

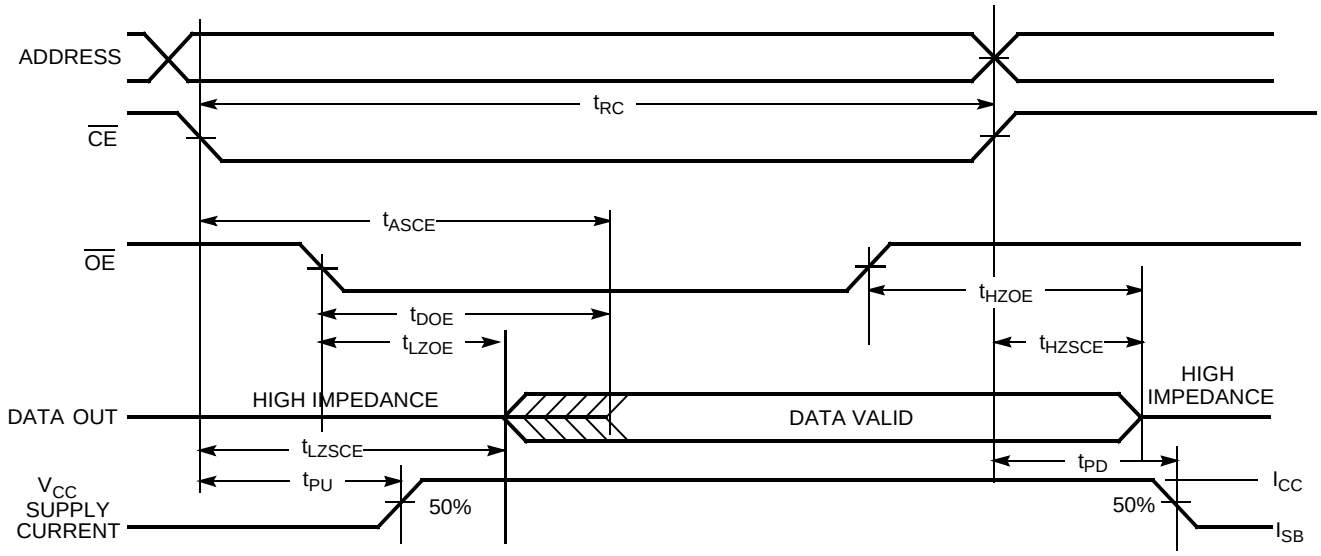


Switching Waveforms

Read Cycle No. 1[12, 13]



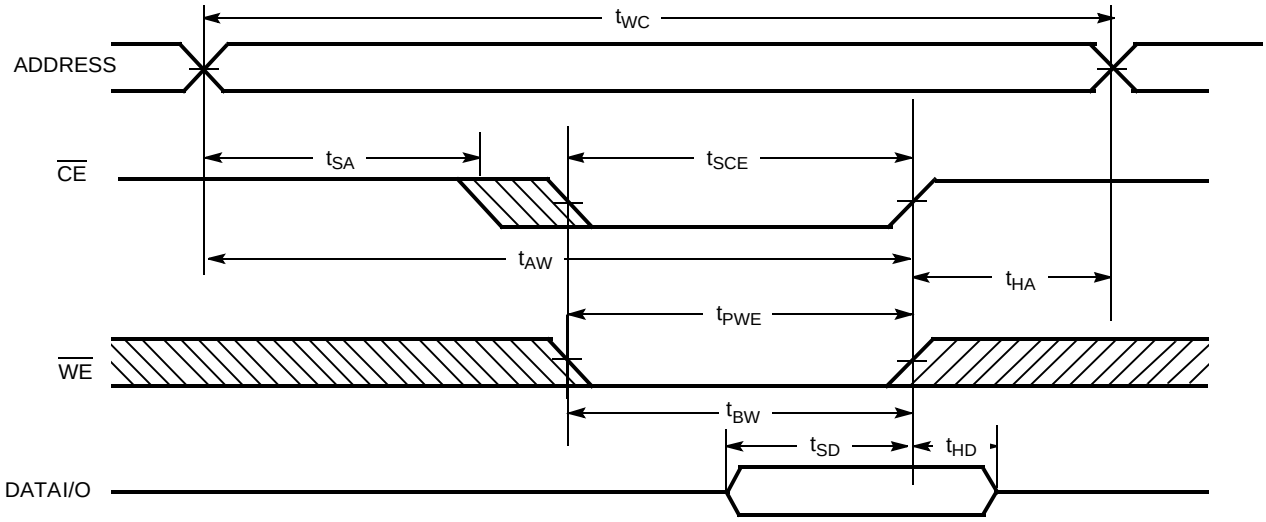
Read Cycle No. 2 ($\overline{OE}$ Controlled)[13, 14]



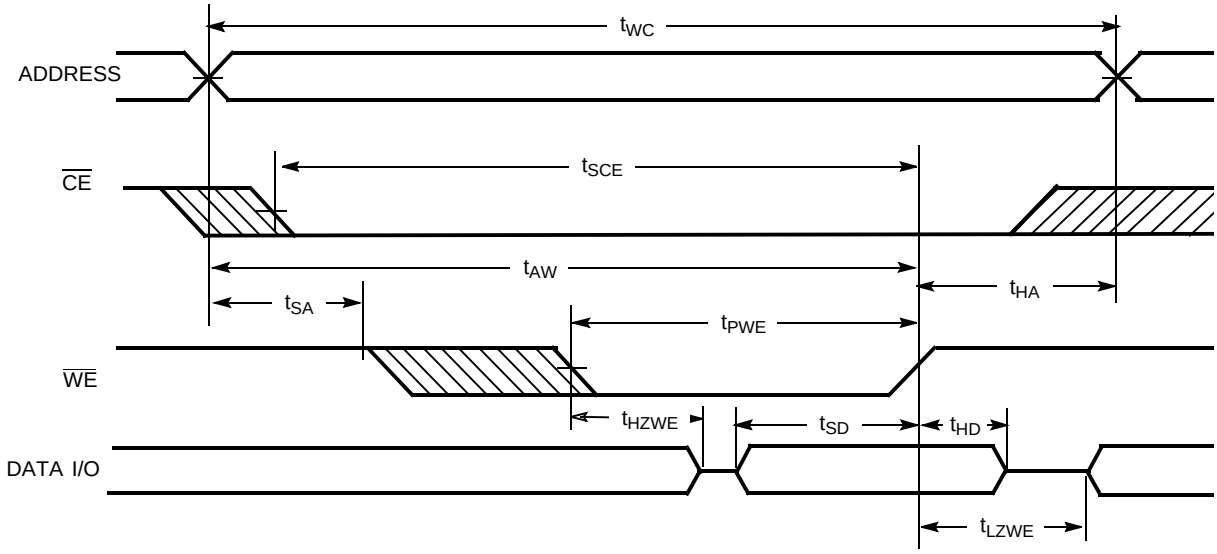
Notes:
12. Device is continuously selected. $\overline{CE} = V_{IL}$.
13. $\overline{WE}$ is HIGH for Read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[15, 16]



Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[15, 16]



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	High-Z	Power-down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High-Z	Selected, Outputs Disabled	Active (I_{CC})

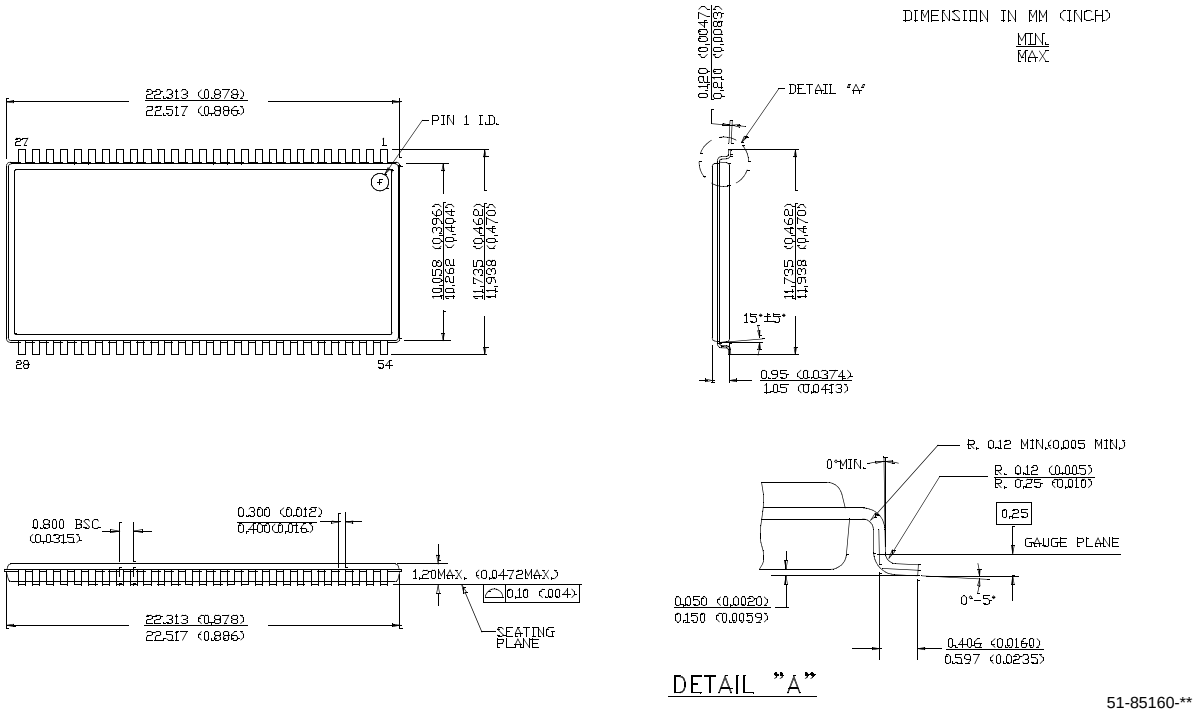
Notes:
15. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1069BV33-10ZC	51-85160	54-pin TSOP II	Commercial
	CY7C1069BV33-10ZXC		54-pin TSOP II (Pb-free)	
	CY7C1069BV33-10ZI		54-pin TSOP II	Industrial
	CY7C1069BV33-10ZXI		54-pin TSOP II (Pb-free)	
12	CY7C1069BV33-12ZC		54-pin TSOP II	Commercial
	CY7C1069BV33-12ZXC		54-pin TSOP II (Pb-free)	
	CY7C1069BV33-12ZI		54-pin TSOP II	Industrial
	CY7C1069BV33-12ZXI		54-pin TSOP II (Pb-free)	

Package Diagram

54-pin TSOP II (51-85160)



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Document History Page

Document Title: CY7C1069BV33 16-Mbit (2M x 8) Static RAM Document Number: 38-05694				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	283950	See ECN	RKF	New data sheet
*A	314014	See ECN	RKF	Final data sheet
*B	492137	See ECN	NXR	Removed 8 ns speed bin Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Updated the Ordering Information Table