



BUK9604-40A

N-channel TrenchMOS logic level FET

Rev. 2 — 7 February 2011

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	40	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 ; see Figure 3	-	-	75	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	300	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.3\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$	-	3.7	5.9	mΩ
		$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$	-	2.9	4	mΩ
		$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 11 ; see Figure 12	-	3.5	4.4	mΩ



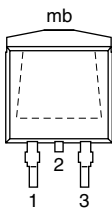
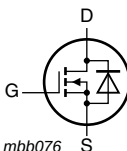
Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\ \Omega$; $V_{GS} = 5\text{ V}$; $T_{J(\text{init})} = 25\text{ }^\circ\text{C}$; unclamped	-	-	1.6	J
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; $V_{DS} = 32\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$; see Figure 13	-	56	-	nC

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain ^[1]		
3	S	source		
mb	D	mounting base; connected to drain		

SOT404 (D2PAK)

[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK9604-40A	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	40	V	
V _{DGR}	drain-gate voltage	R _{GS} = 20 kΩ	-	40	V	
V _{GS}	gate-source voltage		-15	15	V	
I _D	drain current	T _{mb} = 100 °C; V _{GS} = 5 V; see Figure 1	[1]	-	75	A
		T _{mb} = 25 °C; V _{GS} = 5 V; see Figure 1 ;	[1]	-	75	A
		see Figure 3	[2]	-	198	A
I _{DM}	peak drain current	T _{mb} = 25 °C; pulsed; t _p ≤ 10 μs; see Figure 3	-	794	A	
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	300	W	
T _{stg}	storage temperature		-55	175	°C	
T _j	junction temperature		-55	175	°C	
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	[3]	-	198	A
			[1]	-	75	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	794	A	
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 75 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{i(initial)} = 25 °C; unclamped	-	1.6	J	

[1] Continuous current is limited by package.

[2] Current is limited by power dissipation chip rating.

[3] Current is limited by power dissipation chip rating

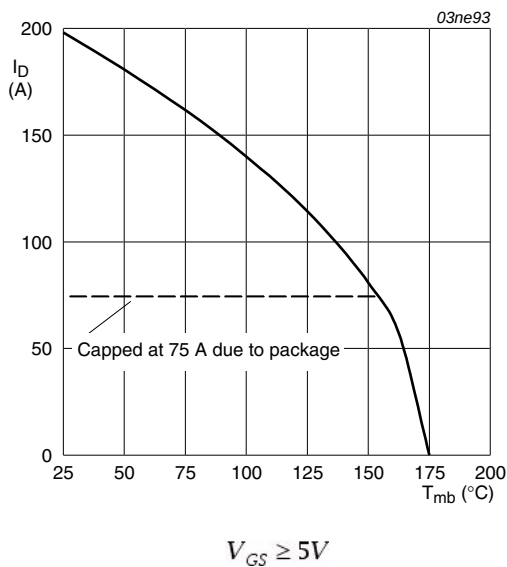


Fig 1. Normalized continuous drain current as a function of mounting base temperature

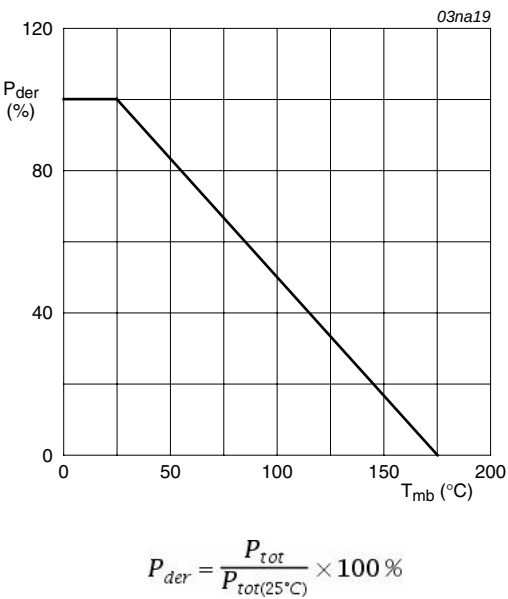


Fig 2. Normalized total power dissipation as a function of mounting base temperature

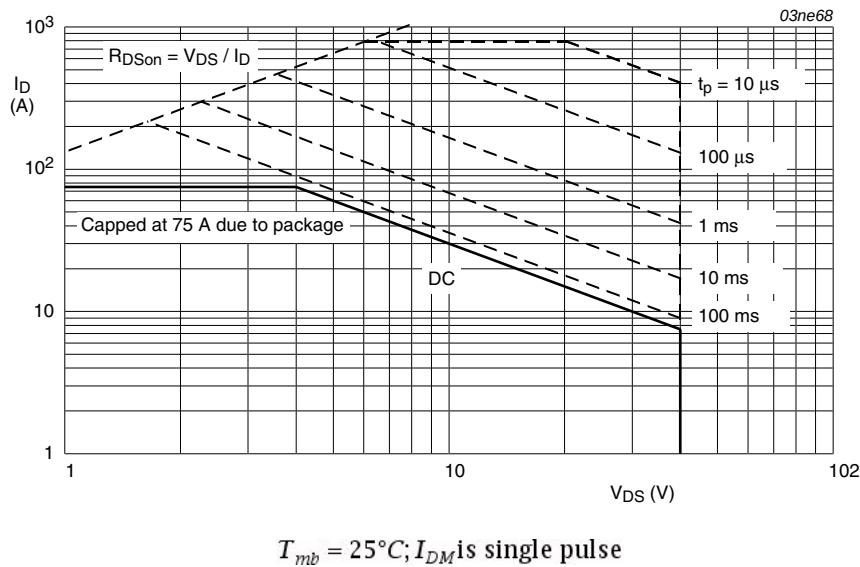


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on printed circuit board; minimum footprint	-	50	-	K/W

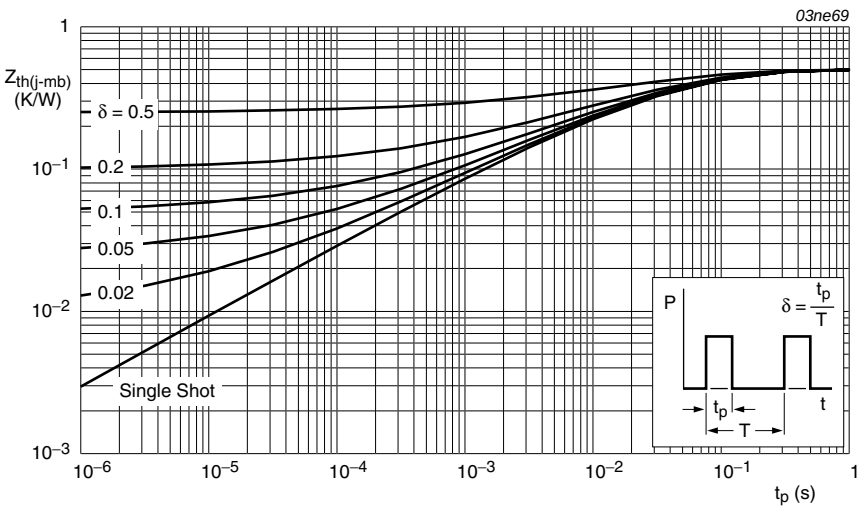


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V; T _j = 25 °C	40	-	-	V
		I _D = 0.25 mA; V _{GS} = 0 V; T _j = -55 °C	36	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; see Figure 10	1	1.5	2	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; see Figure 10	0.5	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; see Figure 10	-	-	2.3	V
I _{DSS}	drain leakage current	V _{DS} = 40 V; V _{GS} = 0 V; T _j = 25 °C	-	0.05	10	μA
		V _{DS} = 40 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.3 V; I _D = 25 A; T _j = 25 °C	-	3.7	5.9	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C	-	2.9	4	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 175 °C; see Figure 11 ; see Figure 12	-	-	8.3	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; see Figure 11 ; see Figure 12	-	3.5	4.4	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 32 V; V _{GS} = 5 V; T _j = 25 °C; see Figure 13	-	128	-	nC
Q _{GS}	gate-source charge		-	13	-	nC
Q _{GD}	gate-drain charge		-	56	-	nC
C _{iss}	input capacitance		V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; see Figure 14	-	6200	8260
C _{oss}	output capacitance	-		1040	1250	pF
C _{rss}	reverse transfer capacitance	-		680	940	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.2 Ω; V _{GS} = 5 V; R _{G(ext)} = 10 Ω; T _j = 25 °C	-	62	-	ns
t _r	rise time		-	309	-	ns
t _{d(off)}	turn-off delay time		-	365	-	ns
t _f	fall time		-	306	-	ns
L _D	internal drain inductance	from upper edge of drain mounting base to centre of die; T _j = 25 °C	-	2.5	-	nH
		from drain lead 6 mm from package to centre of die; T _j = 25 °C	-	4.5	-	nH
L _S	internal source inductance	from source lead to source bond pad; T _j = 25 °C	-	7.5	-	nH

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 40\text{ A}$; $V_{GS} = 0\text{ V}$; $T_J = 25\text{ }^{\circ}\text{C}$; see Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$;	-	260	-	ns
Q_r	recovered charge	$V_{GS} = -10\text{ V}$; $V_{DS} = 30\text{ V}$; $T_J = 25\text{ }^{\circ}\text{C}$	-	531	-	nC

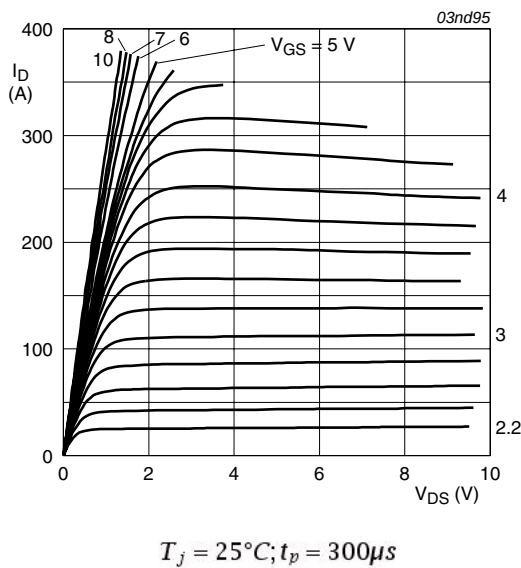


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

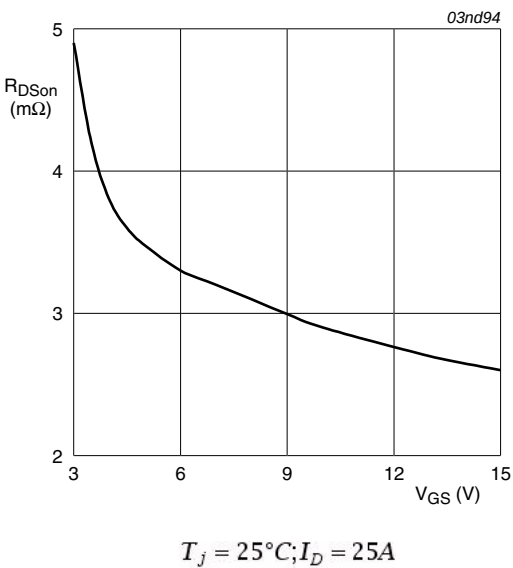


Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

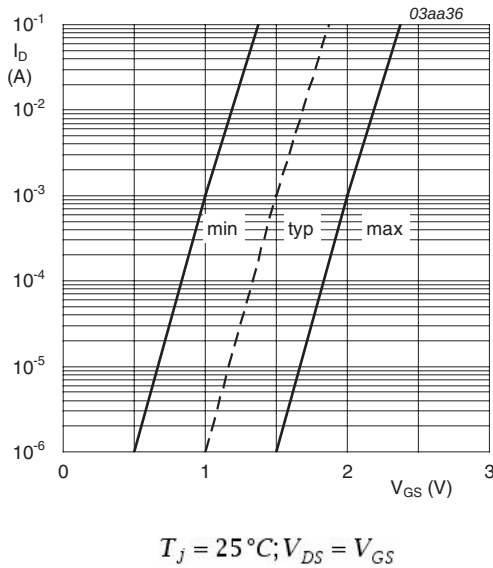


Fig 7. Sub-threshold drain current as a function of gate-source voltage

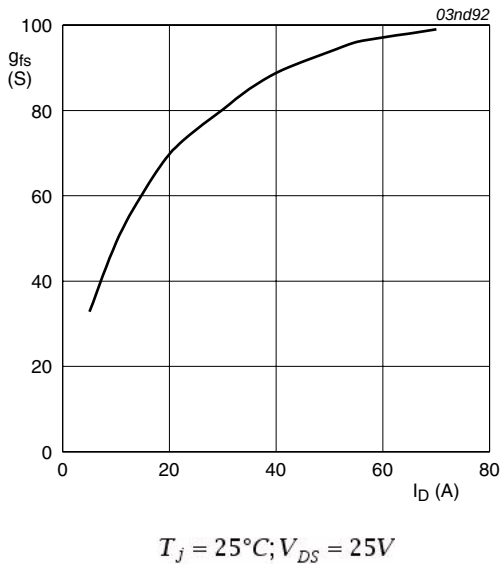


Fig 8. Forward transconductance as a function of drain current; typical values

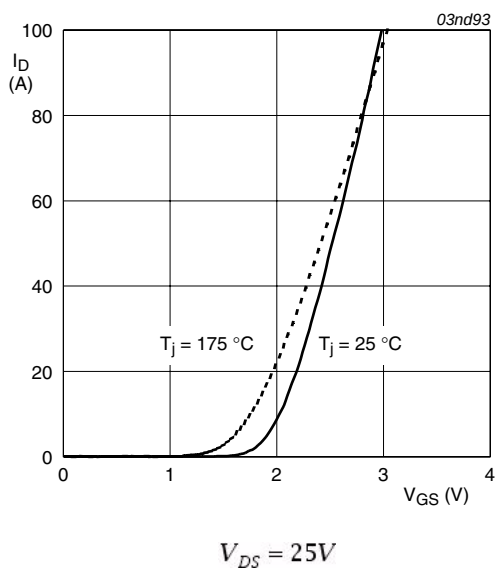


Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

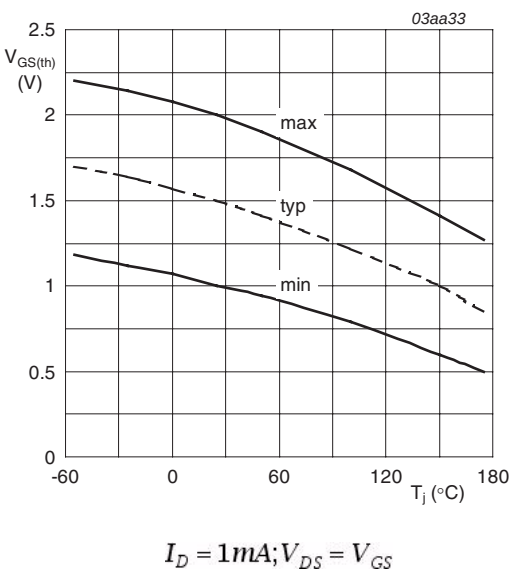


Fig 10. Gate-source threshold voltage as a function of junction temperature

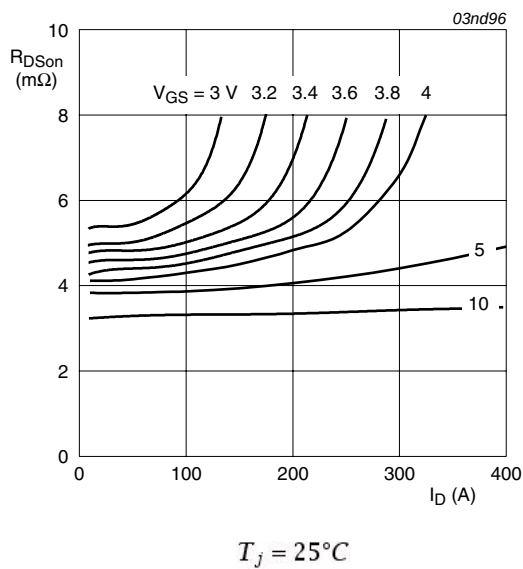


Fig 11. Drain-source on-state resistance as a function of drain current; typical values

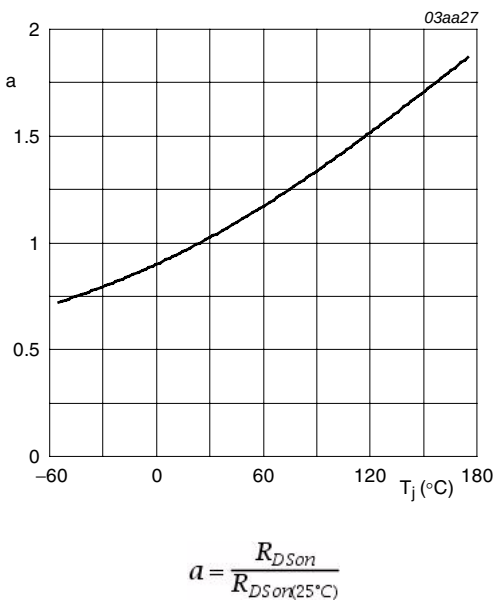


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

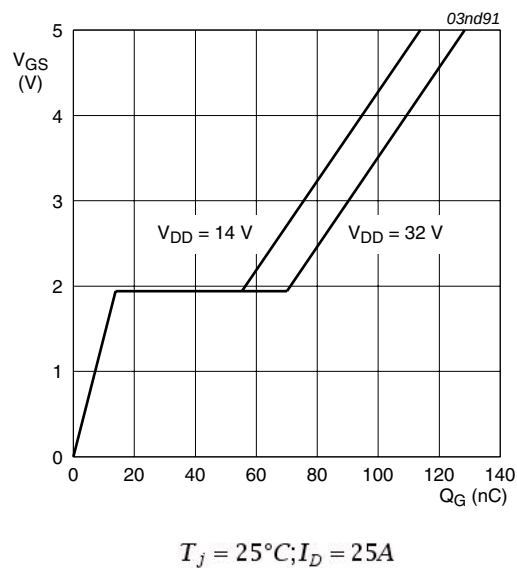


Fig 13. Gate-source voltage as a function of turn-on gate charge; typical values

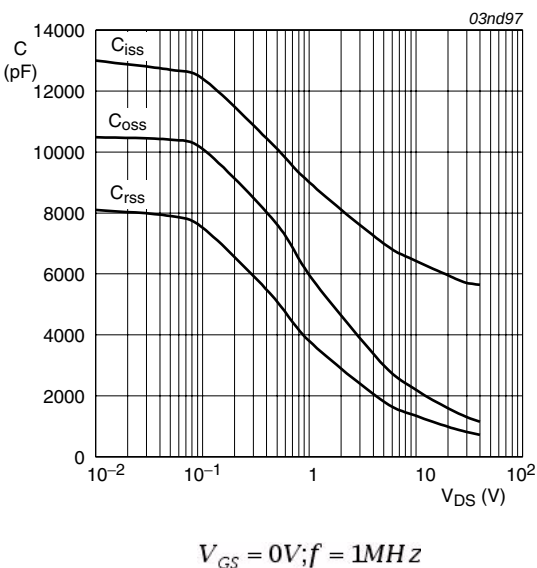


Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

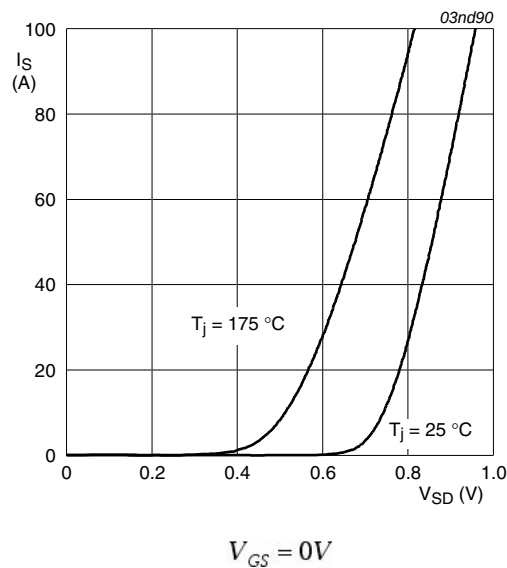
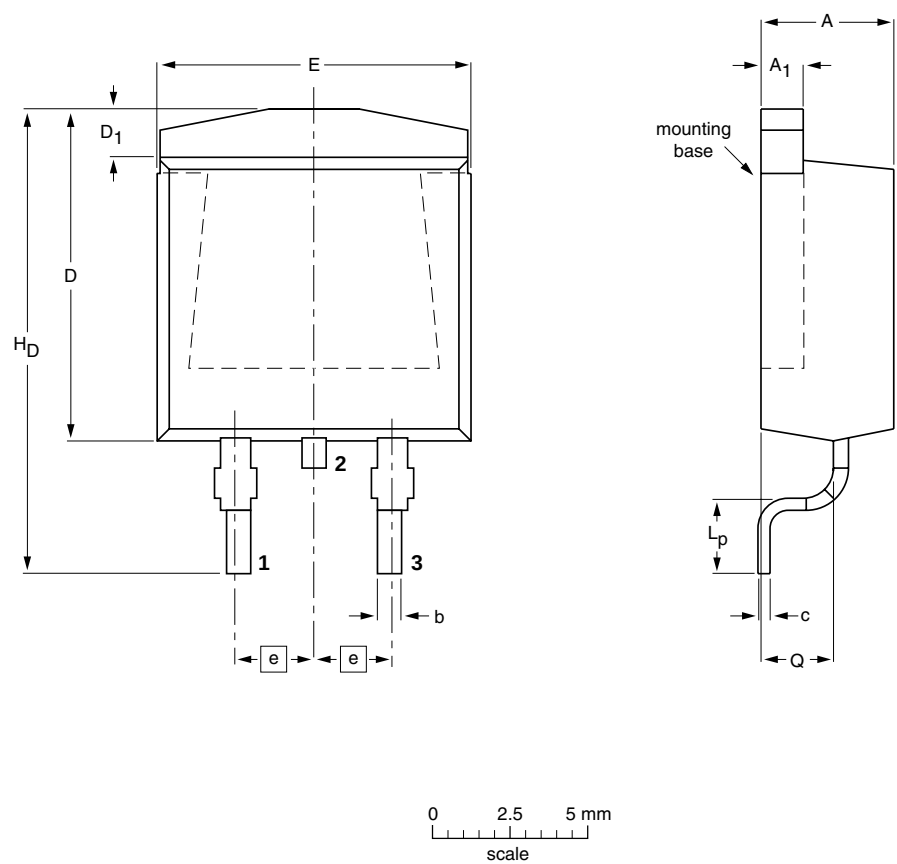


Fig 15. Reverse diode current as a function of reverse diode voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D _{max.}	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						05-02-11 06-03-16

Fig 16. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9504-40A v.2	20110207	Product data sheet	-	BUK95_96_9E04_40A-01
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type number BUK9504-40A separated from data sheet BUK95_96_9E04_40A-01.			
BUK95_96_9E04_40A-01	20011024	Product specification	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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