

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ max}$	$I_D \text{ max}$ $T_A = 25^\circ\text{C}$
-30V	20m Ω @ $V_{GS} = -10\text{V}$	-9.5 A
	29m Ω @ $V_{GS} = -5\text{V}$	-8.5 A

Description and Applications

This MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

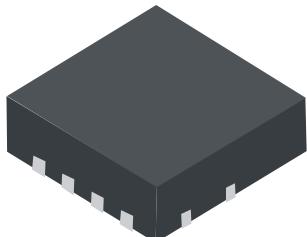
- Backlighting
- Power Management Functions
- DC-DC Converters

Features and Benefits

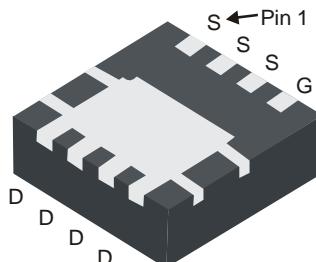
- Low $R_{DS(ON)}$ – ensures on state losses are minimized
- Small form factor thermally efficient package enables higher density end products
- Occupies just 33% of the board area occupied by SO-8 enabling smaller end product
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

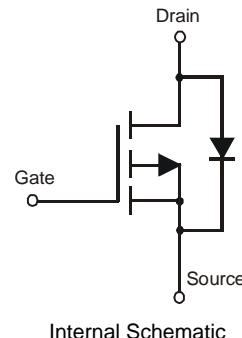
- Case: POWERDI3333-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See diagram
- Terminals: Finish – Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208 
- Weight: 0.072 grams (approximate)



Top View



Bottom View



Internal Schematic

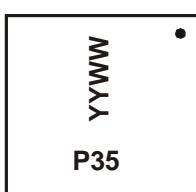
Ordering Information (Note 4)

Part Number	Case	Packaging
DMP3035SFG-7	POWERDI3333-8	2000/Tape & Reel
DMP3035SFG-13	POWERDI3333-8	3000/Tape & Reel

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See <http://www.diodes.com> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at <http://www.diodes.com>.

Marking Information



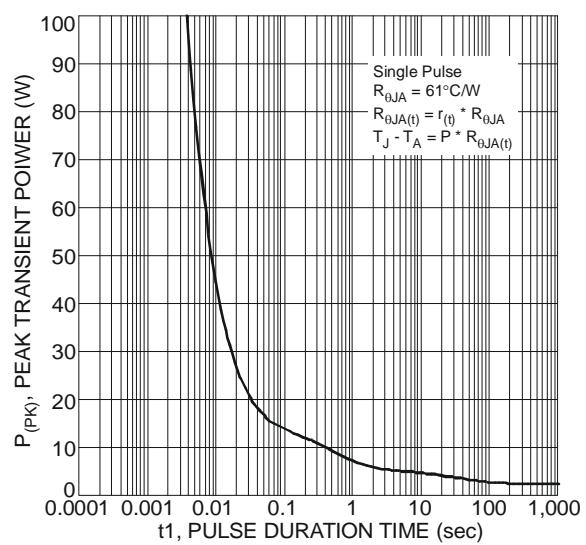
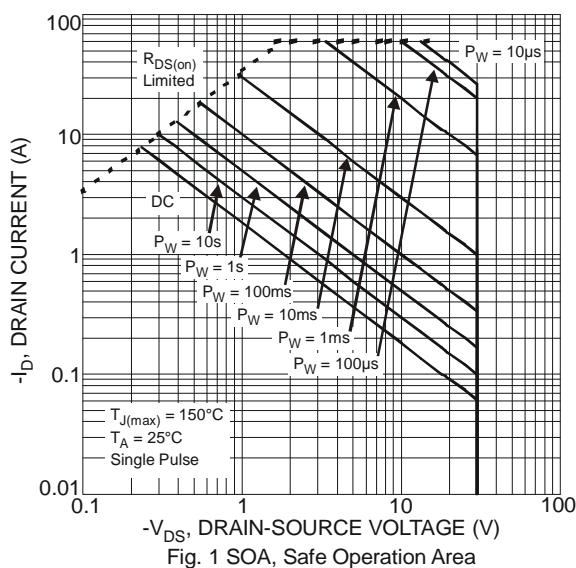
P35 = Product Type Marking Code
 YYWW = Date Code Marking
 YY = Last digit of year (ex: 11 = 2011)
 WW = Week code (01 ~ 53)

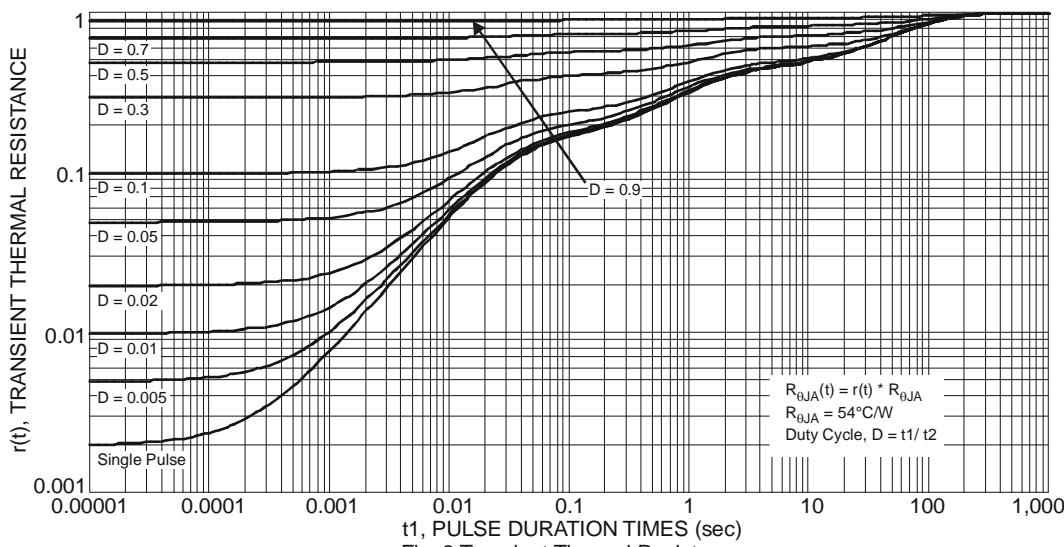
Maximum Ratings @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	-30	V
Gate-Source Voltage			V_{GSS}	± 25	V
Continuous Drain Current (Note 6) $V_{GS} = -10\text{V}$	Steady State	$T_A = 25^\circ\text{C}$ $T_A = 70^\circ\text{C}$	I_D	-8.5 -6.7	A
	$t < 10\text{s}$	$T_A = 25^\circ\text{C}$ $T_A = 70^\circ\text{C}$	I_D	-12.5 -10.0	A
Continuous Drain Current (Note 6) $V_{GS} = -5\text{V}$	Steady State	$T_A = 25^\circ\text{C}$ $T_A = 70^\circ\text{C}$	I_D	-7.0 -5.5	A
	$t < 10\text{s}$	$T_A = 25^\circ\text{C}$ $T_A = 70^\circ\text{C}$	I_D	-10.0 -8.0	A
Pulsed Drain Current (10 μs pulse, duty cycle = 1%)			I_{DM}	-70	A
Maximum Continuous Body Diode Forward Current (Note 6)			I_S	-3.6	A

Thermal Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)		P_D	0.95	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	$R_{\theta JA}$	135	$^\circ\text{C/W}$
	$t < 10\text{s}$		65	$^\circ\text{C/W}$
Total Power Dissipation (Note 6)		P_D	2.3	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady state	$R_{\theta JA}$	55	$^\circ\text{C/W}$
	$t < 10\text{s}$		26	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	6.14	$^\circ\text{C/W}$
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

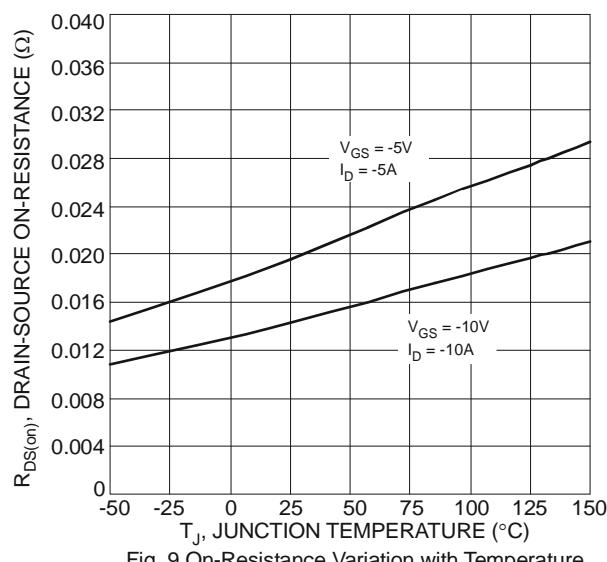
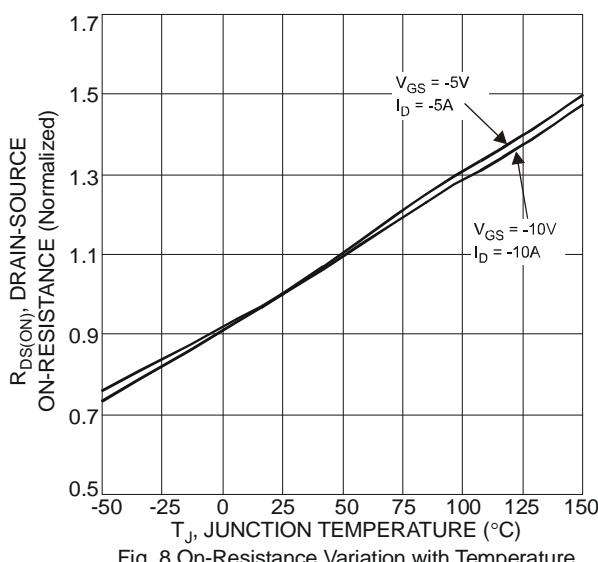
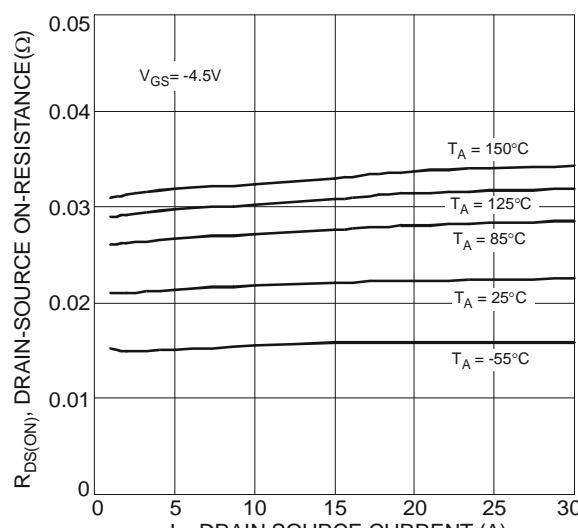
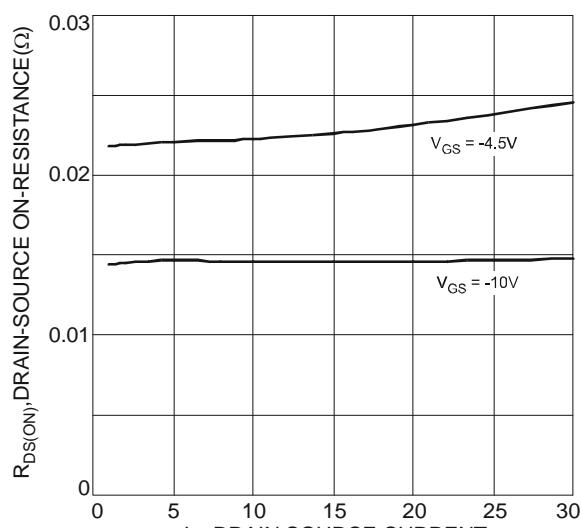
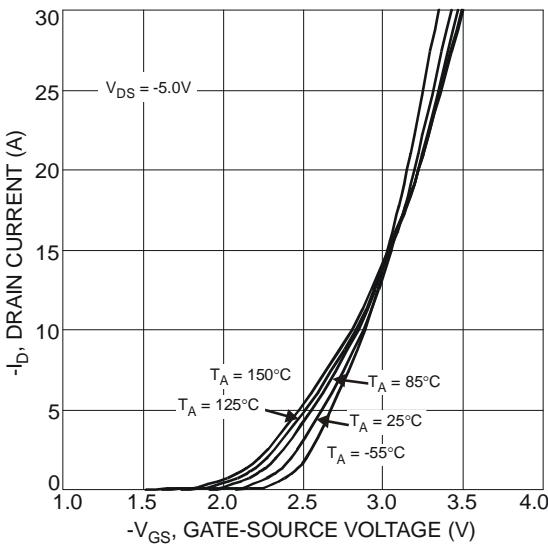
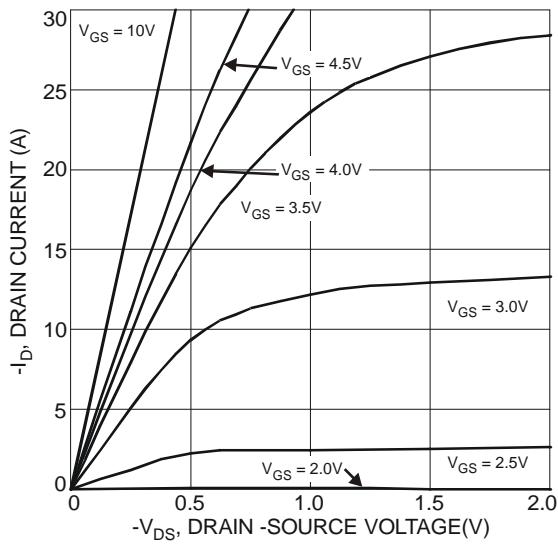



Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-30	-	-	V	$\text{V}_{\text{GS}} = 0\text{V}$, $\text{I}_D = -250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	-	-	-1.0	μA	$\text{V}_{\text{DS}} = -30\text{V}$, $\text{V}_{\text{GS}} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	-	-	± 100	nA	$\text{V}_{\text{GS}} = \pm 25\text{V}$, $\text{V}_{\text{DS}} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$\text{V}_{\text{GS(th)}}$	-1.0	-1.7	-2.5	V	$\text{V}_{\text{DS}} = \text{V}_{\text{GS}}$, $\text{I}_D = -250\mu\text{A}$
Static Drain-Source On-Resistance	$\text{R}_{\text{DS (ON)}}$	-	15	20	$\text{m}\Omega$	$\text{V}_{\text{GS}} = -10\text{V}$, $\text{I}_D = -8\text{A}$
		-	21	29		$\text{V}_{\text{GS}} = -5\text{V}$, $\text{I}_D = -5\text{A}$
Forward Transfer Admittance	$ \text{Y}_{\text{fs}} $	-	22	-	S	$\text{V}_{\text{DS}} = -5\text{V}$, $\text{I}_D = -10.0\text{A}$
Diode Forward Voltage	V_{SD}	-	-0.74	-1.0	V	$\text{V}_{\text{GS}} = 0\text{V}$, $\text{I}_S = -1\text{A}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	-	1633	-	pF	$\text{V}_{\text{DS}} = -15\text{V}$, $\text{V}_{\text{GS}} = 0\text{V}$, $f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	-	459	-	pF	
Reverse Transfer Capacitance	C_{rss}	-	214	-	pF	
Gate Resistance	R_g	-	6.5	13	Ω	$\text{V}_{\text{DS}} = 0\text{V}$, $\text{V}_{\text{GS}} = 0\text{V}$, $f = 1\text{MHz}$
Total Gate Charge $\text{V}_{\text{GS}} = -4.5\text{V}$	Q_g	-	17	-	nC	$\text{V}_{\text{DS}} = -15\text{V}$, $\text{V}_{\text{GS}} = -10\text{V}$, $\text{I}_D = 8\text{A}$
Total Gate Charge $\text{V}_{\text{GS}} = -10\text{V}$	Q_g	-	35.5	-	nC	
Gate-Source Charge	Q_{gs}	-	4.6	-	nC	
Gate-Drain Charge	Q_{gd}	-	5.7	-	nC	
Turn-On Delay Time	$\text{t}_{\text{D(on)}}$	-	8.5	-	ns	$\text{V}_{\text{GEN}} = -10\text{V}$, $\text{V}_{\text{DD}} = -15\text{V}$, $\text{R}_{\text{GEN}} = 3\Omega$, $\text{I}_D = -15\text{A}$
Turn-On Rise Time	t_r	-	14	-	ns	
Turn-Off Delay Time	$\text{t}_{\text{D(off)}}$	-	50	-	ns	
Turn-Off Fall Time	t_f	-	25.8	-	ns	

Notes:

5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.



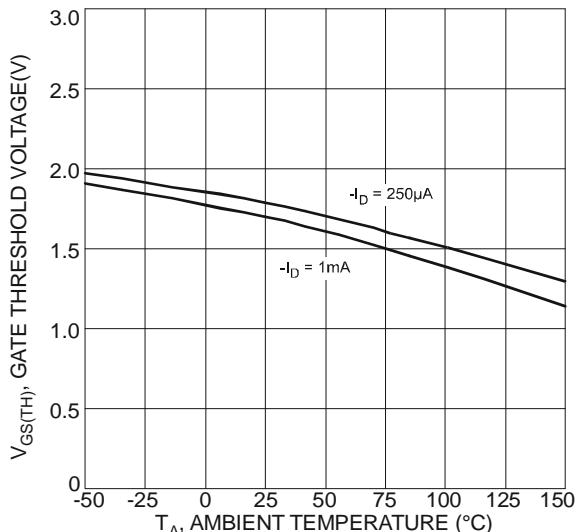


Fig. 10 Gate Threshold Variation vs. Ambient Temperature

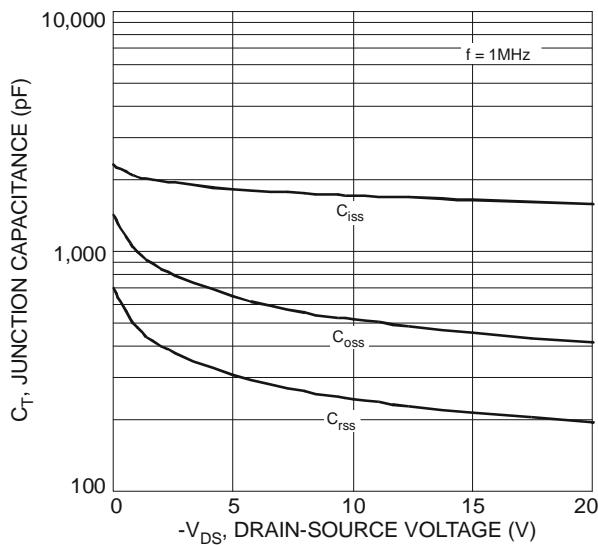


Fig. 12 Typical Junction Capacitance

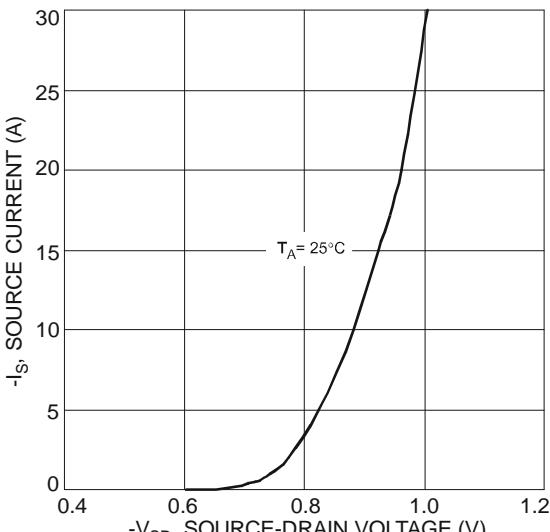


Fig. 11 Diode Forward Voltage vs. Current

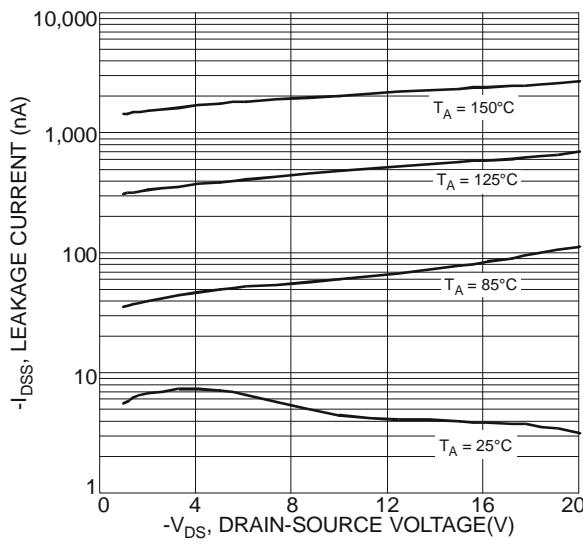


Fig. 13 Typical Drain-Source Leakage Current vs. Voltage

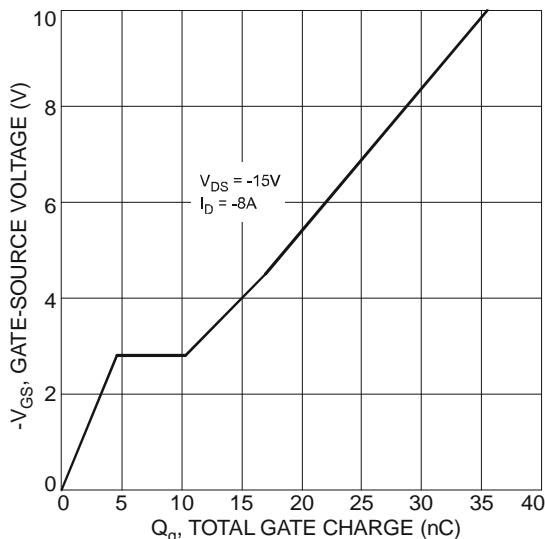
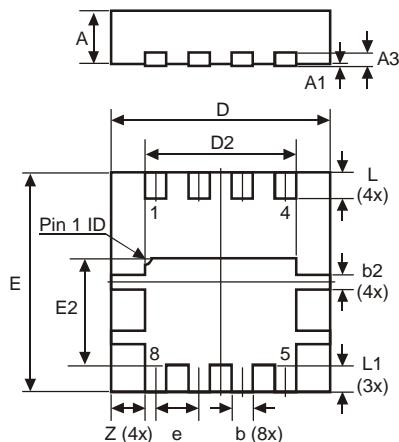


Fig. 14 Gate-Charge Characteristics

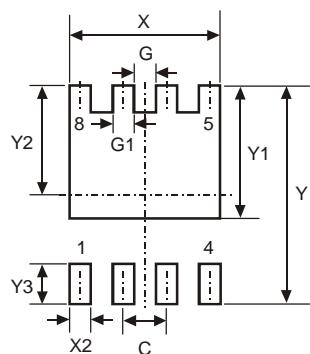
Package Outline Dimensions



POWERDI3333-8			
Dim	Min	Max	Typ
D	3.25	3.35	3.30
E	3.25	3.35	3.30
D2	2.22	2.32	2.27
E2	1.56	1.66	1.61
A	0.75	0.85	0.80
A1	0	0.05	0.02
A3	—	—	0.203
b	0.27	0.37	0.32
b2	—	—	0.20
L	0.35	0.45	0.40
L1	—	—	0.39
e	—	—	0.65
Z	—	—	0.515

All Dimensions in mm

Suggested Pad Layout



Dimensions	Value (in mm)
C	0.650
G	0.230
G1	0.420
Y	3.700
Y1	2.250
Y2	1.850
Y3	0.700
X	2.370
X2	0.420

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