2.5V, 3.3V LVCMOS 1:10 Clock Fanout Buffer
AK8180D

Features

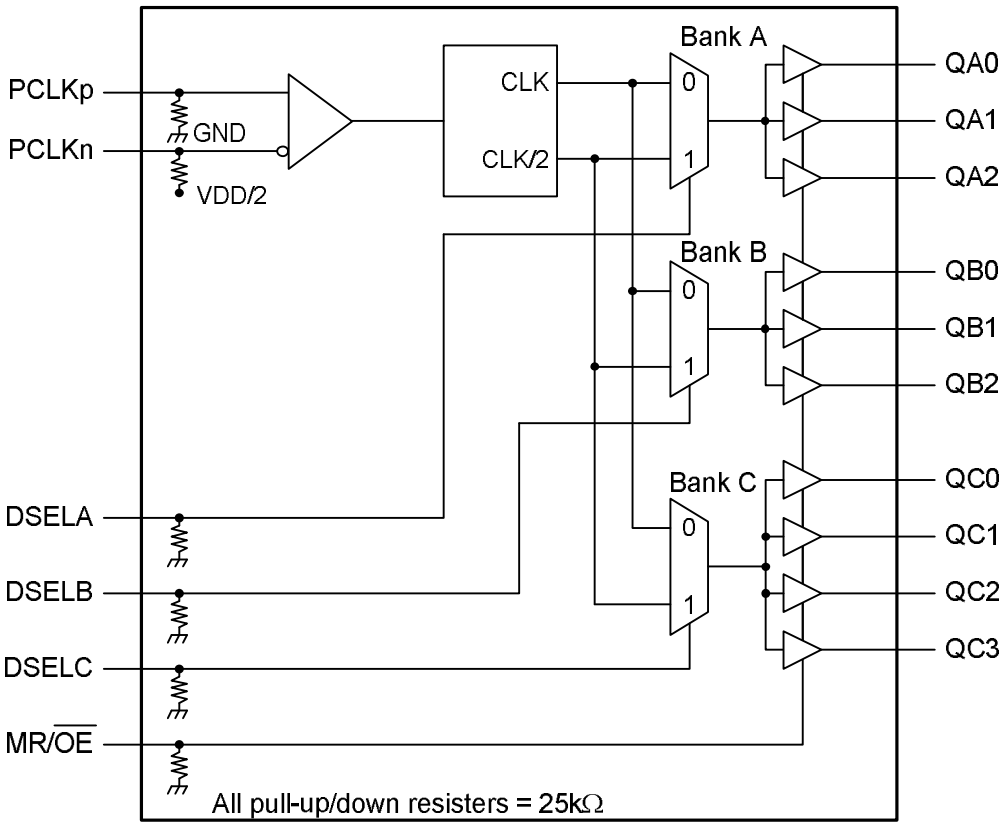
- 3 – 3 – 4 configurable 10 LVCMOS outputs
- Translate LVPECL input to LVCMOS output
- Single, dual and mixed voltage supply available on 2.5V and 3.3V
- Clock output frequency up to 250MHz
- Output-to-output skew : 200ps max
- High-impedance output control
- Enable to drive up to 20 series terminated clock lines
- Operating Temperature Range: -40 to +85℃
- Package: 32-pin LQFP (Pb free)
- Pin compatible with MPC9456

Description

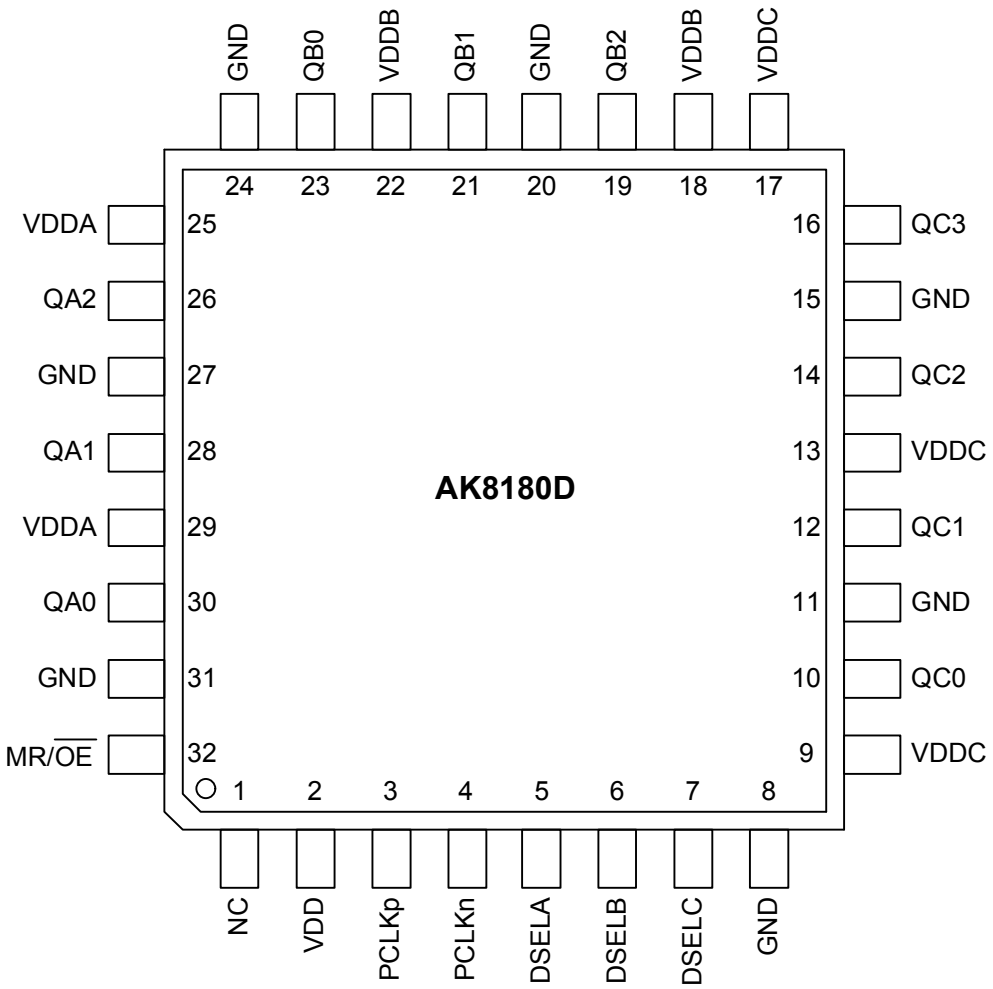
The AK8180D is a member of AKM's LVCMOS clock fanout buffer family designed for telecom, networking and computer applications, requiring a range of clocks with high performance and low skew. The AK8180D distributes 10 buffered clocks configured by pin-setting per bank. The 10 outputs can drive 10 terminated 50 Ω clock lines.

AK8180D are derived from AKM's long-term-experienced clock device technology, and enable clock output to perform low skew. The AK8180D is available in a 7mm x 7mm 32-pin LQFP package.

Block Diagram



Pin Descriptions



Package: 32-Pin LQFP(Top View)

Pin No.	Pin Name	Pin Type	Pullup /down	Description
1	NC	---	--	No internal connection
2	VDD	--	--	Power Supply
3	PCLKp	IN	PD	LVPECL Differential Clock Inputs
4	PCLKn	IN	PU/PD	
5	DSELA	IN	PD	Divide Select Input for Output Bank A
6	DSELB	IN	PD	Divide Select Input for Output Bank B
7	DSELC	IN	PD	Divide Select Input for Output Bank C
8,	GND	--	--	Ground
9	VDDC	--	--	Power Supply for Output bank C
10	QC0	OUT	--	Clock output Bank C
11	GND	--	--	Ground
12	QC1	OUT	--	Clock output Bank C

(continued on next page)

Pin No.	Pin Name	Pin Type	Pullup /down	Description
13	VDDC	--	--	Power Supply for Output bank C
14	QC2	OUT	--	Clock output Bank C
15	GND	--	--	Ground
16	QC3	OUT	--	Clock output Bank C
17	VDDC	--	--	Power Supply for Output bank C
18	VDDB	--	--	Power Supply for Output bank B
19	QB2	OUT	--	Clock output Bank B
20	GND	--	--	Ground
21	QB1	OUT	--	Clock output Bank B
22	VDDB	--	--	Power Supply for Output bank B
23	QB0	OUT	--	Clock output Bank B
24	GND	--	--	Ground
25	VDDA	--	--	Power Supply for Output bank A
26	QA2	OUT	--	Clock output Bank A
27	GND	--	--	Ground
28	QA1	OUT	--	Clock output Bank A
29	VDDA	--	--	Power Supply for Output bank A
30	QA0	OUT	--	Clock output Bank A
31	GND	--	--	Ground
32	MR/$\overline{OE}$	IN	PD	Master Reset and Output Enable (Output disable = High impedance)

PU: Pull up PD: Pull down

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8180D	AK8180D	Tape and Reel	32-pin LQFP	-40 to 85 ℃

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 to 4.6	V
Input voltage	Vin	GND-0.3 to VDD+0.3	V
Input current (any pins except supplies)	I_{IN}	±10	mA
Storage temperature	Tstg	-55 to 130	°C

Note

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-40		85	°C
Supply voltage (1)	VDD	VDD±5%	2.375	2.5	2.625	V
			3.135	3.3	3.465	

(1) Power of 2.5V or 3.3V requires to be supplied from a single source. A decoupling capacitor of 0.1μF for power supply line should be located close to each VDD pin.

Supported VDD Supply Voltage Configurations

Supply Voltage Configuration	VDD	VDDA	VDDB	VDDC	GND
3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	0 V
3.3 V and 2.5 V	3.3 V	3.3 V or 2.5 V	3.3 V or 2.5 V	3.3 V or 2.5 V	0 V
2.5 V	2.5 V	2.5 V	2.5 V	2.5 V	0 V

General Specification

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Termination Voltage	VTT			VDD/2		V
ESD Protection 1	MM	Machine model	200			V
ESD Protection 2	HBM	Human Body Model	2000			V
Latch-Up Immunity	LU		200			mA
Power Dissipation Capacitance		per output		10		pF
Input Capacitance				4.0		pF

Power Supply Current <3.3V>

VDD= 3.3V±5%, Ta: -40 to +85℃

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Full operation (1)	IDD1	CCLK0=250MHz CLK_SEL=L		95	120	mA
Quiescent state (1)(2)	IDD2			1.6	2.6	mA

(1) The outputs have no loads. (2) All inputs are in default state by the internal pull up/down resisters.

DC Characteristics <3.3V>

All specifications at VDD=VDDA=VDDB=VDDC= 3.3V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
High Level Input Voltage	V_{IH}	LVCMOS	2.0		VDD+0.3	V
Low Level Input Voltage	V_{IL}	LVCMOS	-0.3		0.8	V
Peak-to-Peak Input Voltage	Vpp	LVPECL	250			mV
Common Mode Range (1)	Vcmr	LCPECL	1.1		VDD-0.6	V
Input Current (2)	I_L1	Vin=GND or VDD			200	μA
High Level Output Voltage	V_{OH}	I_{OH}= -24mA (3)	2.4			V
Low level Output Voltage	V_{OL}	I_{OL}= +24mA (3) I_{OL}= +12mA			0.55 0.30	V
Output Impedance				14-17		Ω

(1) Vcmr(DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the Vcmr range and the input swing lies within the Vpp(DC) specification.

(2) Input pull-up / pull down resistors influence input current.

(3) The AK8180D is capable of driving 50 Ω transmission lines of the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of VTT. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.

(4) I_{DDQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

AC Characteristics <3.3V> (1)

All specifications at VDD=VDDA=VDDB=VDDC= 3.3V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Input Frequency	f_{IN}	Pin: PCLKp/n	0		250	MHz
Input Pulse Width	t_{pwIN}	Pin: PCLKp/n	1.4			ns
Peak-to-Peak Input Voltage	Vpp	Pin: PCLKp/n	500		1000	mV
Common Mode Range (2)	Vcmr	Pin: PCLKp/n	1.3		VDD-0.8	
Input Rise/Fall time (3)	t_{rIN},t_{fOUT}	Pin: PCLKp/n 0.8 to 2.0V			1.0	ns
Output Frequency	f_{OUT}	Pin: Q0-11	0		250	MHz
Propagation Delay	t_{PLH} t_{PHL}	PCLK to any Q	1.3	2.2	3.55	ns
Output Disable Time	t_{PLZ},t_{PHZ}				10	ns
Output Enable Time	t_{PZL},t_{PZH}				10	ns
Output-to-Output Skew	t_{skPP}	Within one bank Any output, same output divider Any output, Any output divider			150 200 350	ps
Device-to-Device Skew	t_{skD}				2.25	ns
Output Pulse Skew (4)	t_{skO}				200	ps

(continued on next page)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Duty Cycle	DC_{OUT}	DC_{REF}= 50% x1 output DC_{REF}= 25-75% x1/2 output	45 47	50 50	55 53	%
Output Rise/Fall Time	t_r, t_f	0.55 to 2.4V	0.1		1.0	ns

(1) AC characteristics apply for parallel output termination of 50 Ω to VTT.
(2) The AK8180D is functional up to an input and output clock frequency of 350MHz and is characterized up to 250MHz.
(3) Vcmr(AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the Vcmr range and the input swing lies within the Vpp(AC) specification. Violation of Vcmr or Vpp impacts $t_{PLH/PHL}$ and t_{skD}.
(4) Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, input pulse width, output duty cycle and maximum frequency specifications.
(5) Output pulse skew t_{skO} is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$.
Output duty cycle is frequency dependent (= 0.5 ± t_{skO} x fout). For example at fout = 125 MHz the output duty cycle limit is 50% ± 2.5%.

Power Supply Current <2.5V>

VDD= 2.5V±5%, Ta: -40 to +85℃

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Full operation (1)	IDD1	CCLK0=250MHz CLK_SEL=L		71	95	mA
Quiescent state (1)(2)	IDD2			1.6	2.5	mA

(1) The outputs have no loads. (2) All inputs are in default state by the internal pull up/down resisters.

DC Characteristics <2.5V>

All specifications at VDD=VDDA=VDDB=VDDC= 2.5V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
High Level Input Voltage	V_{IH}	LVCMOS	1.7		VDD+0.3	V
Low Level Input Voltage	V_{IL}	LVCMOS	-0.3		0.7	V
Peak-to-Peak Input Voltage	Vpp	LVPECL	250			mV
Common Mode Range (1)	Vcmr	LVPECL	1.1		VDD-0.7	V
Input Current (2)	I_L1	Vin=GND or VDD			200	μA
High Level Output Voltage	V_{OH}	I_{OH}= -15mA (3)	1.8			V
Low level Output Voltage	V_{OL}	I_{OL}= +15mA (3)			0.6	V
Output Impedance				17-20		Ω

(1) Vcmr(DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the Vcmr range and the input swing lies within the Vpp(DC) specification.
(2) Input pull-up / pull down resistors influence input current.
(3) The AK8180D is capable of driving 50 Ω transmission lines of the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of VTT. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.
(4) I_{DDQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

AC Characteristics <2.5V> (1)

All specifications at VDD=VDDA=VDDB=VDDC= 2.5V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Input Frequency (2)	f_{IN}	Pin: PCLKp/n			250	MHz
Input Pulse Width	t_{pwIN}	Pin: PCLKp/n	1.4			ns
Peak-to-Peak Input Voltage	Vpp	Pin: PCLKp/n	500		1000	mV
Common Mode Range (2)	Vcmr	Pin: PCLKp/n	1.1		VDD-0.7	
Input Rise/Fall time (3)	t_{rIN},t_{fOUT}	Pin: PCLKp/n 0.8 to 2.0V			1.0	ns
Output Frequency (2)	f_{OUT}	DSELx = 0 x1 output DSELx = 1 x1/2 output			250 125	MHz
Propagation Delay	t_{PLH} t_{PHL}	PCLKp/n to any Q	1.4	2.4	4.4	ns
Output Disable Time	t_{PLZ},t_{PHZ}				10	ns
Output Enable Time	t_{PZL},t_{PZH}				10	ns
Output-to-Output Skew	t_{skPP}	Within one bank Any output, same output divider Any output, Any output divider			150 200 350	ps
Device-to-Device Skew	t_{skD}				3.0	ns
Output Pulse Skew (4)	t_{skO}				200	ps
Output Duty Cycle	DC_{OUT}	DC_{REF}= 50% x1 or 1/2 output	45	50	55	%
Output Rise/Fall Time	t_r, t_f	0.6 to 1.8V	0.1		1.0	ns

(1) AC characteristics apply for parallel output termination of 50 Ω to VTT.

(2) The AK8180D is functional up to an input and output clock frequency of 350MHz and is characterized up to 250MHz.

(3) Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, input pulse width, output duty cycle and maximum frequency specifications.

(4) Output pulse skew t_{skO} is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$.
Output duty cycle is frequency dependent (= 0.5 ± t_{skO} x fout). For example at fout = 125 MHz the output duty cycle limit is 50% ± 2.5%.

AC Characteristics <mixed with 3.3V and 2.5V> (1)(2)

All specifications at VDD, VDDB= 3.3V±5%, VDDA, VDDC=2.5V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Propagation Delay	t_{PLH}, t_{PHL}	PCLK to any Q	See 3.3V table			ns
Output-to-Output Skew	t_{skPP}	Within one bank Any output, same output divider Any output, Any output divider			150 250 350	ps
Device-to-Device Skew	t_{skD}				2.5	ns
Output Pulse Skew (3)	t_{skO}				250	ps
Output Duty Cycle	DC_{OUT}	DC_{REF}= 50% x1 or 1/2 output	45	50	55	%

(1) AC characteristics apply for parallel output termination of 50 Ω to VTT.

(2) For all other AC specifications, refer to 2.5V and 3.3V tables according to the supply voltage of the output bank.

(3) Output pulse skew t_{skO} is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$.
Output duty cycle is frequency dependent (= 0.5 ± t_{skO} x fout). For example at fout = 125 MHz the output duty cycle limit is 50% ± 2.5%.

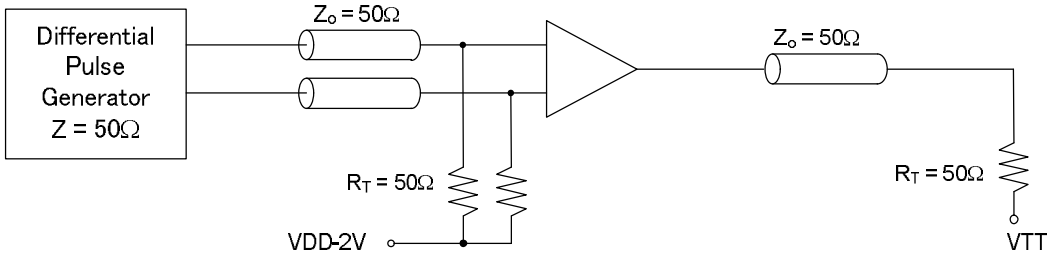


Figure 1 PCLK/PCLKn AC Test Reference

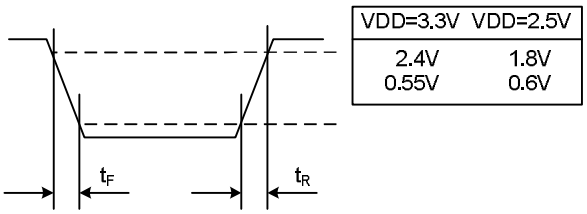


Figure 2 Output Translation Time Test Reference

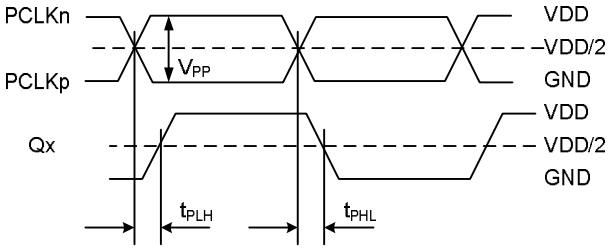
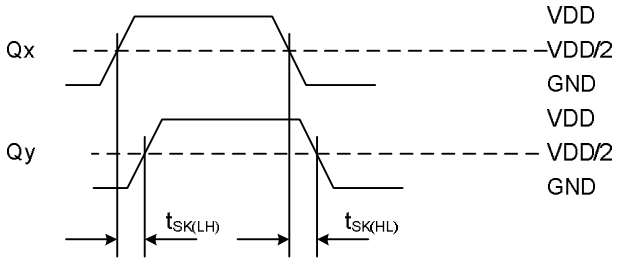
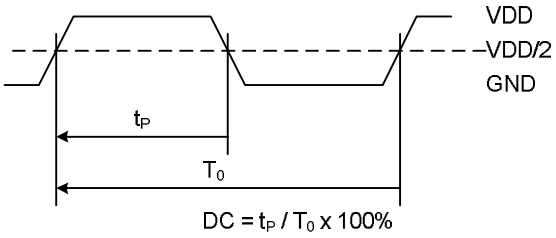


Figure 3 Propagation Delay Test Reference



The pin-to-pin skew is defined as the worst case difference in propagation delay between any two similar delay paths within a single device.

Figure 4 Output-to-Output Skew



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage.

Figure 5 Output Duty Cycle (DC)

Function Table

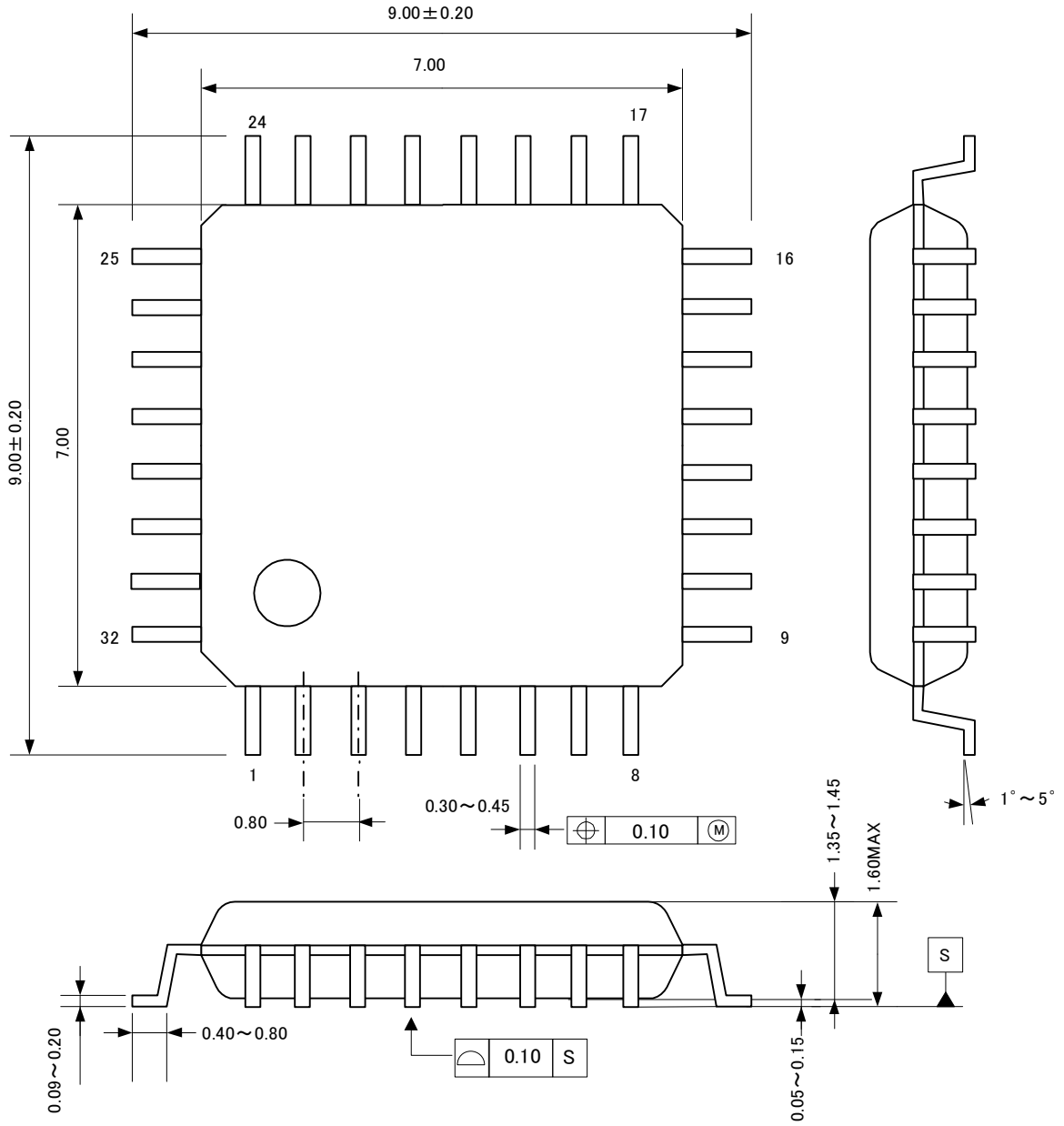
The following table shows the inputs/outputs clock state configured through the control pins.

Table 1: Control-Pin-Setting Function Table

Control Pin	Default	0	1
DSELA	0	QA0-2 = REFCLK x 1	QA0-2 = REFCLK x 1/2
DSELB	0	QB0-2 = REFCLK x 1	QB0-2 = REFCLK x 1/2
DSELC	0	QC0-3 = REFCLK x 1	QC0-3 = REFCLK x 1/2
MR/$\overline{OE}$	0	Output enabled	Internal reset. Outputs disabled. (High impedance)

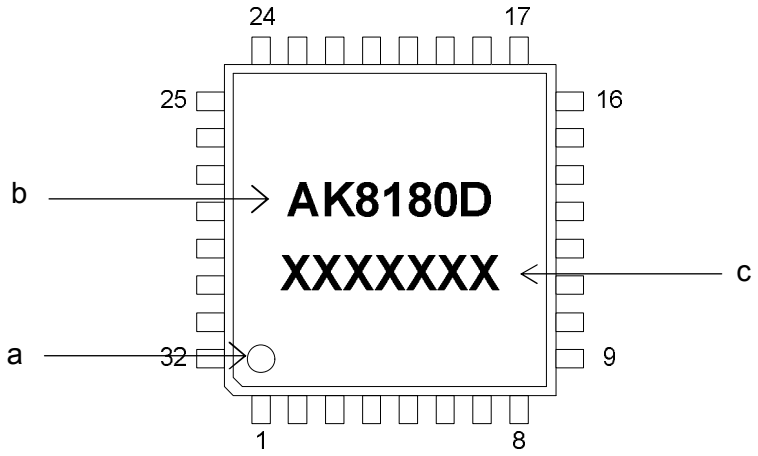
Package Information

- **Mechanical data : 32-lead LQFP**



- **Marking**

a: #1 Pin Index
b: Part number
c: Date code (7 digits)



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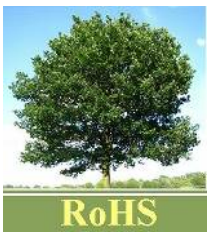
- **RoHS Compliance**



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(*) RoHS compliant products from AKM are identified with "Pb free" letter indication on product label posted on the anti-shield bag and boxes.

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  Note2) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
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