# LM4853 Boomer® Audio Power Amplifier Series Mono 1.5 W / Stereo 300mW Power Amplifier

**Check for Samples: LM4853**

## FEATURES

- **Mono 1.5W BTL or Stereo 300mW Output**
- **Headphone Sense**
- **"Click and Pop" Suppression Circuitry**
- **No Bootstrap Capacitors Required**
- **Thermal Shutdown Protection**
- **Unity-Gain Stable**
- **Available in Space-Saving VSSOP and WSON Packaging**

## APPLICATIONS

- **Portable Computers**
- **Desktop Computers**
- **PDA's**
- **Handheld Games**

## KEY SPECIFICATIONS

- **Output Power at 1% THD+N, 1kHz:**
  - **LM4853LD 3Ω BTL 1.9W (typ)**
  - **LM4853LD 4Ω BTL 1.7W (typ)**
  - **LM4853MM 4Ω BTL 1.5W (typ)**
  - **LM4853MM,LD 8Ω BTL 1.1W (typ)**
  - **LM4853MM,LD 8Ω SE 300mW (typ)**
  - **LM4853MM,LD 32Ω SE 95mW (typ)**
- **THD+N at 1kHz, 95mW into 32Ω SE 1% (typ)**
- **Single Supply Operation 2.4 to 5.5V**
- **Shutdown Current 18µA (typ)**

## DESCRIPTION

The LM4853 is an audio power amplifier capable of delivering 1.5W (typ) of continuous average power into a mono 4Ω bridged-tied load (BTL) with 1% THD+N or 95mW per channel of continuous average power into stereo 32Ω single-ended (SE) loads with 1% THD+N, using a 5V power supply.

The LM4853 can automatically switch between mono BTL and stereo SE modes utilizing a headphone sense pin. It is ideal for any system that provides both a monaural speaker output and a stereo line or headphone output

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. Since the LM4853 does not require bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems.

The LM4853 features an externally controlled, micropower consumption shutdown mode and thermal shutdown protection. The unity-gain stable LM4853's gain is set by external gain-setting resistors

## Connection Diagram

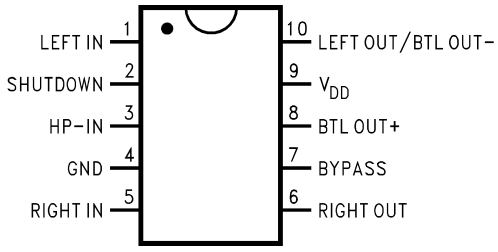


**Figure 1. 10 Lead VSSOP – Top View**
**See Package Number DGS**

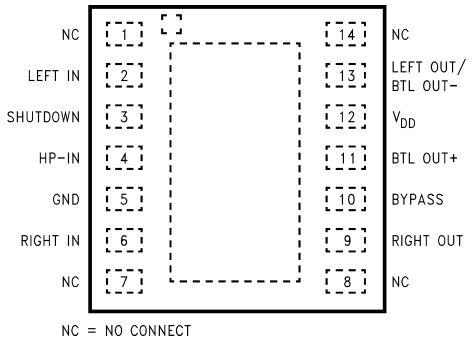


**Figure 2. 14 Lead WSON – Top View**
**See Package Number NHE0014A**

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## Typical Application

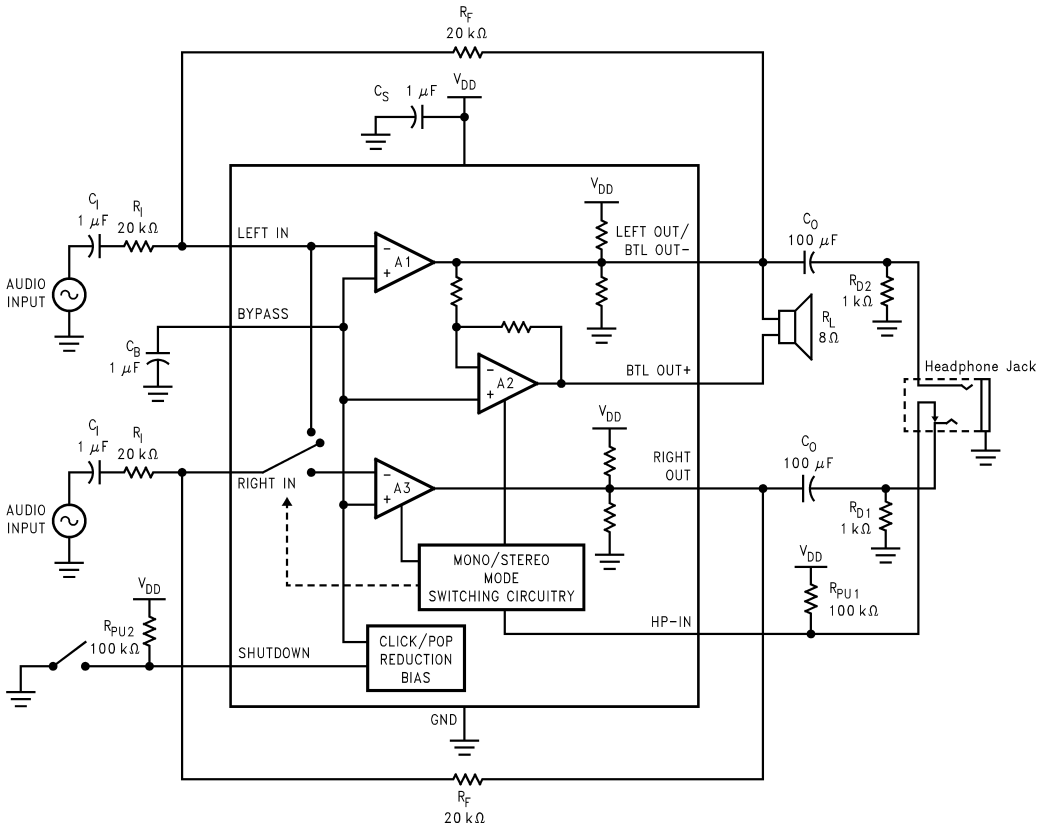



**Figure 3. Typical Audio Amplifier Application Circuit**

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings(1)(2)

| | | | |
|---|---|---|---|
| Supply Voltage | | | 6.0V |
| Storage Temperature | | | −65°C to +150°C |
| ESD Susceptibility(3) | | | 3.5kV |
| ESD Machine model(4) | | | 250V |
| Junction Temperature ($T_J$) | | | 150°C |
| Solder Information | Small Outline Package | Vapor Phase (60 sec.) | 215°C |
| | | Infrared (15 sec.) | 220°C |
| Thermal Resistance | | $\theta_{JA}$ (typ)—DGS | 194°C/W |
| | | $\theta_{JC}$ (typ)—DGS | 52°C/W |
| | | $\theta_{JA}$ (typ)—NHE0014A(5) | 56°C/W |
| | | $\theta_{JC}$ (typ)—NHE0014A | 4.3°C/W |

(1) Absolute Maximum Rating indicate limits beyond which damage to the device may occur.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Human body model, 100pF discharged through a 1.5kΩ resistor.
(4) Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50Ω).
(5) The given $\theta_{JA}$ is for an LM4853LD with the Exposed-DAP soldered to an exposed $1in^2$ area of 1oz printed circuit board copper.

## Operating Ratings(1)

| | |
|---|---|
| Temperature Range | −40°C ≤ to 85°C |
| Supply Voltage $V_{DD}$ | 2.4V ≤ $V_{DD}$ ≤ 5.5V |

(1) Absolute Maximum Rating indicate limits beyond which damage to the device may occur.

## Electrical Characteristics(1)(2)

The following specifications apply for $V_{DD}$= 5.0V, $T_A$= 25°C unless otherwise specified.

| Symbol | Parameter | Conditions | LM4853 | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typical(3) | Limit(4)(5) | |
| $V_{DD}$ | Supply Voltage | | | 2.4 | V (min) |
| | | | | 5.5 | V (max) |
| $I_{DD}$ | Supply Current | BTL Mode; $V_{IN}$ = 0V; $I_O$ = 0A | 2.4 | 7.0 | mA |
| | | SE Mode; $V_{IN}$ = 0V; $I_O$ = 0A | 2.4 | 7.0 | mA |
| $I_{SD}$ | Shutdown Current | SD Mode; $V_{SHUTDOWN}$ = $V_{DD}$ | 18 | | µA |
| $V_{OS}$ | Output Offset Voltage | BTL Mode; $A_V$ = 2 | 5.0 | 40 | mV |
| | | BTL OUT+ to BTL OUT− | | | |

(1) Absolute Maximum Rating indicate limits beyond which damage to the device may occur.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Typical specifications are specified at +25°C and represent the most likely parametric norm.
(4) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.
(5) Limits are specified to TI's AOQL ( Average Outgoing Quality Level ).

## Electrical Characteristics[1][2] (continued)

The following specifications apply for $V_{DD}$= 5.0V, $T_A$= 25°C unless otherwise specified.

| Symbol | Parameter | Conditions | LM4853 | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typical[3] | Limit[4][5] | |
| $P_O$ | Output Power | BTL Mode; $R_L$ = 3Ω THD+N = 1%; LM4853LD | 1.9 | | W |
| | | BTL Mode; $R_L$ = 4Ω THD+N = 1%; LM4853LD | 1.7 | | W |
| | | BTL Mode; $R_L$ = 4Ω THD+N = 1%; LM4853MM | 1.5 | | W |
| | | BTL Mode; $R_L$ = 8Ω THD+N = 1%; LM4853MM, LD | 1.1 | | W |
| | | SE Mode; $R_L$ = 8Ω THD+N = 1%; LM4853MM, LD | 300 | | mW |
| | | SE Mode; $R_L$ = 32Ω THD+N = 1%; LM4853MM, LD | 95 | | mW |
| $V_{IH}$ | Shutdown Input Voltage High | Is < 80µA | | 2.0 | V (min) |
| $V_{IL}$ | Shutdown Input Voltage Low | Is > 0.5mA | | 0.8 | V (max) |
| Crosstalk | Channel Seperation | SE Mode, $R_L$ = 32Ω; f = 1kHz | 73 | | dB |

## Electrical Characteristics[1][2]

The following specifications apply for $V_{DD}$= 3.3V, $T_A$= 25°C unless otherwise specified.

| Symbol | Parameter | Conditions | LM4853 | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typical[3] | Limit[4][5] | |
| $I_{DD}$ | Supply Current | BTL Mode; $V_{IN}$ = 0V; $I_O$ = 0A | 2.0 | | mA |
| | | SE Mode; $V_{IN}$ = 0V; $I_O$ = 0A | 2.0 | | mA |
| $I_{SD}$ | Shutdown Current | SD Mode; $V_{SHUTDOWN}$ = $V_{DD}$ | 12 | | µA |
| $V_{OS}$ | Output Offset Voltage | BTL Mode; $A_V$ = 2 BTL OUT+ to BTL OUT− | 5.0 | 40 | mV |
| $P_O$ | Output Power | BTL Mode; $R_L$ = 8Ω THD+N = 1% | 440 | | mW |
| | | SE Mode; $R_L$ = 32Ω THD+N = 1% | 40 | | mW |
| $V_{IH}$ | Shutdown Input Voltage High | Is < 80µA | | 2.0 | V (min) |
| $V_{IL}$ | Shutdown Input Voltage Low | Is > 0.5mA | | 0.8 | V (max) |

(1) Absolute Maximum Rating indicate limits beyond which damage to the device may occur.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Typical specifications are specified at +25°C and represent the most likely parametric norm.
(4) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.
(5) Limits are specified to TI's AOQL ( Average Outgoing Quality Level ).

## Electrical Characteristics (1)(2)

The following specifications apply for $V_{DD}$= 2.7V, $T_A$= 25°C unless otherwise specified.

| Symbol | Parameter | Conditions | LM4853 | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typical (3) | Limit (4)(5) | |
| $I_{DD}$ | Supply Current | BTL Mode; $V_{IN}$ = 0V; $I_O$ = 0A | 1.8 | | mA |
| | | SE Mode; $V_{IN}$ = 0V; $I_O$ = 0A | 1.8 | | mA |
| $I_{SD}$ | Shutdown Current | SD Mode; $V_{SHUTDOWN}$ = $V_{DD}$ | 10 | | µA |
| $V_{OS}$ | Output Offset Voltage | BTL Mode; $A_V$ = 2<br>BTL OUT+ to BTL OUT− | 5.0 | 40 | mV |
| $P_O$ | Output Power | BTL Mode; $R_L$ = 8Ω<br>THD+N = 1% | 300 | | mW |
| | | SE Mode; $R_L$ = 32Ω<br>THD+N = 1% | 25 | | mW |
| $V_{IH}$ | Shutdown Input Voltage High | Is < 80 µA | | 2.0 | V (min) |
| $V_{IL}$ | Shutdown Input Voltage Low | Is > 0.5mA | | 0.8 | V (max) |

(1) Absolute Maximum Rating indicate limits beyond which damage to the device may occur.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Typical specifications are specified at +25°C and represent the most likely parametric norm.
(4) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.
(5) Limits are specified to TI's AOQL ( Average Outgoing Quality Level ).

## External Components Description

See Figure 3.

| Components | | Functional Description |
|---|---|---|
| 1. | $R_i$ | Inverting input resistance which sets the closed-loop gain in conjunction with $R_f$. This resistor also forms a high pass filter with $C_i$ at $f_c = 1/(2\pi R_i C_i)$. |
| 2. | $C_i$ | Input coupling capacitor which blocks the DC voltage at the amplifier's input terminals. Also creates a highpass filter with $R_i$ at $f_c = 1/(2\pi R_i C_i)$. Refer to the section, PROPER SELECTION OF EXTERNAL COMPONENTS, for an explanation of how to determine the value of $C_i$. |
| 3. | $R_f$ | Feedback resistance which sets the closed-loop gain in conjunction with $R_i$. |
| 4. | $C_s$ | Supply bypass capacitor which provides power supply filtering. Refer to the POWER SUPPLY BYPASSING section for information concerning proper placement and selection of the supply bypass capacitor. |
| 5. | $C_B$ | Bypass pin capacitor which provides half-supply filtering. Refer to the section, PROPER SELECTION OF EXTERNAL COMPONENTS, for information concerning proper placement and selection of $C_B$. |
| 6. | $C_O$ | Output coupling capacitor which blocks the DC voltage at the amplifier's output. Forms a high pass filter with the single-ended load $R_L$ at $f_O = 1/(2\pi R_L C_O)$. |

## Typical Performance Characteristics
## LD Specific Characteristics

**LM4853LD**
**THD+N vs Frequency**

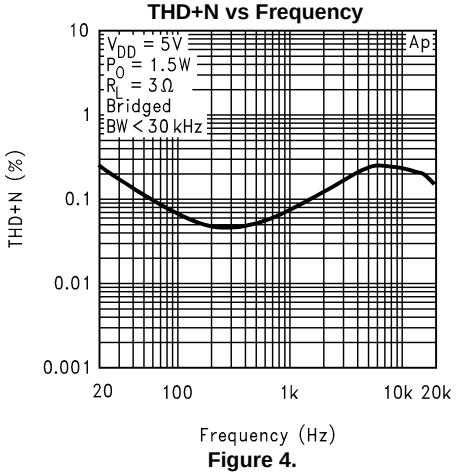



**Figure 4.**

**LM4853LD**
**THD+N vs Frequency**

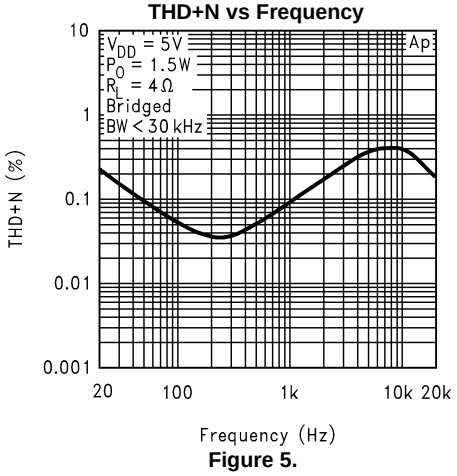



**Figure 5.**

**LM4853LD**
**THD+N vs Output Power**

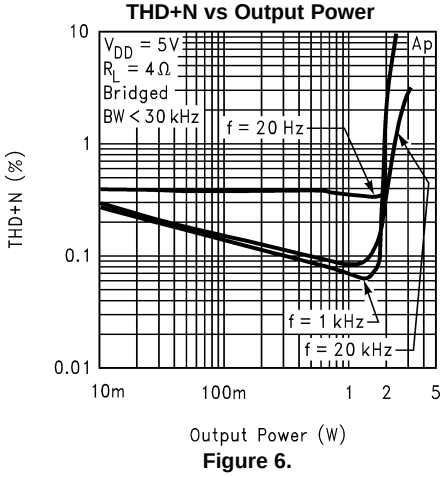



**Figure 6.**

**LM4853LD**
**THD+N vs Output Power**

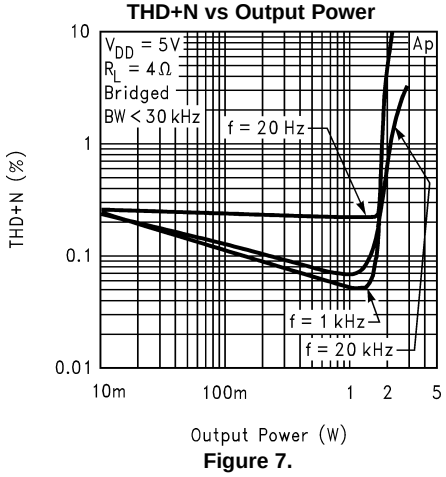



**Figure 7.**

**LM4853LD**
**Power Dissipation vs Output Power**

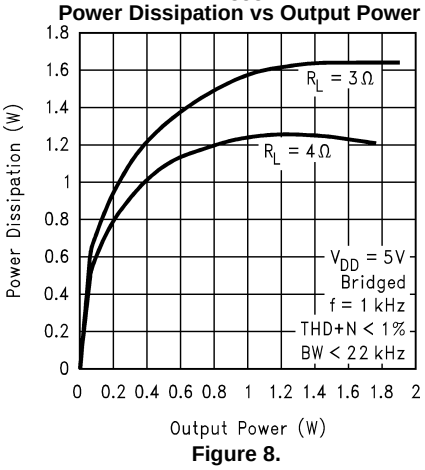



**Figure 8.**

**LM4853LD**
**Power Derating Curve**

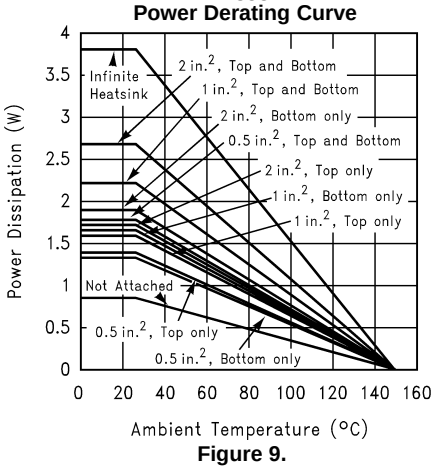



**Figure 9.**

## Typical Performance Characteristics

**THD+N vs Frequency**

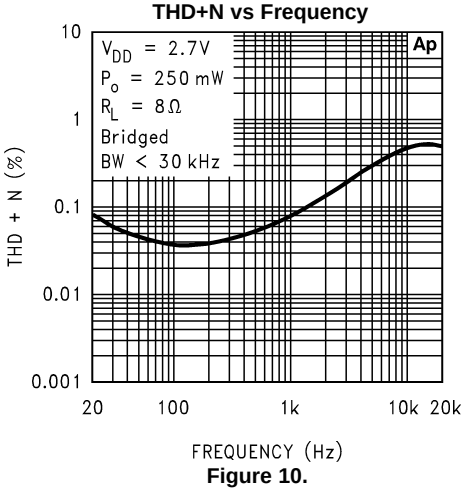



**Figure 10.**

**THD+N vs Frequency**

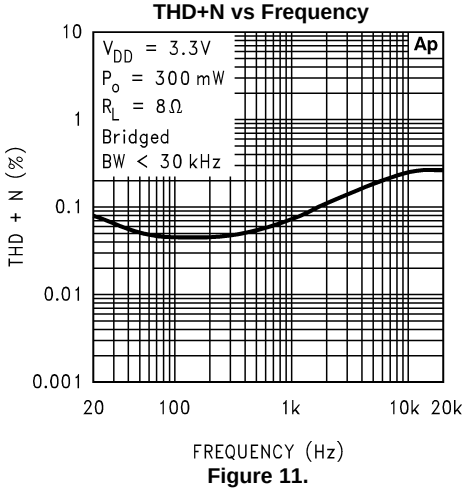



**Figure 11.**

**THD+N vs Frequency**

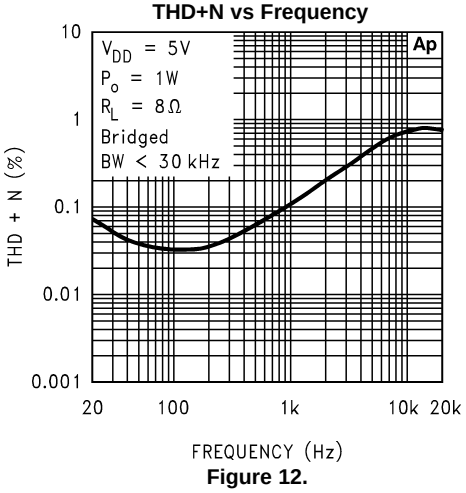



**Figure 12.**

**THD+N vs Frequency**

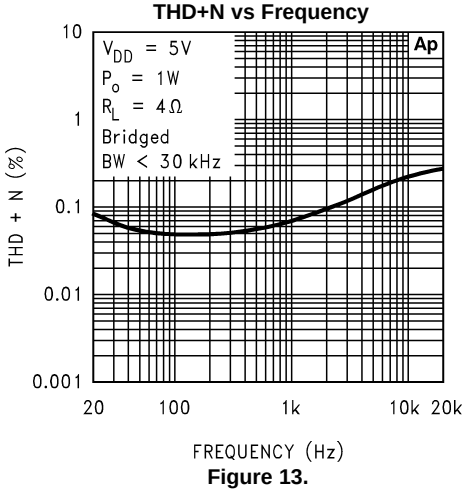



**Figure 13.**

**THD+N vs Frequency**

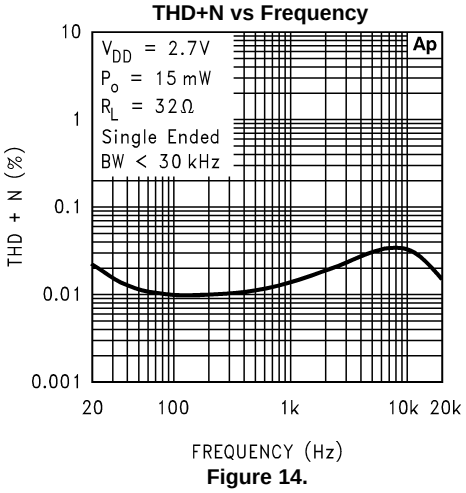



**Figure 14.**

**THD+N vs Frequency**

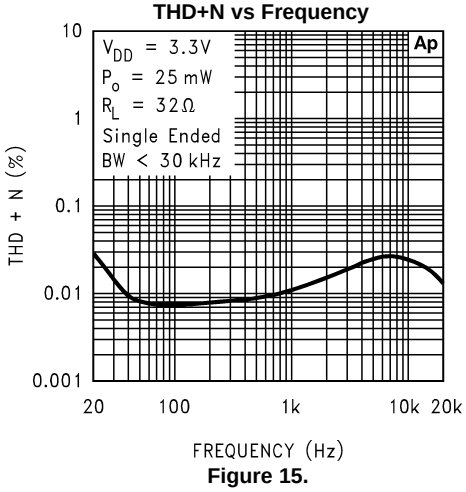



**Figure 15.**

## Typical Performance Characteristics (continued)

**THD+N vs Frequency**

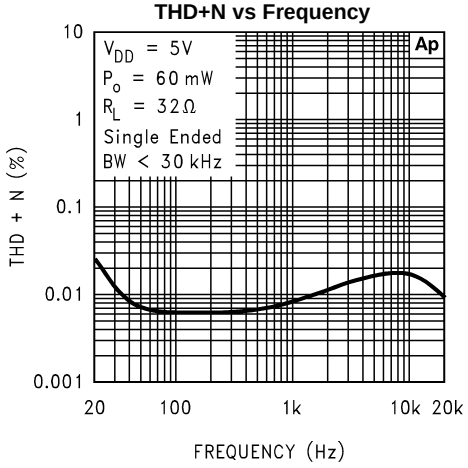



**Figure 16.**

**THD+N vs Output Power**

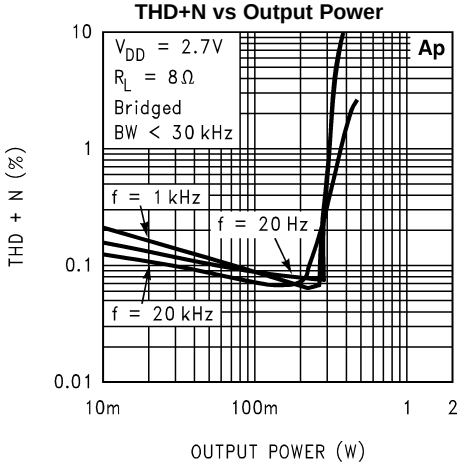



**Figure 17.**

**THD+N vs Output Power**

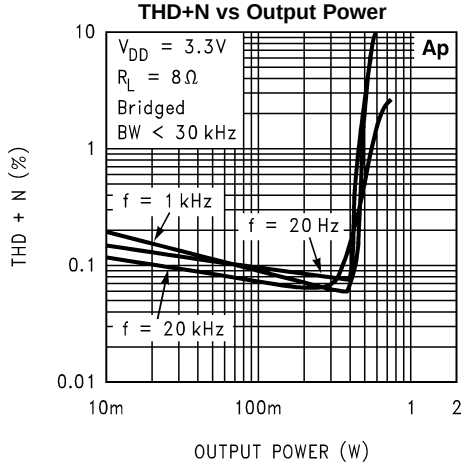



**Figure 18.**

**THD+N vs Output Power**

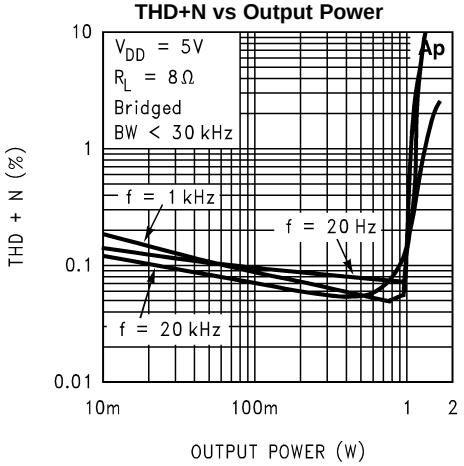



**Figure 19.**

**THD+N vs Output Power**

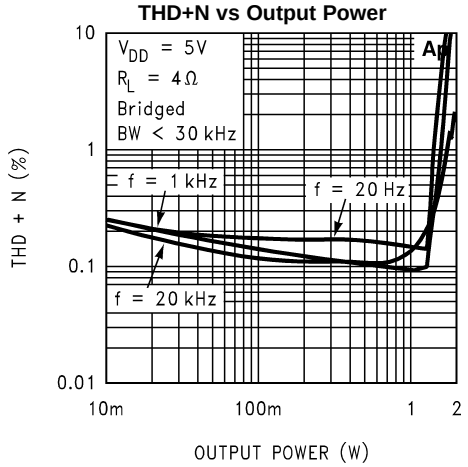



**Figure 20.**

**THD+N vs Output Power**

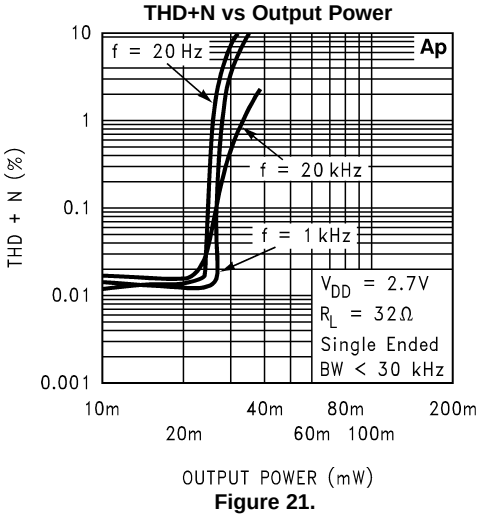



**Figure 21.**

## Typical Performance Characteristics (continued)

**THD+N vs Output Power**

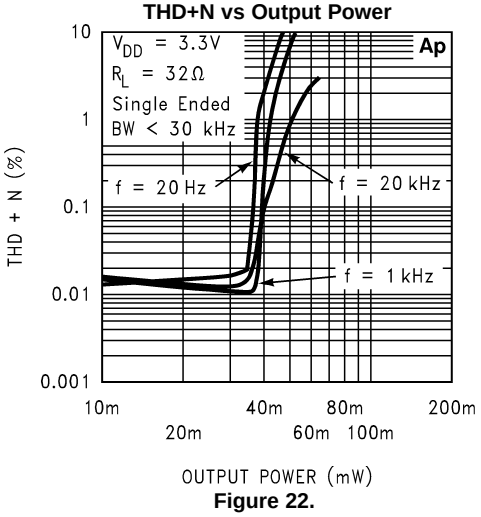



**Figure 22.**

**THD+N vs Output Power**

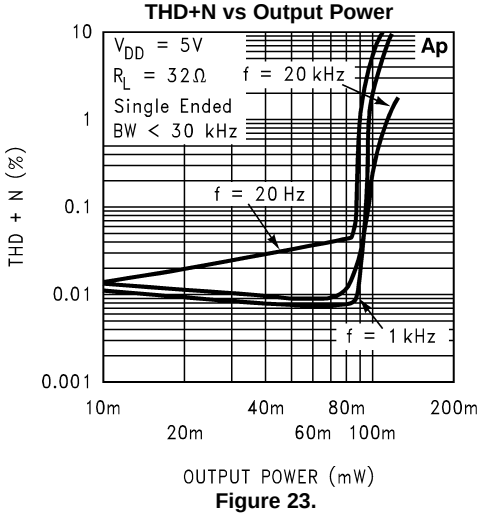



**Figure 23.**

**THD+N vs Output Power**

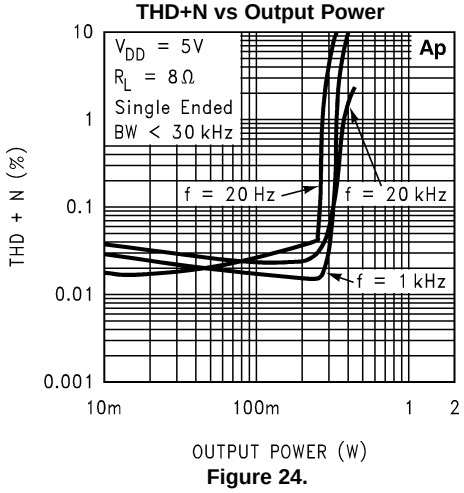



**Figure 24.**

**Output Power vs Load Resistance**

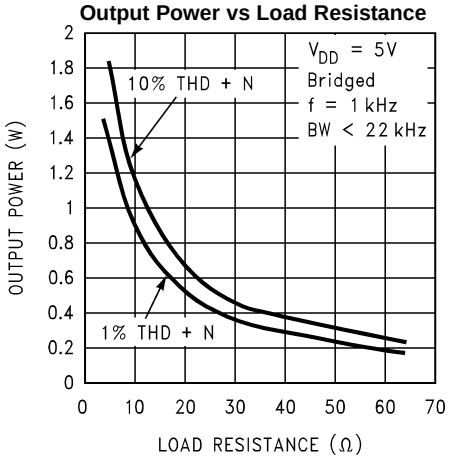



**Figure 25.**

**Output Power vs Load Resistance**

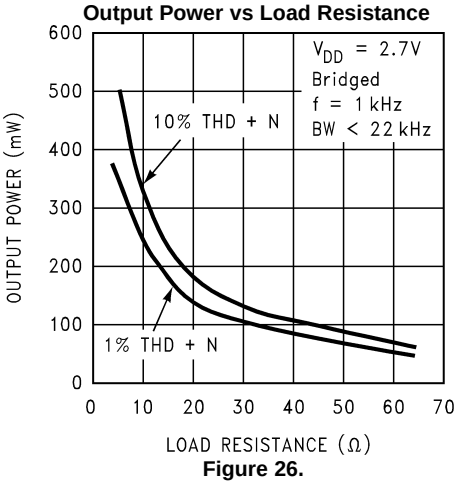



**Figure 26.**

**Output Power vs Supply Voltage**

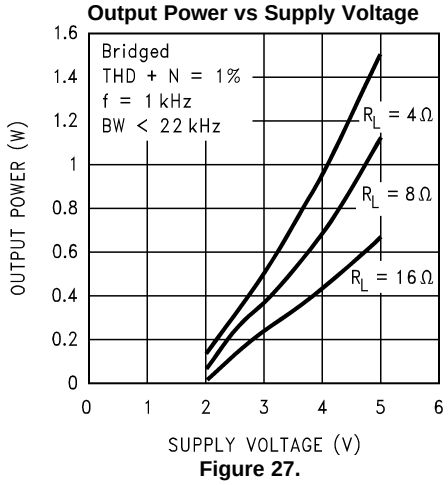



**Figure 27.**

## Typical Performance Characteristics (continued)

**Output Power vs Supply Voltage**

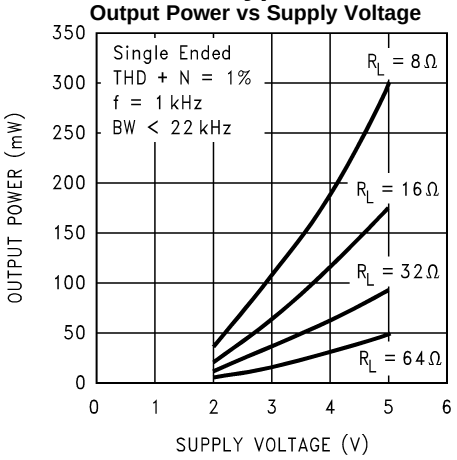



**Figure 28.**

**Dropout Voltage vs Supply Voltage**

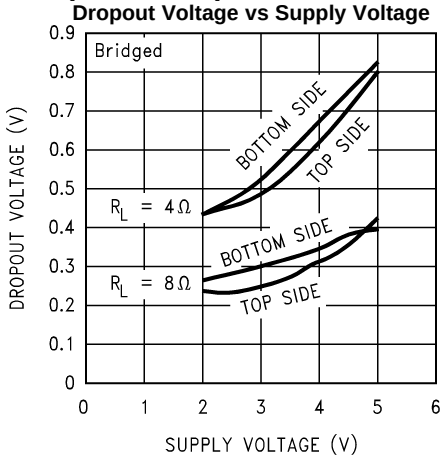



**Figure 29.**

**Power Dissipation vs Output Power**

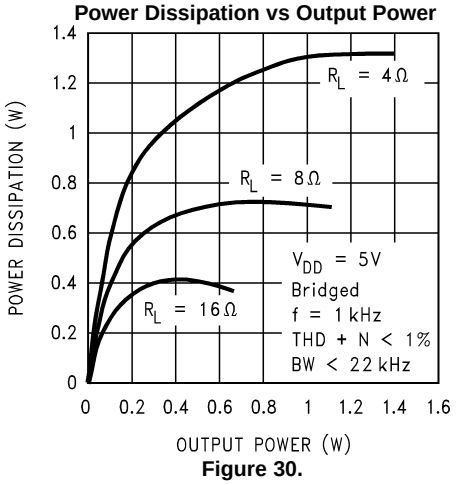



**Figure 30.**

**Power Dissipation vs Output Power**

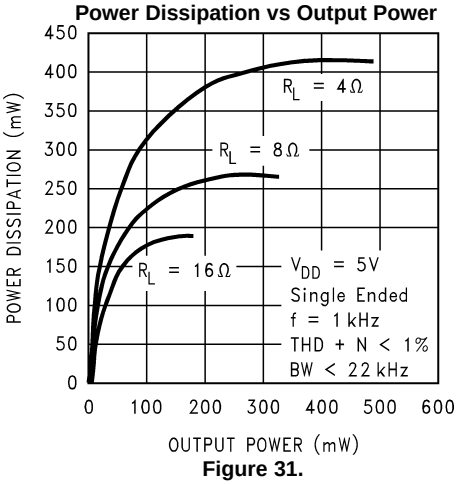



**Figure 31.**

**Power Derating Curve**

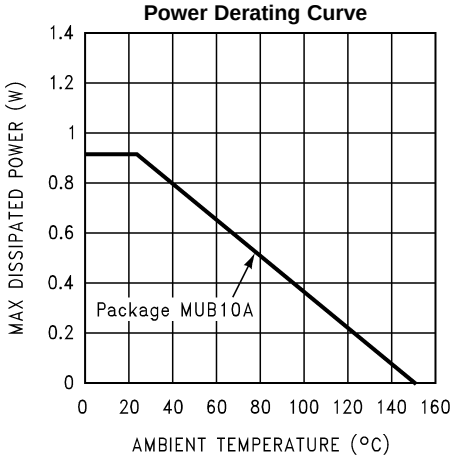



**Figure 32.**

**Channel Separation**

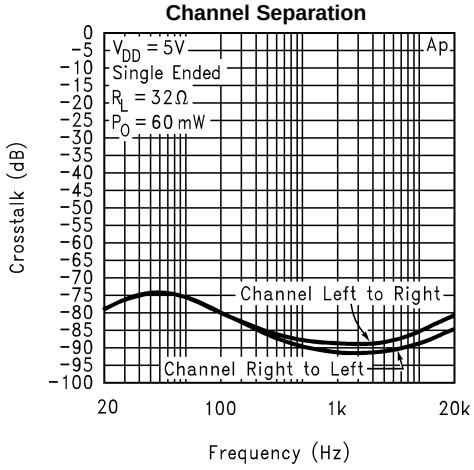



**Figure 33.**

## Typical Performance Characteristics (continued)

**Noise Floor**

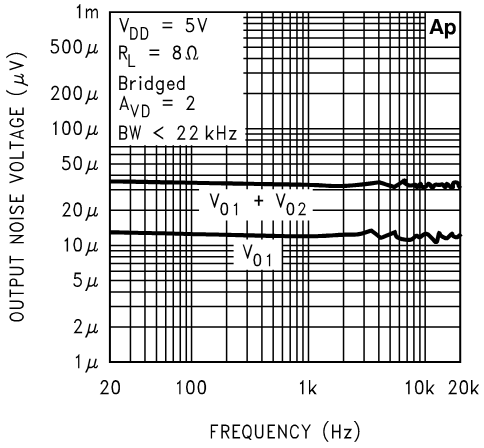



**Figure 34.**

**Open Loop Frequency Response**

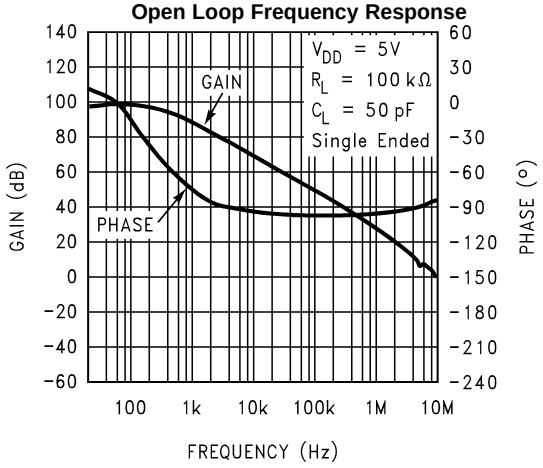



**Figure 35.**

**Supply Current vs Supply Voltage**

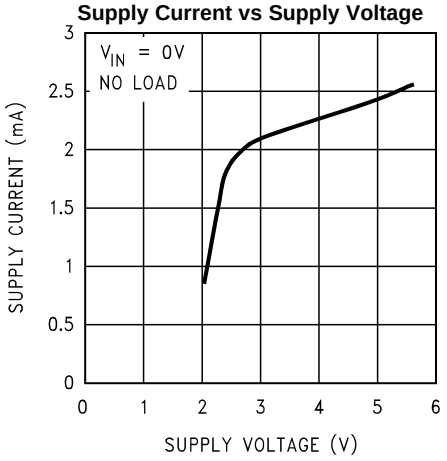



**Figure 36.**

**Power Supply Rejection Ratio**

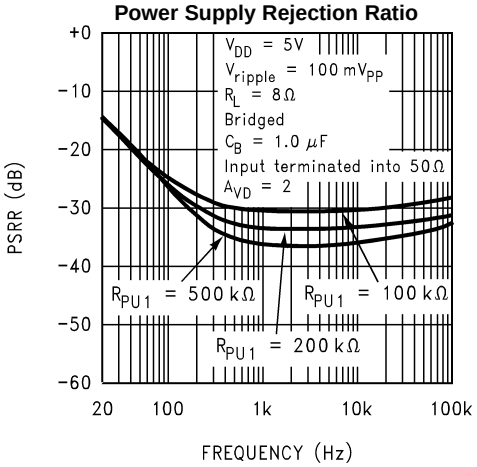



**Figure 37.**

**Power Supply Rejection Ratio**

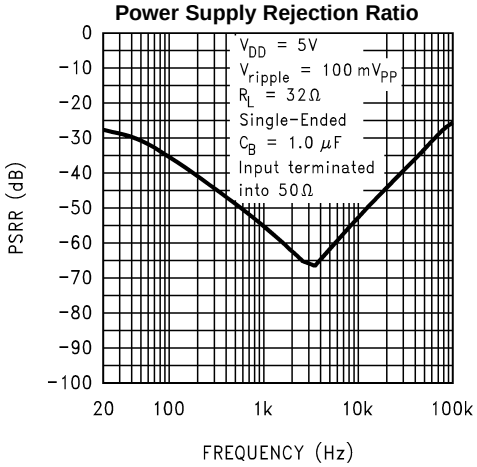



**Figure 38.**

# APPLICATION INFORMATION

## BRIDGED AND SINGLE-ENDED OPERATION

As shown in Typical Application, the LM4853 contains three operational amplifiers (A1-A3). These amplifiers can be configured for SE or BTL modes.

In the SE mode, the LM4853 operates as a high current output dual op amp. A1 and A3 are independent amplifiers with an externally configured gain of $A_V = - R_F/R_I$. The outputs of A1 and A3 are used to drive an external set of headphones plugged into the headphone jack. Amplifier A2 is shut down to a high output impedance state in SE mode. This prevents any current flow into the mono bridge-tied load, thereby muting it.

In BTL mode, A3 is shut down to a high impedance state. The audio signal from the RIGHT IN pin is directed to the inverting input of A1. As a result, the LEFT IN and RIGHT IN audio signals, $V_{INL}$ and $V_{INR}$, are summed together at the input of A1. A2 is then activated with a closed-loop gain of $A_V = -1$ fixed by two internal 20kΩ resistors. The outputs of A1 and A2 are then used to drive the mono bridged-tied load.

## EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATION

The LM4853's exposed-DAP (die attach paddle) package (LD) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane, and surrounding air. The result is a low voltage audio power amplifier that produces 1.7W at ≤ 1% THD+N with a 4Ω load. This high power is achieved through careful consideration of necessary thermal design. Failing to optimize thermal design may compromise the LM4853's high power performance and activate unwanted, though necessary, thermal shutdown protection.

The LD package must have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad is connected to a large plane of continuous unbroken copper. This plane forms a thermal mass, heat sink, and radiation area. Place the heat sink area on either outside plane in the case of a two-sided PCB, or on an inner layer of a board with more than two layers. Connect the DAP copper pad to the inner layer or backside copper heat sink area with 4(2x2) vias. The via diameter should be 0.012in-0.013in with a 1.27mm pitch. Ensure efficient thermal conductivity by plating through the vias.

Best thermal performance is achieved with the largest practical heat sink area. If the heatsink and amplifier share the same PCB layer, a nominal $2.5in^2$ area is necessary for 5V operation with a 4Ω load. Heatsink areas not placed on the same PCB layer as the LM4853 should be $5in^2$ (min) for the same supply voltage and load resistance. The last two area recommendations apply for 25°C ambient temperature. Increase the area to compensate for ambient temperatures above 25°C. The LM4853's power de-rating curve in the Typical Performance Characteristics LD Specific Characteristics shows the maximum power dissipation versus temperature. An example PCB layout for the LD package is shown in the Demonstration Board Layout section. For further detailed and specific information concerning PCB layout, fabrication, and mounting an NHE (WSON) package, see TI's AN-1187 Application Report.

## BRIDGE CONFIGURATION EXPLANATION

When the LM4853 is in BTL mode, the output of amplifier A1 serves as the input to amplifier A2, which results in both amplifiers producing signals identical in magnitude, but out of phase by 180°. Consequently, the differential gain for the mono channel is:

$$A_{VD} = V_{OUT} / (V_{INL} + V_{INR}) = 2 \times (R_F / R_I) \quad (1)$$

Driving a load differentially through the BTL OUT- and BTL OUT+ outputs is an amplifier configuration commonly referred to as "bridged mode". Bridged mode operation is different from the classical single-ended amplifier configuration where one side of its load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration. It drives a load differentially, which doubles output swing for a specified supply voltage. This produces four times the output power as that produced by a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive output signal clipping, please refer to the AUDIO POWER AMPLIFIER DESIGN section.

A bridge configuration, such as the one used in LM4853, also creates a second advantage over single-ended amplifiers. Since the differential outputs, BTL OUT- and BTL OUT+, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for the output coupling capacitor that a single supply, single-ended amplifier configuration requires. Eliminating an output coupling capacitor in a single-ended configuration forces the half-supply bias voltage across the load. This increases internal IC power dissipation and may cause permanent loudspeaker damage.

## POWER DISSIPATION

Whether the power amplifier is bridged or single-ended, power dissipation is a major concern when designing the amplifier. Equation 2 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified load.

$$P_{DMAX} = (V_{DD})^2/(2\pi^2 R_L)\text{: Single-Ended} \quad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation.Equation 3 states the maximum power dissipation point for a bridge amplifier operating at the same given conditions.

$$P_{DMAX} = 4 \times (V_{DD})^2/(2\pi^2 R_L)\text{: Bridge Mode} \quad (3)$$

The LM4853 is designed to drive either two single-ended loads simultaneously or one mono bridged-tied load. In SE mode, the maximum internal power dissipation is 2 times that of Equation 2. In BTL mode, the maximum internal power dissipation is the result of Equation 3. Even with this substantial increase in power dissipation, the LM4853 does not require heatsinking. The power dissipation from Equation 3 must not be greater than the power dissipation predicted by Equation 4:

$$P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA} \quad (4)$$

For the package DGS, $\theta_{JA}$ = 194°C/W. $T_{JMAX}$ = 150°C for the LM4853. Depending on the ambient temperature, $T_A$, of the surroundings, Equation 4 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 3 is greater than that of Equation 4, then either the supply voltage must be decreased, the load impedance increased, or the ambient temperature reduced. For the typical application of a 5V power supply, and an 8Ω bridged load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 27°C for package DGS. This assumes the device operates at maximum power dissipation and uses surface mount packaging. Internal power dissipation is a function of output power. If typical operation is not around the maximum power dissipation point, operation at higher ambient temperatures is possible. Refer to the Typical Performance Characteristics curves for power dissipation information for different output power levels.

## POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. The value of the pin bypass capacitor, $C_B$, directly affects the LM4853's half-supply voltage stability and PSRR. The stability and supply rejection increase as the bypass capacitor's value increases Typical applications employ a 5V regulator with a 10µF and a 0.1µF bypass capacitors which aid in supply filtering. This does not eliminate the need for bypassing the supply nodes of the LM4853. The selection of bypass capacitors, especially $C_B$, is thus dependent upon desired PSRR requirements, click and pop performance, system cost, and size constraints.

## SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4853 features amplifier bias circuitry shutdown. This shutdown function is activated by applying a logic high to the SHUTDOWN pin. The trigger point is 2.0V minimum for a logic high level, and 0.8V maximum for a logic low level. It is best to switch between ground and the supply, $V_{DD}$, to ensure correct shutdown operation. By switching the SHUTDOWN pin to $V_{DD}$, the LM4853 supply current draw will be minimized in idle mode. Whereas the device will be disabled with shutdown voltages less than $V_{DD}$, the idle current may be greater than the typical value of 18µA. In either case, the SHUTDOWN pin should be tied to a fixed voltage to avoid unwanted state changes.

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry. This provides a quick, smooth shutdown transition. Another solution is to use a single-pole, single-throw switch in conjunction with an external pull-up resistor. When the switch is closed, the SHUTDOWN pin is connected to ground and enables the amplifier. If the switch is open, the external pull-up resistor, $R_{PU2}$ will disable the LM4853. This scheme ensures that the SHUTDOWN pin will not float, thus preventing unwanted state changes.

## HP-IN FUNCTION

The LM4853 features a headphone control pin, HP-IN, that enables the switching between BTL and SE modes. A logic-low to HP-IN activates the BTL mode, while a logic-high activates the SE mode.

Figure 39 shows the implementation of the LM4853's headphone control. The voltage divider formed by $R_{PU1}$ and $R_{D1}$ sets the voltage at HP-IN to be approximately 50mV with no headphones plugged into the system. This logic-low voltage at the HP-IN pin enables the BTL mode

When a set of headphones is plugged into the system, the headphone jack's contact pin is disconnected from the signal pin. This also interrupts the voltage divider set up by the resistors $R_{PU1}$ and $R_{D1}$. Resistor $R_{PU1}$ applies $V_{DD}$ to the HP-IN pin, switching the LM4853 out of BTL mode and into SE mode. The amplifier then drives the headphones, whose impedance is in parallel with resistors $R_{D1}$ and $R_{D2}$. Resistors $R_{D1}$ and $R_{D2}$ have negligible effect on the output drive capability since the typical impedance of headphones is 32Ω.

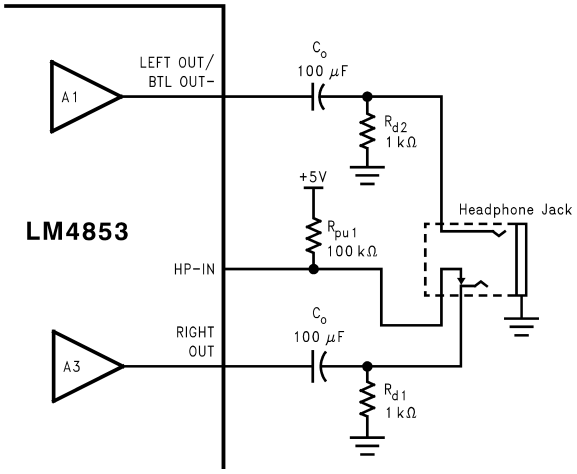



**Figure 39. Headphone Control Circuit**

Also shown in Figure 39 are the electrical connections for the headphone jack and plug. A 3-wire plug consists of a Tip, Ring, and Sleave, where the Tip and Ring are audio signal conductors and the Sleave is the common ground return. One control pin for each headphone jack is sufficient to indicate to the control inputs that a user has inserted a plug into the jack and that the headphone mode of operation is desired.

To ensure smooth transition from BTL to SE operation, it is important to connect HP-IN and $R_{PU1}$ to the control pin on the Right Output of the headphone jack. The control pin on the Left Output of the headphone jack should be left open. Connecting the node between the HP-IN and $R_{PU1}$ to the Left Output control pin may cause unwanted state changes to the HP-IN pin.

## PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical for optimum device and system performance. While the LM4853 is tolerant to a variety of external component combinations, consideration must be given to the external component values that maximize overall system quality.

The LM4853's unity-gain stability allows a designer to maximize system performance. The LM4853's gain should be set no higher than necessary for any given application. A low gain configuration maximizes signal-to-noise performance and minimizes THD+N. However, a low gain configuration also requires large input signals to obtain a given output power. Input signals equal to or greater than $1V_{RMS}$ are available from sources such as audio codecs. Please refer to the section, AUDIO POWER AMPLIFIER DESIGN, for a more complete explanation of proper gain selection.

### Selecting Input and Output Capacitor Values

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in Figure 3. The input coupling capacitor $C_I$ and resistor $R_I$ form a first order high pass filter that limits low frequency response. $C_I$'s value should be based on the desired frequency response weighed against the following: Large value input and output capacitors are both expensive and space consuming for portable designs. Clearly a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Thus, large value input and output capacitors may not increase system performance.

## AUDIO POWER AMPLIFIER DESIGN

### Design a 1W / 8Ω Bridged Audio Amplifier

Given:

- Power Output: $1W_{RMS}$
- Load Impedance 8Ω
- Input Level: $1V_{RMS}$
- Input Impedance: 20kΩ
- Bandwidth: 100Hz - 20kHz ± 0.25dB

A designer must first determine the minimum supply voltage needed to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the Typical Performance Characteristics section, the supply rail can be easily found. A second way to determine the minimum supply rail is to calculate the required $V_{OPEAK}$ using Equation 5 and add the dropout voltage. This results in Equation 6, where $V_{ODTOP}$ and $V_{ODBOT}$ are extrapolated from the Dropout Voltage vs Supply Voltage curve in the Typical Performance Characteristics section.

$$V_{OPEAK} = \sqrt{2 R_L P_O} \quad (5)$$

$$V_{DD} \geq (V_{OPEAK} + (V_{ODTOP} + V_{ODBOT})) \quad (6)$$

Using the Output Power vs Supply Voltage graph for an 8Ω load, the minimum supply rail is 4.7V. But since 5V is a standard supply voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the LM4853 to reproduce peaks in excess of 1W without producing audible distortion. However, the designer must make sure that the chosen power supply voltage and output load does not violate the conditions explained in the POWER DISSIPATION section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 7.

$$A_{VD} \geq \sqrt{P_O R_L} / (V_{IN}) = V_{ORMS}/V_{INRMS} \quad (7)$$

$$R_F / R_I = A_{VD} / 2 \quad (8)$$

From Equation 6, the minimum $A_{VD}$ is 2.83; use $A_{VD} = 3$.

The desired input impedance was 20kΩ, and with an $A_{VD}$ of 3, using Equation 8 results in an allocation of $R_I$ = 20kΩ and $R_F$ = 30kΩ.

The final design step is to set the amplifier's −3dB frequency bandwidth. To achieve the desired ± 0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one−fifth the lower bandwidth limit and the high frequency response must extend o at least five times the upper bandwidth limit. The variation for both response limits is 0.17dB, well within the ± 0.25dB desired limit. This results in:

$$f_L = 100Hz / 5 = 20Hz \quad (9)$$

$$f_H = 20kHz \times 5 = 100kHz \quad (10)$$

As stated in the External Components Description section, $R_I$ in conjunction with $C_I$ create a highpass filter. Find the coupling capacitor's value using Equation 11.

$$C_I \geq 1 / (2\pi R_I f_L) \quad (11)$$

$$C_I \geq 1 / ( 2\pi \times 20k\Omega \times 20Hz) = 0.397\mu F \quad (12)$$

Use a 0.39µF capacitor, the closest standard value.

The high frequency pole is determined by the product of the desired high frequency pole, $f_H$, and the differential gain, $A_{VD}$. With $A_{VD}$ = 3 and $f_H$ = 100kHz, the resulting GBWP = 150kHz which is much smaller than the LM4853 GBWP of 10MHz. This difference indicates that a designer can still use the LM4853 at higher differential gains without bandwidth limitations.

## PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 3Ω AND 4Ω LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependant on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by a 4Ω load from 2.0W to 1.95W. This problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

### Demonstration Board Layout

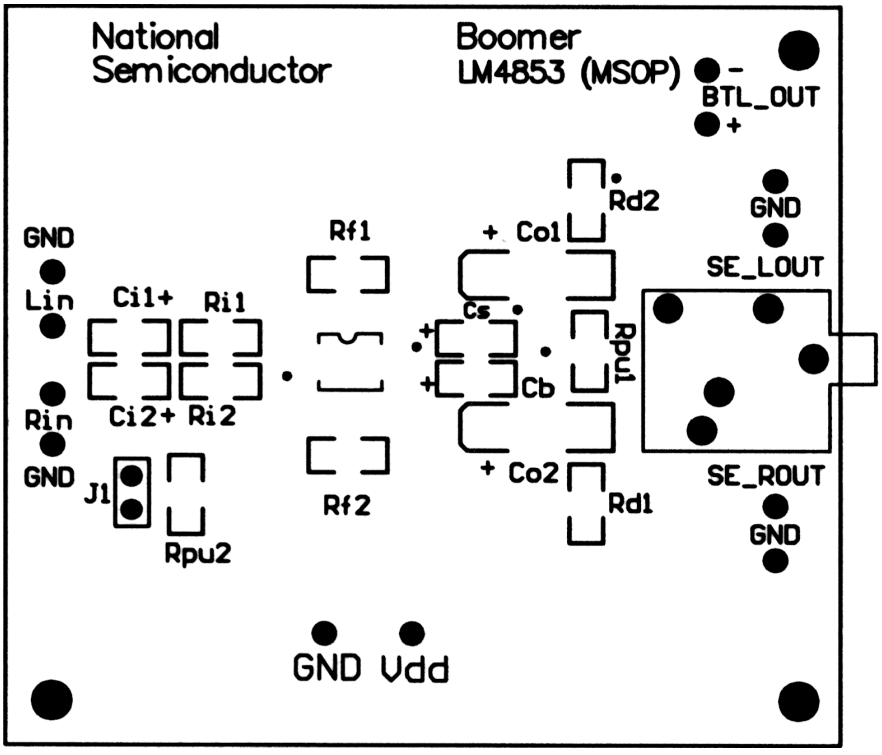



**Figure 40. Recommended MM PC Board Layout: Component-Side SilkScreen**

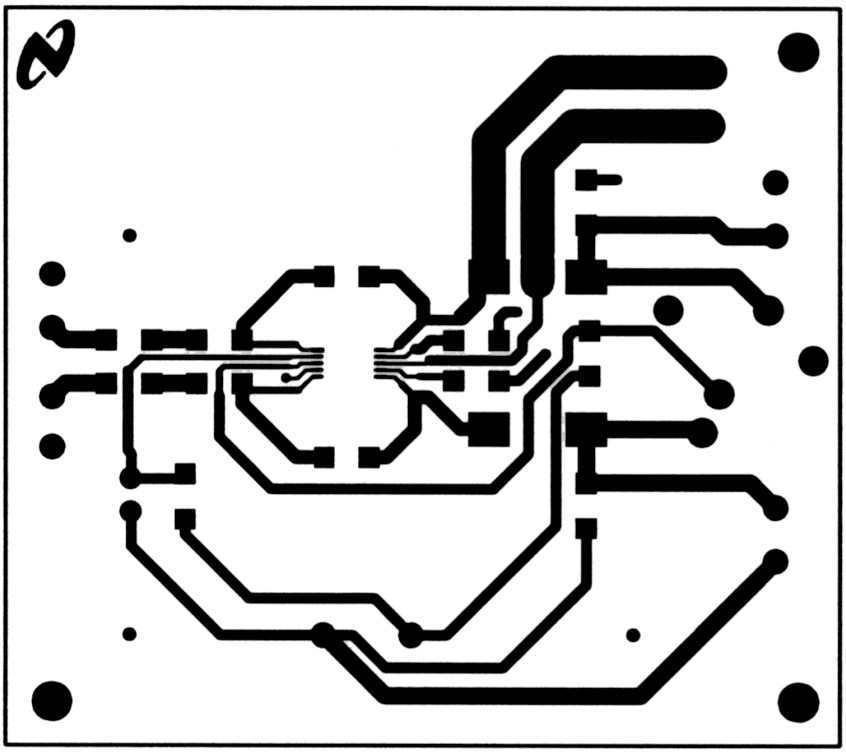


**Figure 41. Recommended MM PC Board Layout: Component-Side Layout**

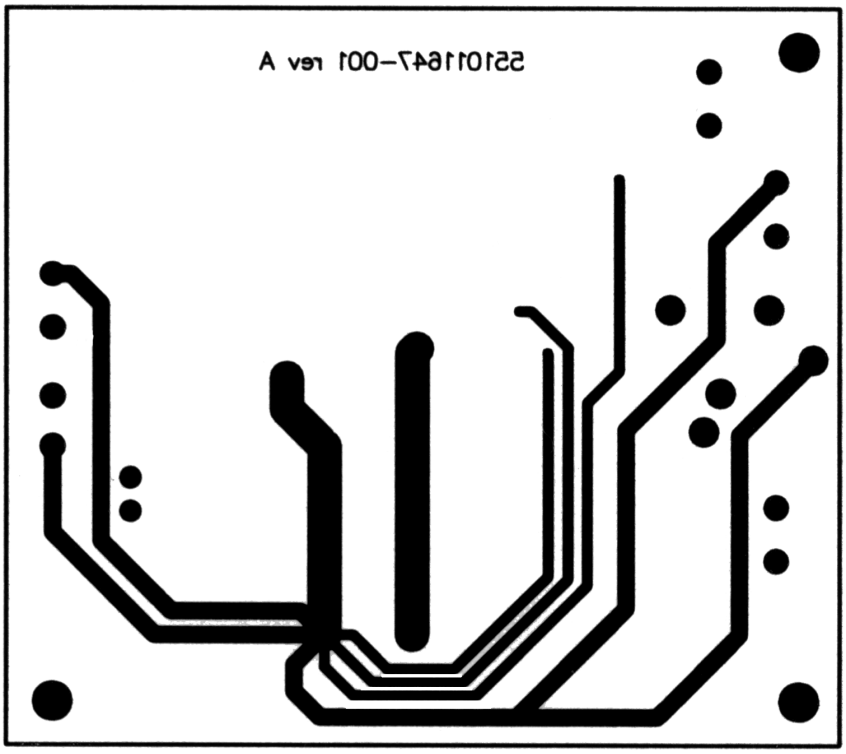



**Figure 42. Recommended MM PC Board Layout: Bottom-Side Layout**

## REVISION HISTORY

| Changes from Revision D (May 2013) to Revision E | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 17 |

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LM4853LD/NOPB | Active | Production | WSON (NHE) \| 14 | 1000 \| LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | L4853LD |
| LM4853LD/NOPB.A | Active | Production | WSON (NHE) \| 14 | 1000 \| LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | L4853LD |
| LM4853MM/NOPB | Active | Production | VSSOP (DGS) \| 10 | 1000 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | G53 |
| LM4853MM/NOPB.A | Active | Production | VSSOP (DGS) \| 10 | 1000 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | G53 |
| LM4853MMX/NOPB | Active | Production | VSSOP (DGS) \| 10 | 3500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | G53 |
| LM4853MMX/NOPB.A | Active | Production | VSSOP (DGS) \| 10 | 3500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | G53 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

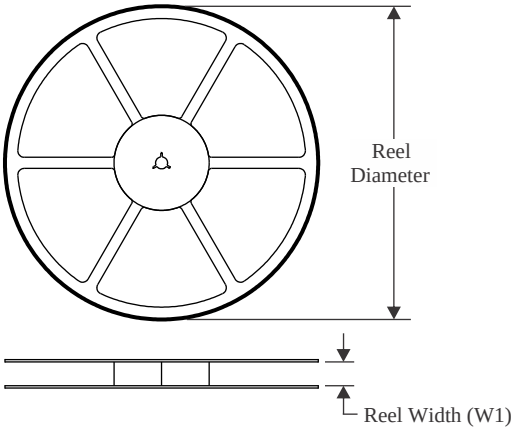
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

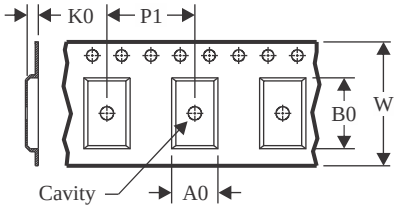
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

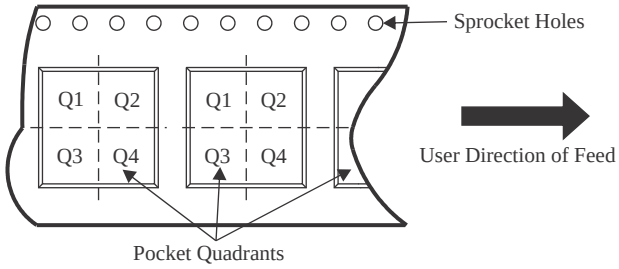



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

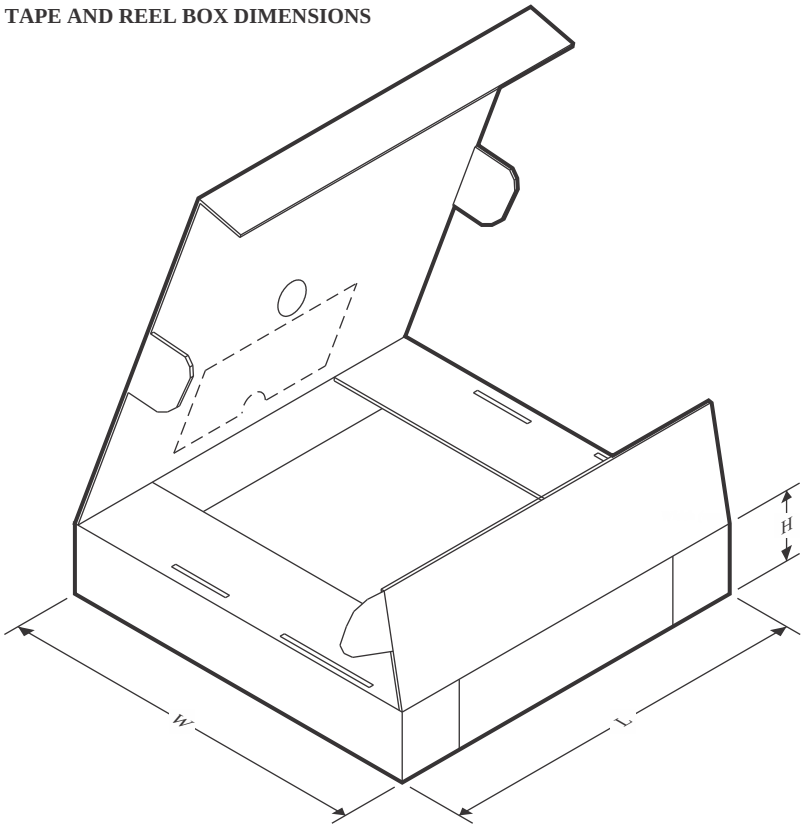
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM4853LD/NOPB | WSON | NHE | 14 | 1000 | 177.8 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LM4853MM/NOPB | VSSOP | DGS | 10 | 1000 | 177.8 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LM4853MMX/NOPB | VSSOP | DGS | 10 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

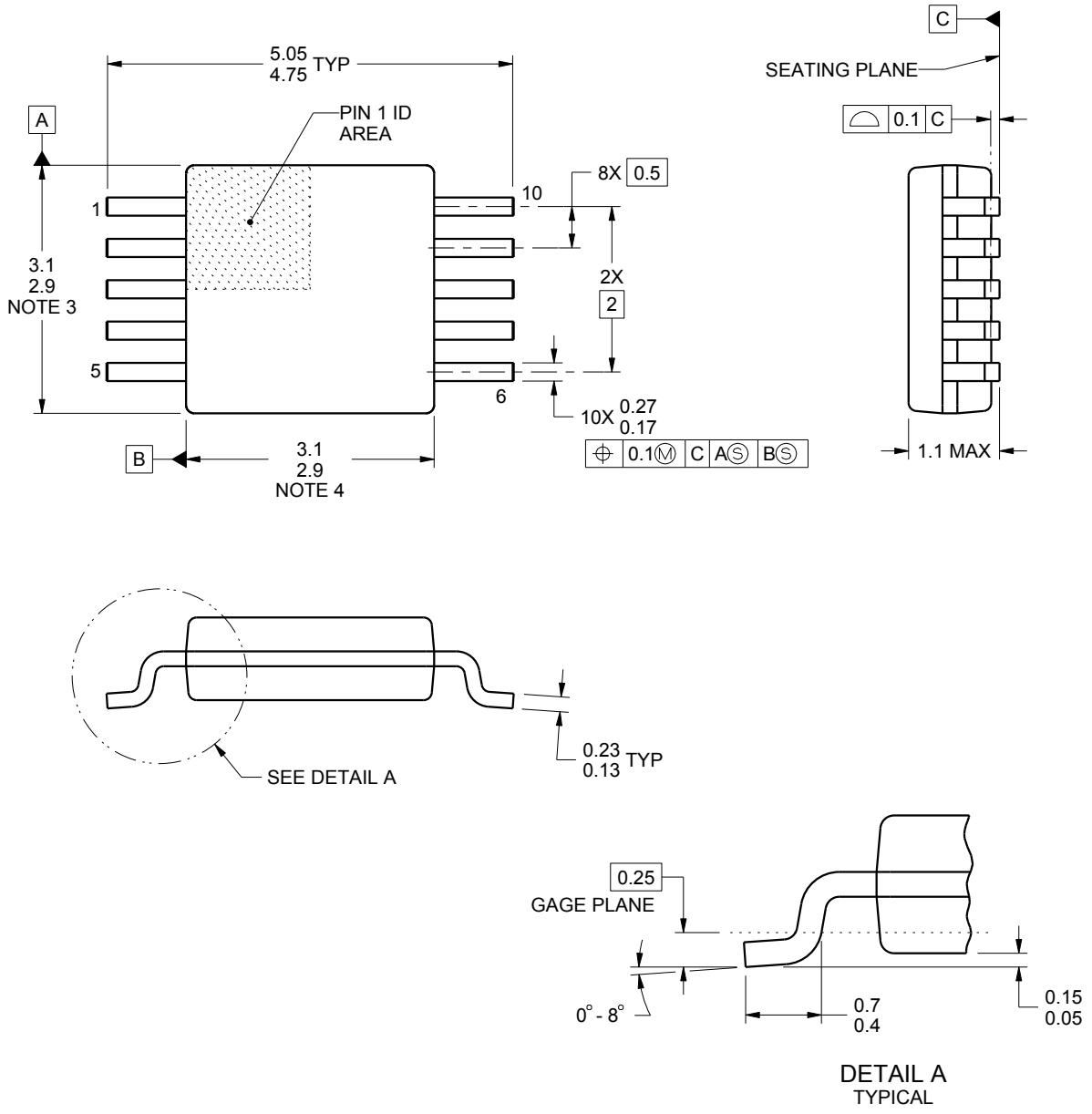
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM4853LD/NOPB | WSON | NHE | 14 | 1000 | 208.0 | 191.0 | 35.0 |
| LM4853MM/NOPB | VSSOP | DGS | 10 | 1000 | 208.0 | 191.0 | 35.0 |
| LM4853MMX/NOPB | VSSOP | DGS | 10 | 3500 | 367.0 | 367.0 | 35.0 |

# PACKAGE OUTLINE

## DGS0010A

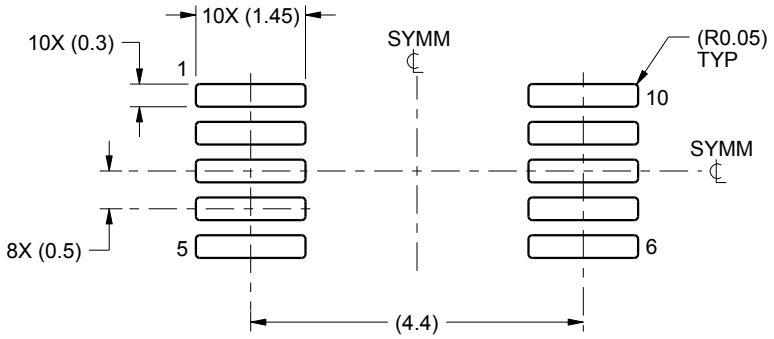
## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

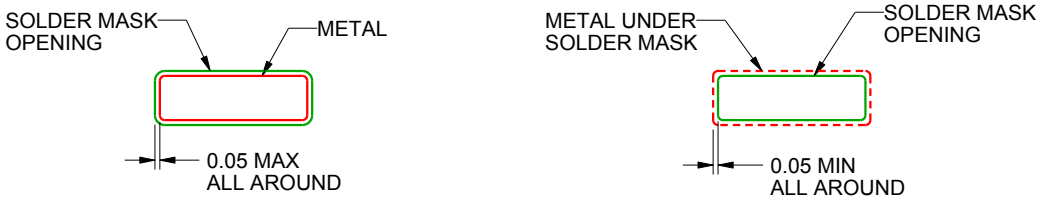



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.




LAND PATTERN EXAMPLE
SCALE:10X




SOLDER MASK DETAILS
NOT TO SCALE

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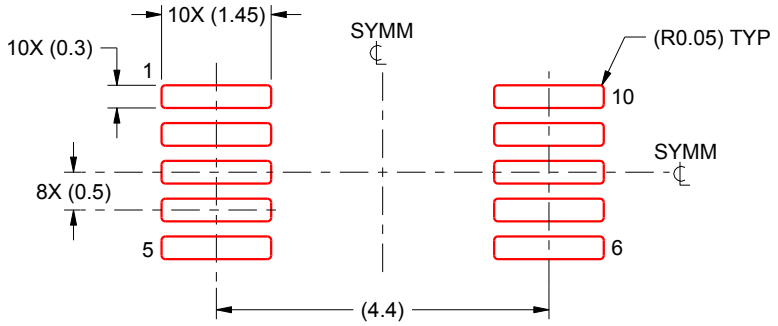
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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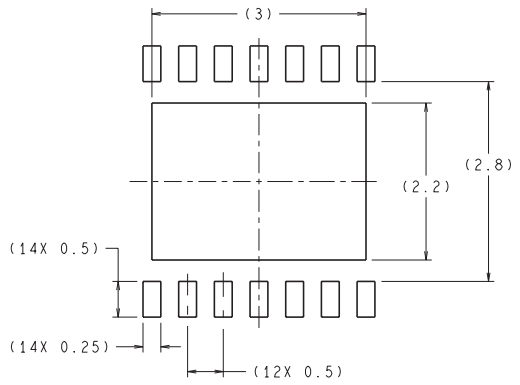
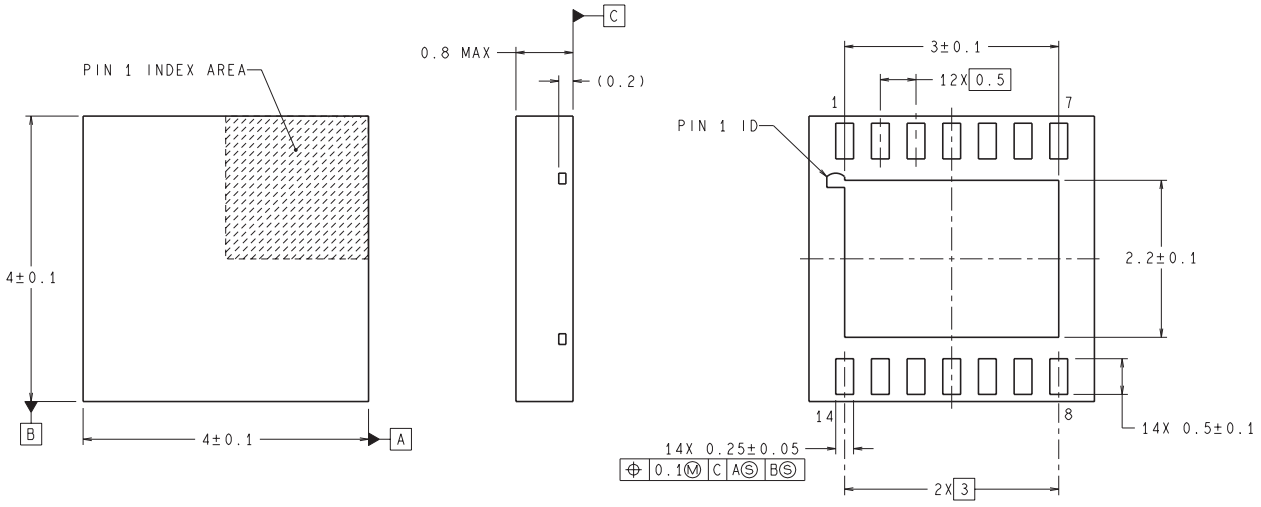



RECOMMENDED LAND PATTERN
1:1 RATION WITH PKG SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS




LDA14A (REV A)

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