

## 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 ANALOG INPUTS

### FEATURES

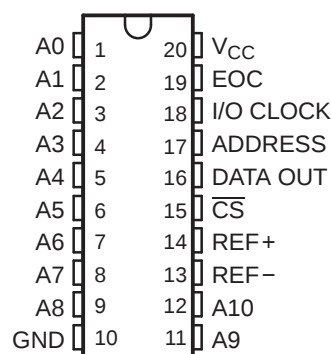
- 10-Bit Resolution A/D Converter
- 11 Analog Input Channels
- Three Built-In Self-Test Modes
- Inherent Sample-and-Hold Function
- Total Unadjusted Error:  $\pm 1\text{LSB}$  Max
- On-Chip System Clock
- End-of-Conversion (EOC) Output
- Terminal Compatible With TLC542
- CMOS Technology

### DESCRIPTION

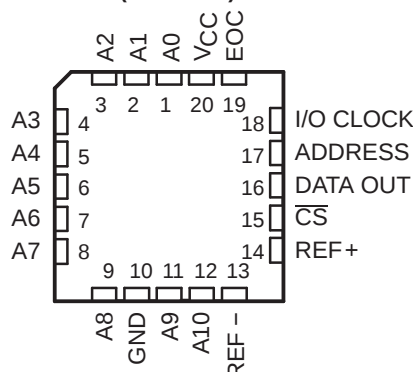
The TLC1542C, TLC1542I, TLC1542M, TLC1542Q, TLC1543C, TLC1543I, and TLC1543Q are CMOS 10-bit switched-capacitor successive-approximation analog-to-digital converters. These devices have three inputs and a 3-state output [chip select ( $\overline{\text{CS}}$ ), input-output clock (I/O CLOCK), address input (ADDRESS), and data output (DATA OUT)] that provide a direct 4-wire interface to the serial port of a host processor. These devices allow high-speed data transfers from the host.

In addition to a high-speed A/D converter and versatile control capability, these devices have an on-chip 14-channel multiplexer that can select any one of 11 analog inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic. At the end of A/D conversion, the end-of-conversion (EOC) output goes high to indicate that conversion is complete. The converter incorporated in the devices features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating free-air temperature range.

DB, DW, J, OR N PACKAGE  
(TOP VIEW)



FK OR FN PACKAGE  
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

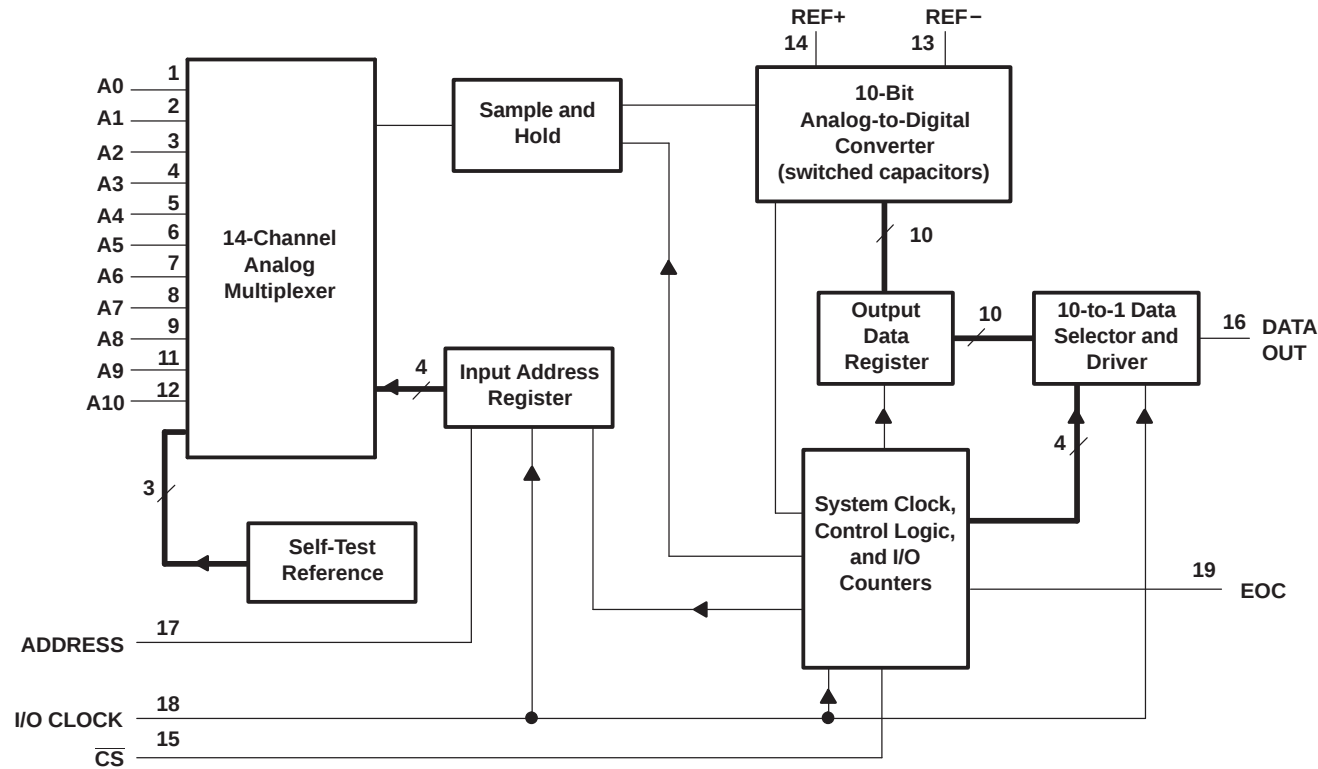


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

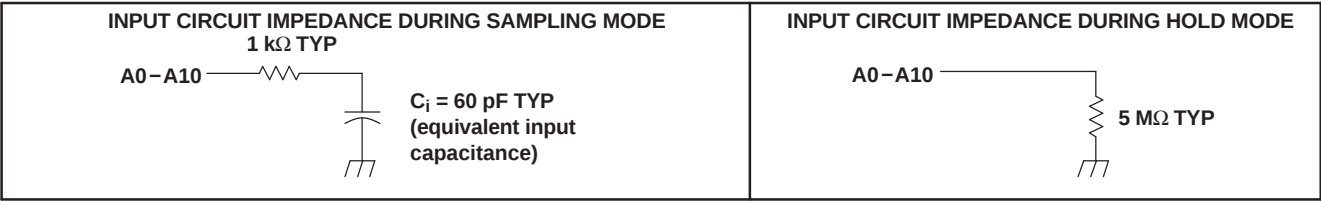
**AVAILABLE OPTIONS**

| T <sub>A</sub> | PACKAGE            |                    |                   |                 |                   |                 |
|----------------|--------------------|--------------------|-------------------|-----------------|-------------------|-----------------|
|                | SMALL OUTLINE (DB) | SMALL OUTLINE (DW) | CHIP CARRIER (FN) | PLASTIC DIP (N) | CHIP CARRIER (FK) | CERAMIC DIP (J) |
| 0°C to 70°C    |                    | TLC1542CDW         | TLC1542CFN        | TLC1542CN       |                   |                 |
|                | TLC1543CDB         | TLC1543CDW         | TLC1543CFN        | TLC1543CN       |                   |                 |
| -40°C to 85°C  |                    | TLC1542IDW         | TLC1542IFN        | TLC1542IN       |                   |                 |
|                | TLC1543IDB         | TLC1543IDW         | TLC1543IFN        | TLC1543IN       |                   |                 |
| -40°C to 125°C |                    |                    | TLC1542QFN        |                 |                   |                 |
|                | TLC1543QDB         | TLC1543QDW         | TLC1543QFN        |                 |                   |                 |
| -55°C to 125°C |                    |                    |                   |                 | TLC1542MFK        | TLC1542MJ       |

**FUNCTIONAL BLOCK DIAGRAM**



**TYPICAL EQUIVALENT INPUTS**



**TERMINAL FUNCTIONS**

| TERMINAL<br>NAME NO. |             | I/O | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|----------------------|-------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ADDRESS              | 17          | I   | Serial address input. A 4-bit serial address selects the desired analog input or test voltage that is to be converted next. The address data is presented with the MSB first and shifts in on the first four rising edges of I/O CLOCK. After the four address bits have been read into the address register, this input is ignored for the remainder of the current conversion period.                                                                                                                                                                                                                                                                                                                                                                                      |
| A0-A10               | 1-9, 11, 12 | I   | Analog signal inputs. The 11 analog inputs are applied to these terminals and are internally multiplexed. The driving source impedance should be less than or equal to 1 k $\Omega$ .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| $\overline{CS}$      | 15          | I   | Chip select. A high-to-low transition on this input resets the internal counters and controls and enables DATA OUT, ADDRESS, and I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock. A low-to-high transition disables ADDRESS and I/O CLOCK within a setup time plus two falling edges of the internal system clock.                                                                                                                                                                                                                                                                                                                                                                                                            |
| DATA OUT             | 16          | O   | The 3-state serial output for the A/D conversion result. This output is in the high-impedance state when $\overline{CS}$ is high and active when $\overline{CS}$ is low. With a valid chip select, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB value of the previous conversion result. The next falling edge of I/O CLOCK drives this output to the logic level corresponding to the next most significant bit, and the remaining bits shift out in order with the LSB appearing on the ninth falling edge of I/O CLOCK. On the tenth falling edge of I/O CLOCK, DATA OUT is driven to a low logic level so that serial interface data transfers of more than ten clocks produce zeroes as the unused LSBs. |
| EOC                  | 19          | O   | End of conversion. This output goes from a high to a low logic level on the trailing edge of the tenth I/O CLOCK and remains low until the conversion is complete and data are ready for transfer.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| GND                  | 10          | I   | The ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to this terminal.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| I/O CLOCK            | 18          | I   | Input/output clock. This terminal receives the serial I/O CLOCK input and performs the following four functions: 1) It clocks the four input address bits into the address register on the first four rising edges of the I/O CLOCK with the multiplex address available after the fourth rising edge. 2) On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplex input begins charging the capacitor array and continues to do so until the tenth falling edge of I/O CLOCK. 3) It shifts the nine remaining bits of the previous conversion data out on DATA OUT. 4) It transfers control of the conversion to the internal state controller on the falling edge of the tenth clock.                                                   |
| REF+                 | 14          | I   | The upper reference voltage value (nominally $V_{CC}$ ) is applied to this terminal. The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the voltage applied to the REF- terminal.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| REF-                 | 13          | I   | The lower reference voltage value (nominally ground) is applied to this terminal.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| $V_{CC}$             | 20          | I   | Positive supply voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

**DETAILED DESCRIPTION**

With chip select ( $\overline{CS}$ ) inactive (high), the ADDRESS and I/O CLOCK inputs are initially disabled and DATA OUT is in the high-impedance state. When the serial interface takes  $\overline{CS}$  active (low), the conversion sequence begins with the enabling of I/O CLOCK and ADDRESS and the removal of DATA OUT from the high-impedance state. The serial interface then provides the 4-bit channel address to ADDRESS and the I/O CLOCK sequence to I/O CLOCK. During this transfer, the serial interface also receives the previous conversion result from DATA OUT. I/O CLOCK receives an input sequence that is between 10 and 16 clocks long from the host serial interface. The first four I/O clocks load the address register with the 4-bit address on ADDRESS, selecting the desired analog channel, and the next six clocks providing the control timing for sampling the analog input.

There are six basic serial-interface timing modes that can be used with the device. These modes are determined by the speed of I/O CLOCK and the operation of  $\overline{CS}$  as shown in Table 1. These modes are (1) a fast mode with a 10-clock transfer and  $\overline{CS}$  inactive (high) between conversion cycles, (2) a fast mode with a 10-clock transfer and  $\overline{CS}$  active (low) continuously, (3) a fast mode with an 11- to 16-clock transfer and  $\overline{CS}$  inactive (high) between conversion cycles, (4) a fast mode with a 16-clock transfer and  $\overline{CS}$  active (low) continuously, (5) a slow mode with an 11- to 16-clock transfer and  $\overline{CS}$  inactive (high) between conversion cycles, and (6) a slow mode with a 16-clock transfer and  $\overline{CS}$  active (low) continuously.

The MSB of the previous conversion appears at DATA OUT on the falling edge of  $\overline{CS}$  in mode 1, mode 3, and mode 5, on the rising edge of EOC in mode 2 and mode 4, and following the sixteenth clock falling edge in mode 6. The remaining nine bits are shifted out on the next nine falling edges of I/O CLOCK. Ten bits of data are transmitted to the host-serial interface through DATA OUT. The number of serial clock pulses used also depends on the mode of operation, but a minimum of ten clock pulses is required for conversion to begin. On the tenth clock falling edge, the EOC output goes low and returns to the high logic level when conversion is complete and the result can be read by the host. Also, on the tenth clock falling edge, the internal logic takes DATA OUT low to ensure that the remaining bit values are zero when the I/O CLOCK transfer is more than ten clocks long.

Table 1 lists the operational modes with respect to the state of  $\overline{CS}$ , the number of I/O serial transfer clocks that can be used, and the timing edge on which the MSB of the previous conversion appears at the output.

**Table 1. MODE OPERATION**

| MODES      |        | $\overline{CS}$                | NO. OF I/O CLOCK        | MSB AT DATA OUT <sup>(1)</sup> | TIMING DIAGRAM |
|------------|--------|--------------------------------|-------------------------|--------------------------------|----------------|
| Fast Modes | Mode 1 | High between conversion cycles | 10                      | $\overline{CS}$ falling edge   | Figure 9       |
|            | Mode 2 | Low continuously               | 10                      | EOC rising edge                | Figure 10      |
|            | Mode 3 | High between conversion cycles | 11 TO 16 <sup>(2)</sup> | $\overline{CS}$ falling edge   | Figure 11      |
|            | Mode 4 | Low continuously               | 16 <sup>(2)</sup>       | EOC rising edge                | Figure 12      |
| Slow Modes | Mode 5 | High between conversion cycles | 11 to 16 <sup>(3)</sup> | $\overline{CS}$ falling edge   | Figure 13      |
|            | Mode 6 | Low continuously               | 16 <sup>(3)</sup>       | 16th clock falling edge        | Figure 14      |

(1) These edges also initiate serial-interface communication.

(2) No more than 16 clocks should be used.

(3) No more than 16 clocks should be used.

## FAST MODES

The device is in a fast mode when the serial I/O CLOCK data transfer is completed before the conversion is completed. With a 10-clock serial transfer, the device can only run in a fast mode since a conversion does not begin until the falling edge of the tenth I/O CLOCK.

### **MODE 1: FAST MODE, $\overline{CS}$ INACTIVE (HIGH) BETWEEN CONVERSION CYCLES, 10-CLOCK TRANSFER**

In this mode,  $\overline{CS}$  is inactive (high) between serial I/O CLOCK transfers and each transfer is ten clocks long. The falling edge of  $\overline{CS}$  begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of  $\overline{CS}$  ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of  $\overline{CS}$  disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

### **MODE 2: FAST MODE, $\overline{CS}$ ACTIVE (LOW) CONTINUOUSLY, 10-CLOCK TRANSFER**

In this mode,  $\overline{CS}$  is active (low) between serial I/O CLOCK transfers and each transfer is ten clocks long. After the initial conversion cycle,  $\overline{CS}$  is held active (low) for subsequent conversions; the rising edge of EOC then begins each sequence by removing DATA OUT from the low logic level, allowing the MSB of the previous conversion to appear immediately on this output.

### **MODE 3: FAST MODE, $\overline{CS}$ INACTIVE (HIGH) BETWEEN CONVERSION CYCLES, 11- to 16-CLOCK TRANSFER**

In this mode,  $\overline{CS}$  is inactive (high) between serial I/O CLOCK transfers, and each transfer can be 11 to 16 clocks long. The falling edge of  $\overline{CS}$  begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of  $\overline{CS}$  ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of  $\overline{CS}$  disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

#### **MODE 4: FAST MODE, $\overline{CS}$ ACTIVE (LOW) CONTINUOUSLY, 16-CLOCK TRANSFER**

In this mode,  $\overline{CS}$  is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle,  $\overline{CS}$  is held active (low) for subsequent conversions; the rising edge of EOC then begins each sequence by removing DATA OUT from the low logic level, allowing the MSB of the previous conversion to appear immediately on this output.

#### **SLOW MODES**

In a slow mode, the conversion is completed before the serial I/O CLOCK data transfer is completed. A slow mode requires a minimum 11-clock transfer into I/O CLOCK, and the rising edge of the eleventh clock must occur before the conversion period is complete; otherwise, the device loses synchronization with the host-serial interface and  $\overline{CS}$  has to be toggled to initialize the system. The eleventh rising edge of the I/O CLOCK must occur within 9.5  $\mu$ s after the tenth I/O clock falling edge.

#### **MODE 5: SLOW MODE, $\overline{CS}$ INACTIVE (HIGH) BETWEEN CONVERSION CYCLES, 11- to 16-CLOCK TRANSFER**

In this mode,  $\overline{CS}$  is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of  $\overline{CS}$  begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of  $\overline{CS}$  ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of  $\overline{CS}$  disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

#### **MODE 6: SLOW MODE, $\overline{CS}$ ACTIVE (LOW) CONTINUOUSLY, 16-CLOCK TRANSFER**

In this mode,  $\overline{CS}$  is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle,  $\overline{CS}$  is held active (low) for subsequent conversions. The falling edge of the sixteenth I/O CLOCK then begins each sequence by removing DATA OUT from the low state, allowing the MSB of the previous conversion to appear immediately at DATA OUT. The device is then ready for the next 16-clock transfer initiated by the serial interface.

#### **ADDRESS BITS**

The 4-bit analog channel-select address for the next conversion cycle is presented to the ADDRESS terminal (MSB first) and is clocked into the address register on the first four leading edges of I/O CLOCK. This address selects one of 14 inputs (11 analog inputs or three internal test inputs).

#### **ANALOG INPUTS AND TEST MODES**

The 11 analog inputs and the three internal test inputs are selected by the 14-channel multiplexer according to the input address as shown in Tables 2 and 3. The input multiplexer is a break-before-make type to reduce input-to-input noise injection resulting from channel switching.

Sampling of the analog input starts on the falling edge of the fourth I/O CLOCK, and sampling continues for six I/O CLOCK periods. The sample is held on the falling edge of the tenth I/O CLOCK. The three test inputs are applied to the multiplexer, sampled, and converted in the same manner as the external analog inputs.

**Table 2. ANALOG-CHANNEL-SELECT ADDRESS**

| ANALOG INPUT SELECTED | VALUE SHIFTED INTO ADDRESS INPUT |     |
|-----------------------|----------------------------------|-----|
|                       | BINARY                           | HEX |
| A0                    | 0000                             | 0   |
| A1                    | 0001                             | 1   |
| A2                    | 0010                             | 2   |
| A3                    | 0011                             | 3   |
| A4                    | 0100                             | 4   |
| A5                    | 0101                             | 5   |
| A6                    | 0110                             | 6   |
| A7                    | 0111                             | 7   |
| A8                    | 1000                             | 8   |
| A9                    | 1001                             | 9   |
| A10                   | 1010                             | A   |

**Table 3. TEST-MODE-SELECT ADDRESS**

| INTERNAL SELF-TEST VOLTAGE SELECTED <sup>(1)</sup> | VALUE SHIFTED INTO ADDRESS INPUT |     | OUTPUT RESULT (HEX) <sup>(2)</sup> |
|----------------------------------------------------|----------------------------------|-----|------------------------------------|
|                                                    | BINARY                           | HEX |                                    |
| $\frac{V_{\text{ref+}} - V_{\text{ref-}}}{2}$      | 1011                             | B   | 200                                |
| $V_{\text{ref-}}$                                  | 1100                             | C   | 000                                |
| $V_{\text{ref+}}$                                  | 1101                             | D   | 3FF                                |

(1)  $V_{\text{ref+}}$  is the voltage applied to the REF+ input, and  $V_{\text{ref-}}$  is the voltage applied to the REF- input.

(2) The output results shown are the ideal values and vary with the reference stability and with internal offsets.

## CONVERTER AND ANALOG INPUT

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the  $S_C$  switch and all  $S_T$  switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all  $S_T$  and  $S_C$  switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF-) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF-. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half  $V_{CC}$ ), a 0 bit is placed in the output register and the 512-weight capacitor is switched to REF-. If the voltage at the summing node is less than the trip point of the threshold detector, a 1 bit is placed in the register and the 512-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are counted.

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to count and weigh the bits from MSB to LSB.

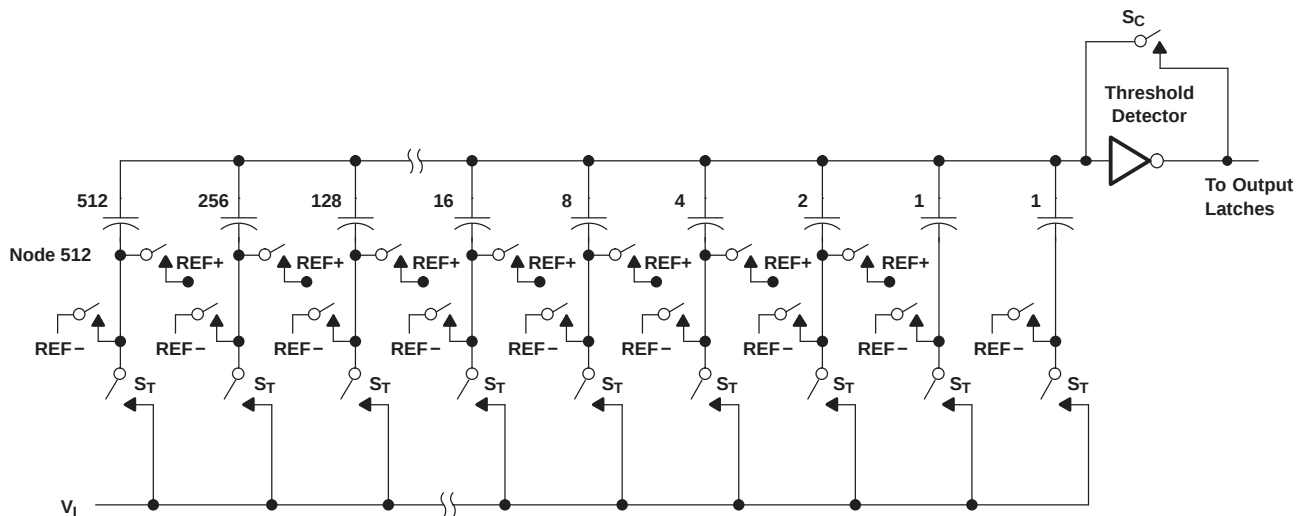


Figure 1. Simplified Model of the Successive-Approximation System

## CHIP-SELECT OPERATION

The trailing edge of  $\overline{CS}$  starts all modes of operation, and  $\overline{CS}$  can abort a conversion sequence in any mode. A high-to-low transition on  $\overline{CS}$  within the specified time during an ongoing cycle aborts the cycle, and the device returns to the initial state (the contents of the output data register remain at the previous conversion result). Exercise care to prevent  $\overline{CS}$  from being taken low close to completion of conversion because the output data can be corrupted.

## REFERENCE VOLTAGE INPUTS

There are two reference inputs used with the device: REF+ and REF-. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero reading respectively. The values of REF+, REF-, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ and at zero when the input signal is equal to or lower than REF-.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                    |                                                                  | UNIT                                 |
|--------------------|------------------------------------------------------------------|--------------------------------------|
| $V_{CC}$ , see (2) | Supply voltage range                                             | -0.5 V to 6.5 V                      |
| $V_I$              | Input voltage range                                              | -0.3 V to $V_{CC} + 0.3$ V           |
| $V_O$              | Output voltage range                                             | -0.3 V to $V_{CC} + 0.3$ V           |
| $V_{ref+}$         | Positive reference voltage                                       | $V_{CC} + 0.1$ V                     |
| $V_{ref-}$         | Negative reference voltage                                       | -0.1 V                               |
|                    | Peak input current (any input)                                   | ±20 mA                               |
|                    | Peak total input current (all inputs)                            | ±30 mA                               |
| $T_A$              | Operating free-air temperature range                             | TLC1542C, TLC1543C<br>0°C to 70°C    |
|                    |                                                                  | TLC1542I, TLC1543I<br>-40°C to 85°C  |
|                    |                                                                  | TLC1542Q, TLC1543Q<br>-40°C to 125°C |
|                    |                                                                  | TLC1542M<br>-55°C to 125°C           |
| $T_{stg}$          | Storage temperature range,                                       | -65°C to 150°C                       |
|                    | Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds | 260°C                                |

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to digital ground with REF- and GND wired together (unless otherwise noted).

## RECOMMENDED OPERATING CONDITIONS

|                                     |                                                                      |                           | MIN   | NOM      | MAX            | UNIT |
|-------------------------------------|----------------------------------------------------------------------|---------------------------|-------|----------|----------------|------|
| $V_{CC}$                            | Supply voltage                                                       |                           | 4.5   | 5        | 5.5            | V    |
| $V_{ref+}$ , see (1)                | Positive reference voltage                                           |                           |       | $V_{CC}$ |                | V    |
| $V_{ref-}$ , see (1)                | Negative reference voltage                                           |                           |       | 0        |                | V    |
| $V_{ref+} - V_{ref-}$ , see (1)     | Differential reference voltage                                       |                           | 2.5   | $V_{CC}$ | $V_{CC} + 0.2$ | V    |
|                                     | Analog input voltage, see (1)                                        |                           | 0     |          | $V_{CC}$       | V    |
| $V_{IH}$                            | High-level control input voltage                                     | $V_{CC} = 4.5$ V to 5.5 V | 2     |          |                | V    |
| $V_{IL}$                            | Low-level control input voltage                                      | $V_{CC} = 4.5$ V to 5.5 V |       |          | 0.8            | V    |
| $t_{su(A)}$ , see Figure 4          | Setup time, address bits at data input before I/O CLOCK↑             |                           | 100   |          |                | ns   |
| $t_{h(A)}$ , see Figure 4           | Hold time, address bits after I/O CLOCK↑                             |                           | 0     |          |                | ns   |
| $t_{h(CS)}$ , see Figure 5          | Hold time, $\overline{CS}$ low after last I/O CLOCK↓                 |                           | 0     |          |                | ns   |
| $t_{su(CS)}$ , see (2) and Figure 5 | Setup time, $\overline{CS}$ low before clocking in first address bit |                           | 1.425 |          |                | μs   |
|                                     | Clock frequency at I/O CLOCK, see (3)                                |                           | 0     |          | 2.1            | MHz  |
| $t_{WH(I/O)}$                       | Pulse duration, I/O CLOCK high,                                      |                           | 190   |          |                | ns   |
| $t_{WL(I/O)}$                       | Pulse duration, I/O CLOCK low,                                       |                           | 190   |          |                | ns   |
| $t_{l(I/O)}$ , see (4) and Figure 6 | Transition time, I/O CLOCK,                                          |                           |       |          | 1              | μs   |
| $t_{l(CS)}$                         | Transition time, ADDRESS and $\overline{CS}$ ,                       |                           |       |          | 10             | μs   |

- (1) Analog input voltages greater than that applied to REF+ convert as all ones (111111111), while input voltages less than that applied to REF- convert as all zeros (000000000). The device is functional with reference voltages down to 1 V ( $V_{ref+} - V_{ref-}$ ); however, the electrical specifications are no longer applicable.
- (2) To minimize errors caused by noise at  $\overline{CS}$ , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after  $\overline{CS}$ ↓ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum  $\overline{CS}$  setup time has elapsed.
- (3) For 11- to 16-bit transfers, after the tenth I/O CLOCK falling edge ( $\leq 2$  V) at least 1 I/O CLOCK rising edge ( $\geq 2$  V) must occur within 9.5 μs.
- (4) This is the time required for the clock input signal to fall from  $V_{IHmin}$  to  $V_{ILmax}$  or to rise from  $V_{ILmax}$  to  $V_{IHmin}$ . In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 μs for remote data-acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

**RECOMMENDED OPERATING CONDITIONS (continued)**

|       |                                 |                    | MIN | NOM | MAX | UNIT |
|-------|---------------------------------|--------------------|-----|-----|-----|------|
| $T_A$ | Operating free-air temperature, | TLC1542C, TLC1543C | 0   |     | 70  | °C   |
|       |                                 | TLC1542I, TLC1543I | -40 |     | 85  |      |
|       |                                 | TLC1542Q, TLC1543Q | -40 |     | 125 |      |
|       |                                 | TLC1542M           | -55 |     | 125 |      |

**ELECTRICAL CHARACTERISTICS**

over recommended operating free-air temperature range,  $V_{CC} = V_{ref+} = 4.5\text{ V to }5.5\text{ V}$ , I/O CLOCK frequency = 2.1 MHz (unless otherwise noted)

| PARAMETER                                         |                                                             | TEST CONDITIONS                                                |                                           | MIN | TYP <sup>(1)</sup> | MAX                  | UNIT |
|---------------------------------------------------|-------------------------------------------------------------|----------------------------------------------------------------|-------------------------------------------|-----|--------------------|----------------------|------|
| V <sub>OH</sub>                                   | High-level output voltage                                   | V <sub>CC</sub> = 4.5 V,                                       | I <sub>OH</sub> = -1.6 mA                 | 2.4 |                    | V <sub>CC</sub> -0.1 | V    |
|                                                   |                                                             | V <sub>CC</sub> = 4.5 V to 5.5 V,                              | I <sub>OH</sub> = -20 μA                  |     |                    |                      |      |
| V <sub>OL</sub>                                   | Low-level output voltage                                    | V <sub>CC</sub> = 4.5 V,                                       | I <sub>OL</sub> = 1.6 mA                  |     |                    | 0.4                  | V    |
|                                                   |                                                             | V <sub>CC</sub> = 4.5 V to 5.5 V,                              | I <sub>OL</sub> = 20 μA                   |     |                    | 0.1                  |      |
| I <sub>OZ</sub>                                   | Off-state (high-impedance-state) output current             | V <sub>O</sub> = V <sub>CC</sub> ,                             | $\overline{\text{CS}}$ at V <sub>CC</sub> |     |                    | 10                   | μA   |
|                                                   |                                                             | V <sub>O</sub> = 0,                                            | $\overline{\text{CS}}$ at V <sub>CC</sub> |     |                    | -10                  |      |
| I <sub>IH</sub>                                   | High-level input current                                    | V <sub>I</sub> = V <sub>CC</sub>                               |                                           |     | 0.005              | 2.5                  | μA   |
| I <sub>IL</sub>                                   | Low-level input current                                     | V <sub>I</sub> = 0                                             |                                           |     | 0.005              | -2.5                 | μA   |
| I <sub>CC</sub>                                   | Operating supply current                                    | $\overline{\text{CS}}$ at 0 V                                  |                                           |     | 0.8                | 2.5                  | mA   |
|                                                   | Selected channel leakage current TLC1542/TLC1543 C, I, or Q | Selected channel at V <sub>CC</sub> ,                          | Unselected channel at 0 V                 |     |                    | 1                    | μA   |
|                                                   |                                                             | Selected channel at 0 V,                                       | Unselected channel at V <sub>CC</sub>     |     |                    | -1                   |      |
|                                                   | Selected channel leakage current TLC1542M                   | Selected channel at V <sub>CC</sub> ,<br>T <sub>A</sub> = 25°C | Unselected channel at 0 V,                |     |                    | 1                    | μA   |
|                                                   |                                                             | Selected channel at 0 V,<br>T <sub>A</sub> = 25°C              | Unselected channel at V <sub>CC</sub> ,   |     |                    | -1                   |      |
|                                                   |                                                             | Selected channel at V <sub>CC</sub> ,                          | Unselected channel at 0 V                 |     |                    | 2.5                  |      |
|                                                   |                                                             | Selected channel at 0 V,                                       | Unselected channel at V <sub>CC</sub>     |     |                    | -2.5                 |      |
| Maximum static analog reference current into REF+ |                                                             | V <sub>ref+</sub> = V <sub>CC</sub> ,                          | V <sub>ref-</sub> = GND                   |     |                    | 10                   | μA   |
| C <sub>i</sub>                                    | Input capacitance                                           | Analog inputs                                                  |                                           |     | 7                  |                      | pF   |
|                                                   |                                                             | Control inputs                                                 |                                           |     | 5                  |                      |      |

(1) All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

**OPERATING CHARACTERISTICS**

over recommended operating free-air temperature range,  $V_{CC} = V_{ref+} = 4.5\text{ V to }5.5\text{ V}$ , I/O CLOCK frequency = 2.1 MHz (unless otherwise noted)

|       |                                     | TEST CONDITIONS   | MIN | TYP <sup>(1)</sup> | MAX       | UNIT |
|-------|-------------------------------------|-------------------|-----|--------------------|-----------|------|
| $E_L$ | Linearity error, see <sup>(2)</sup> | TLC1542C, I, or Q |     |                    | $\pm 0.5$ | LSB  |
|       |                                     | TLC1543C, I, or Q |     |                    | $\pm 1$   | LSB  |
|       |                                     | TLC1542M          |     |                    | $\pm 1$   | LSB  |

(1) All typical values are at  $T_A = 25^\circ\text{C}$ .

(2) Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.

## OPERATING CHARACTERISTICS (continued)

over recommended operating free-air temperature range,  $V_{CC} = V_{ref+} = 4.5\text{ V to }5.5\text{ V}$ , I/O CLOCK frequency = 2.1 MHz (unless otherwise noted)

|                                                                       |                                                                                                                  | TEST<br>CONDITIONS                     | MIN                | TYP <sup>(1)</sup> | MAX                               | UNIT                 |
|-----------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|----------------------------------------|--------------------|--------------------|-----------------------------------|----------------------|
| E <sub>ZS</sub>                                                       | Zero-scale error, see <sup>(3)</sup>                                                                             | TLC1542C, I, or Q                      | See <sup>(4)</sup> |                    | ±1                                | LSB                  |
|                                                                       |                                                                                                                  | TLC1543C, I, or Q                      | See <sup>(4)</sup> |                    | ±1                                | LSB                  |
|                                                                       |                                                                                                                  | TLC1542M                               | See <sup>(4)</sup> |                    | ±1                                | LSB                  |
| E <sub>FS</sub>                                                       | Full-scale error, see <sup>(3)</sup>                                                                             | TLC1542C, I, or Q                      | See <sup>(4)</sup> |                    | ±1                                | LSB                  |
|                                                                       |                                                                                                                  | TLC1543C, I, or Q                      | See <sup>(4)</sup> |                    | ±1                                | LSB                  |
|                                                                       |                                                                                                                  | TLC1542M                               | See <sup>(4)</sup> |                    | ±1                                | LSB                  |
|                                                                       | Total unadjusted error, see <sup>(5)</sup>                                                                       | TLC1542C, I, or Q                      |                    |                    | ±1                                | LSB                  |
|                                                                       |                                                                                                                  | TLC1543C, I, or Q                      |                    |                    | ±1                                | LSB                  |
|                                                                       |                                                                                                                  | TLC1542M                               |                    |                    | ±1                                | LSB                  |
| Self-test output code, see <a href="#">Table 3</a> and <sup>(6)</sup> |                                                                                                                  | ADDRESS = 1011                         |                    | 512                |                                   |                      |
|                                                                       |                                                                                                                  | ADDRESS = 1100                         |                    | 0                  |                                   |                      |
|                                                                       |                                                                                                                  | ADDRESS = 1101                         |                    | 1023               |                                   |                      |
| t <sub>conv</sub>                                                     | Conversion time                                                                                                  | See timing diagrams                    |                    |                    | 21                                | μs                   |
| t <sub>c</sub>                                                        | Total cycle time (access, sample, and conversion)                                                                | See timing diagrams and <sup>(7)</sup> |                    |                    | 21<br>+10 I/O<br>CLOCK<br>periods | μs                   |
| t <sub>acq</sub>                                                      | Channel acquisition time (sample)                                                                                | See timing diagrams and <sup>(7)</sup> |                    |                    | 6                                 | I/O CLOCK<br>periods |
| t <sub>v</sub>                                                        | Valid time, DATA OUT remains valid after I/O CLOCK↓                                                              | See <a href="#">Figure 6</a>           | 10                 |                    |                                   | ns                   |
| t <sub>d(I/O-DATA)</sub>                                              | Delay time, I/O CLOCK↓ to DATA OUT valid                                                                         | See <a href="#">Figure 6</a>           |                    |                    | 240                               | ns                   |
| t <sub>d(I/O-EOC)</sub>                                               | Delay time, tenth I/O CLOCK↓ to EOC↓                                                                             | See <a href="#">Figure 7</a>           |                    | 70                 | 240                               | ns                   |
| t <sub>d(EOC-DATA)</sub>                                              | Delay time, EOC↑ to DATA OUT (MSB)                                                                               | See <a href="#">Figure 8</a>           |                    |                    | 100                               | ns                   |
| t <sub>PZH</sub> , t <sub>PZL</sub>                                   | Enable time, $\overline{CS}$ ↓ to DATA OUT (MSB driven)                                                          | See <a href="#">Figure 3</a>           |                    |                    | 1.3                               | μs                   |
| t <sub>PHZ</sub> , t <sub>PLZ</sub>                                   | Disable time, $\overline{CS}$ ↑ to DATA OUT (high impedance)                                                     | See <a href="#">Figure 3</a>           |                    |                    | 150                               | ns                   |
| t <sub>r(EOC)</sub>                                                   | Rise time, EOC                                                                                                   | See <a href="#">Figure 8</a>           |                    |                    | 300                               | ns                   |
| t <sub>f(EOC)</sub>                                                   | Fall time, EOC                                                                                                   | See <a href="#">Figure 7</a>           |                    |                    | 300                               | ns                   |
| t <sub>r(DATA)</sub>                                                  | Rise time, data bus                                                                                              | See <a href="#">Figure 6</a>           |                    |                    | 300                               | ns                   |
| t <sub>f(DATA)</sub>                                                  | Fall time, data bus                                                                                              | See <a href="#">Figure 6</a>           |                    |                    | 300                               | ns                   |
| t <sub>d(I/O-CS)</sub>                                                | Delay time, tenth I/O CLOCK↓ to $\overline{CS}$ ↓ to abort conversion (see <a href="#">Note</a> <sup>(8)</sup> ) |                                        |                    |                    | 9                                 | μs                   |

- (3) Zero-scale error is the difference between 0000000000 and the converted output for zero input voltage; full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.
- (4) Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF- convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V ( $V_{ref+}-V_{ref-}$ ); however, the electrical specifications are no longer applicable.
- (5) Total unadjusted error comprises linearity, zero-scale, and full-scale errors.
- (6) Both the input address and the output codes are expressed in positive logic.
- (7) I/O CLOCK period = 1/(I/O CLOCK frequency) (see Figure 6)
- (8) Any transitions of  $\overline{CS}$  are recognized as valid only if the level is maintained for a setup time plus two falling edges of the internal clock (1.425 μs) after the transition.

## PARAMETER MEASUREMENT INFORMATION

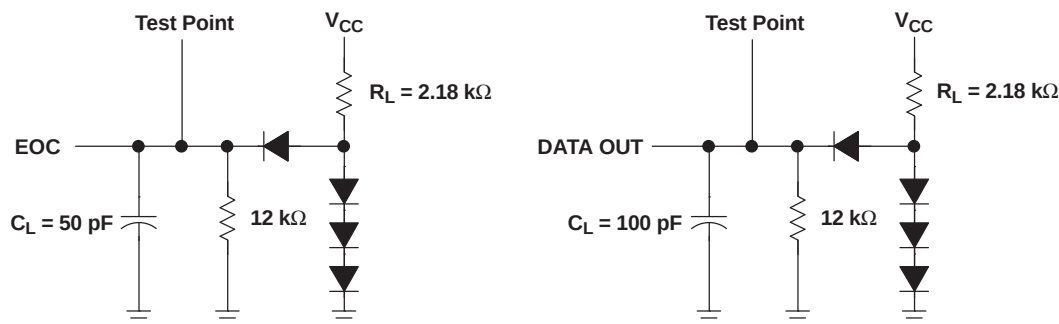


Figure 2. Load Circuits

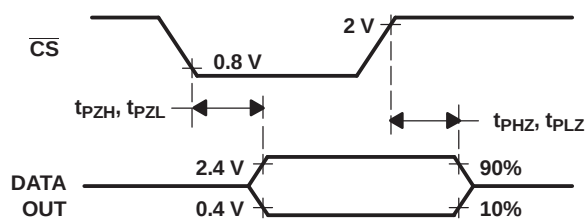


Figure 3. DATA OUT Enable and Disable Voltage Waveforms

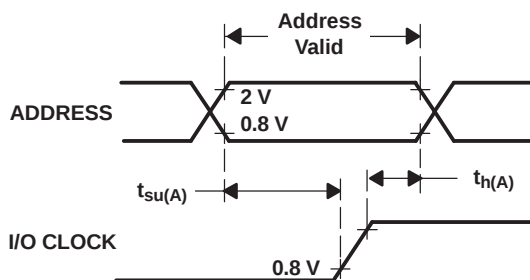


Figure 4. ADDRESS Setup and Hold Time Voltage Waveforms

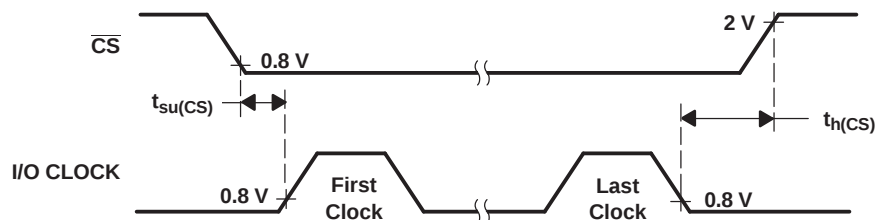


Figure 5. I/O CLOCK Setup and Hold Time Voltage Waveforms

## PARAMETER MEASUREMENT INFORMATION (continued)

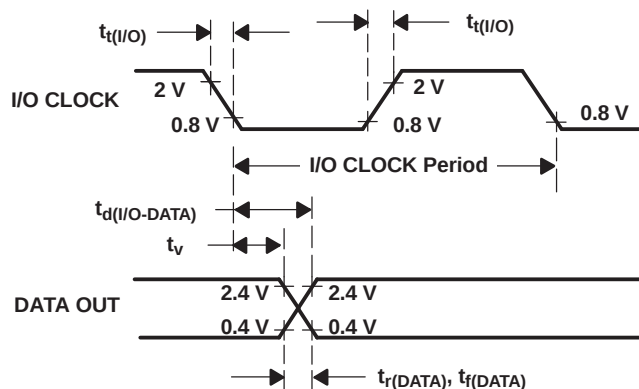


Figure 6. I/O CLOCK and DATA OUT Voltage Waveforms

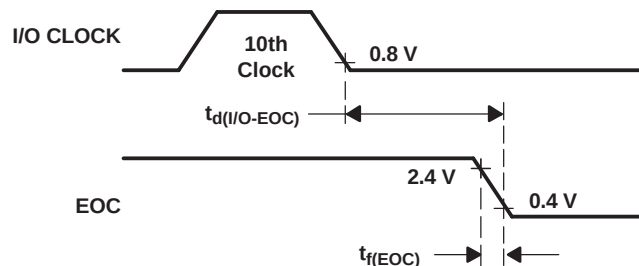


Figure 7. I/O CLOCK and EOC Voltage Waveforms

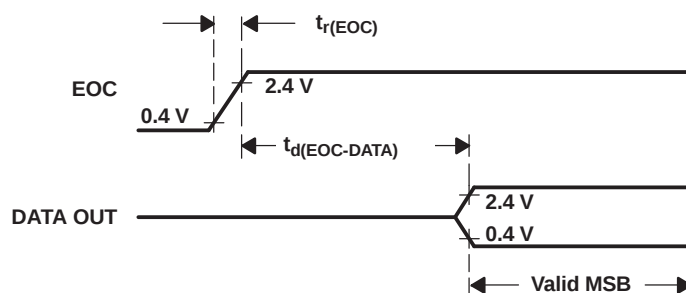
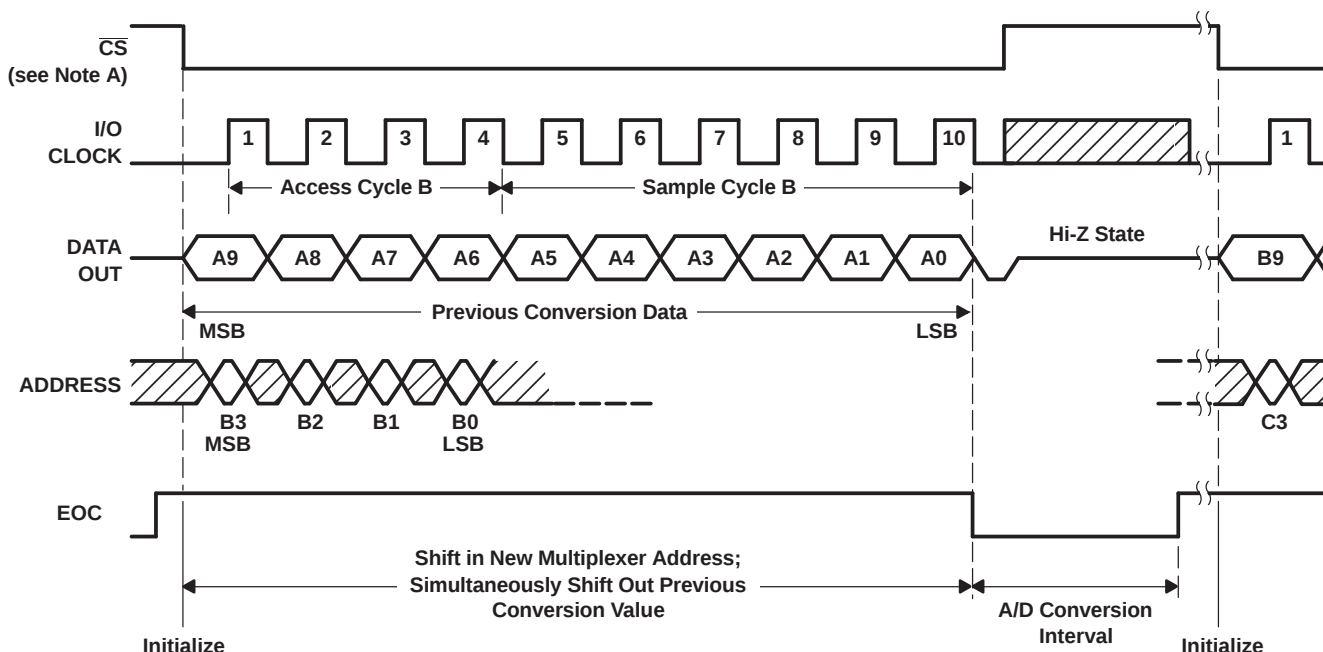


Figure 8. EOC and DATA OUT Voltage Waveforms

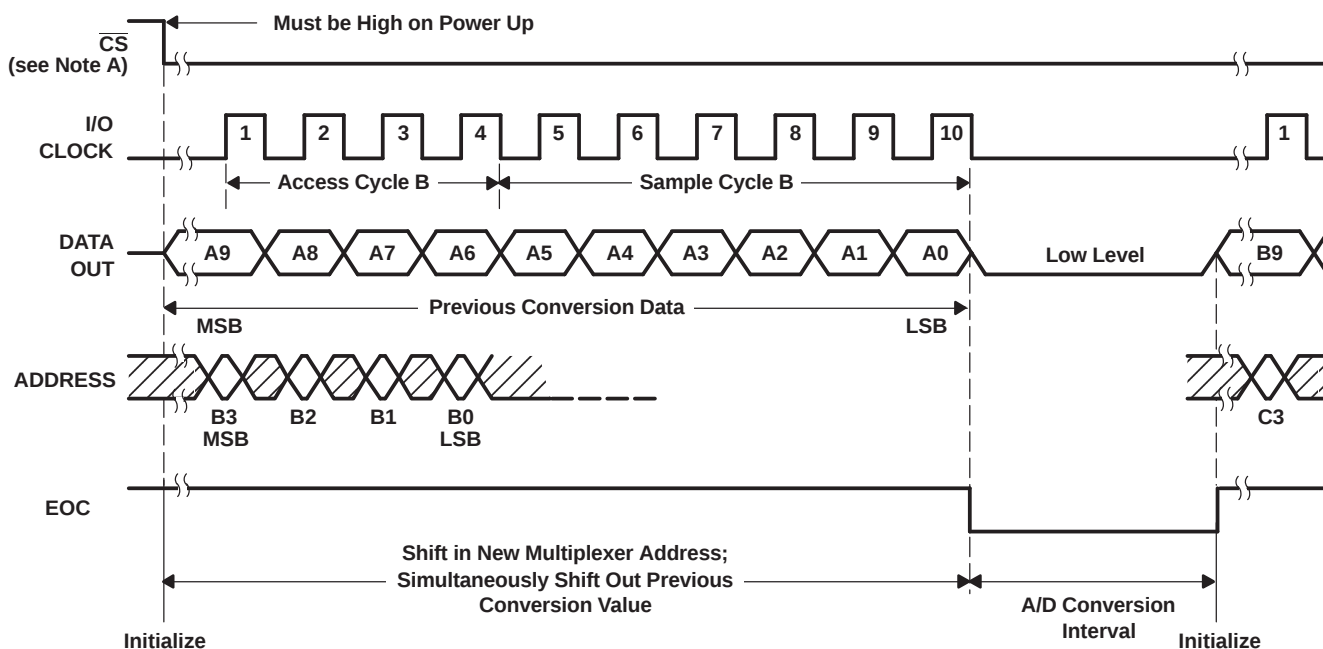
## PARAMETER MEASUREMENT INFORMATION (continued)

### TIMING DIAGRAMS



- A. To minimize errors caused by noise at  $\overline{CS}$ , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after  $\overline{CS}\downarrow$  before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum  $\overline{CS}$  setup time has elapsed.

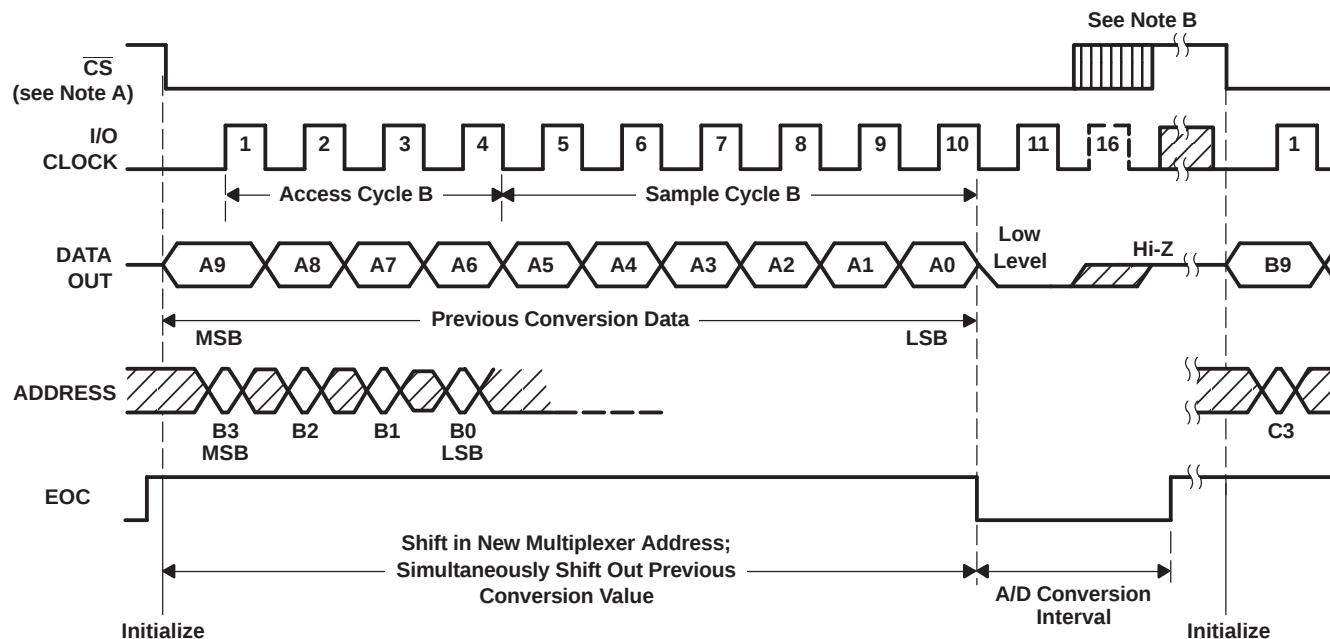
Figure 9. Timing for 10-Clock Transfer Using  $\overline{CS}$



- A. To minimize errors caused by noise at  $\overline{CS}$ , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after  $\overline{CS}\downarrow$  before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum  $\overline{CS}$  setup time has elapsed.

Figure 10. Timing for 10-Clock Transfer Not Using  $\overline{CS}$

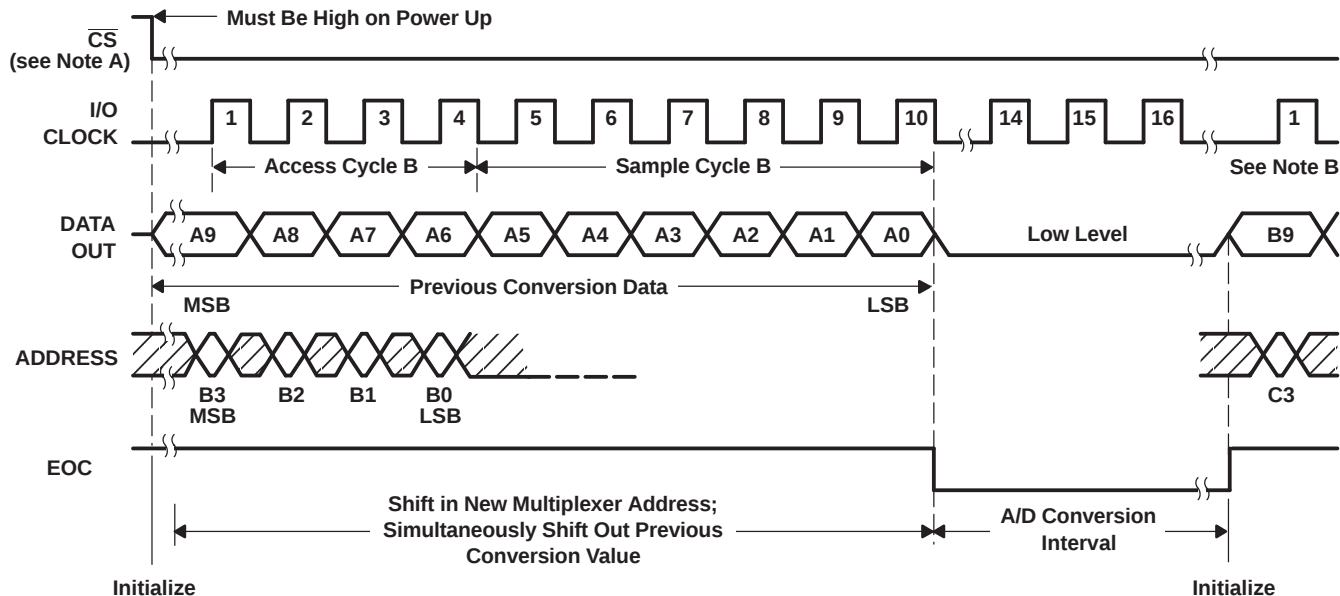
## PARAMETER MEASUREMENT INFORMATION (continued)



- A. To minimize errors caused by noise at  $\overline{CS}$ , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after  $\overline{CS}\downarrow$  before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum  $\overline{CS}$  setup time has elapsed.
- B. A low-to-high transition of  $\overline{CS}$  disables ADDRESS and the I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.

**Figure 11. Timing for 11- to 16-Clock Transfer Using  $\overline{CS}$  (Serial Transfer Interval Shorter Than Conversion)**

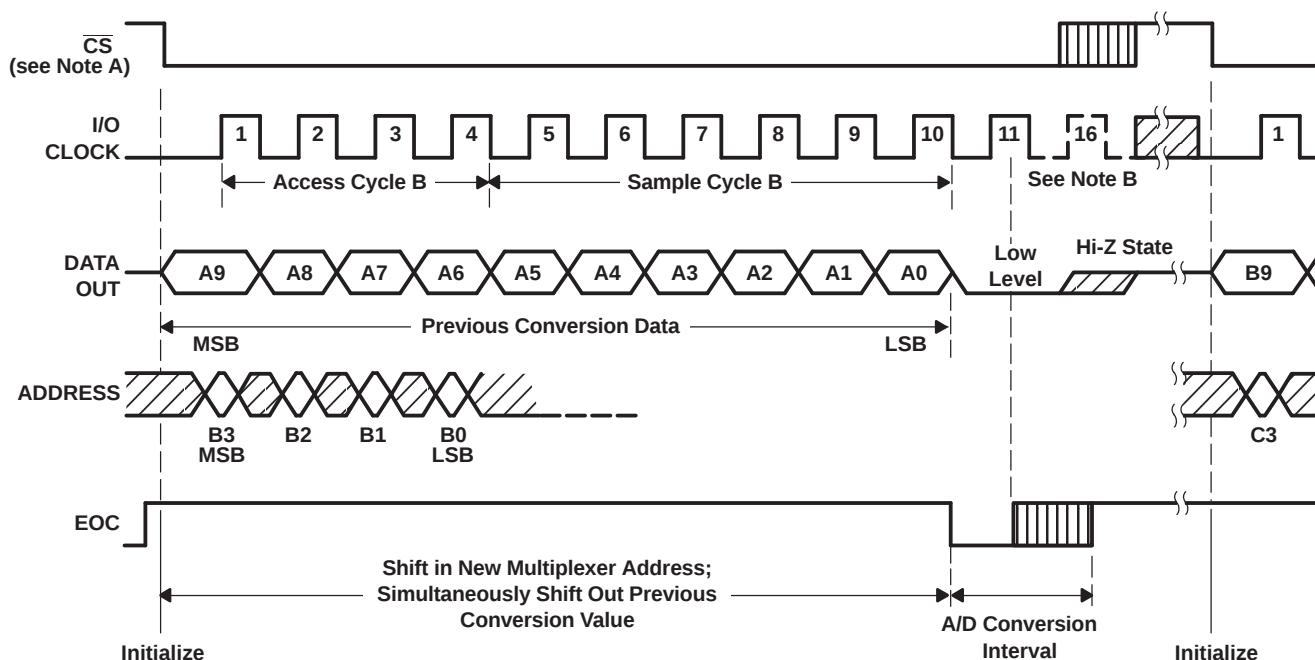
# PARAMETER MEASUREMENT INFORMATION (continued)



- To minimize errors caused by noise at  $\overline{CS}$ , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after  $\overline{CS}\downarrow$  before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum  $\overline{CS}$  setup time has elapsed.
- The first I/O CLOCK must occur after the rising edge of EOC.

**Figure 12. Timing for 16-Clock Transfer Not Using  $\overline{CS}$  (Serial Transfer Interval Shorter Than Conversion)**

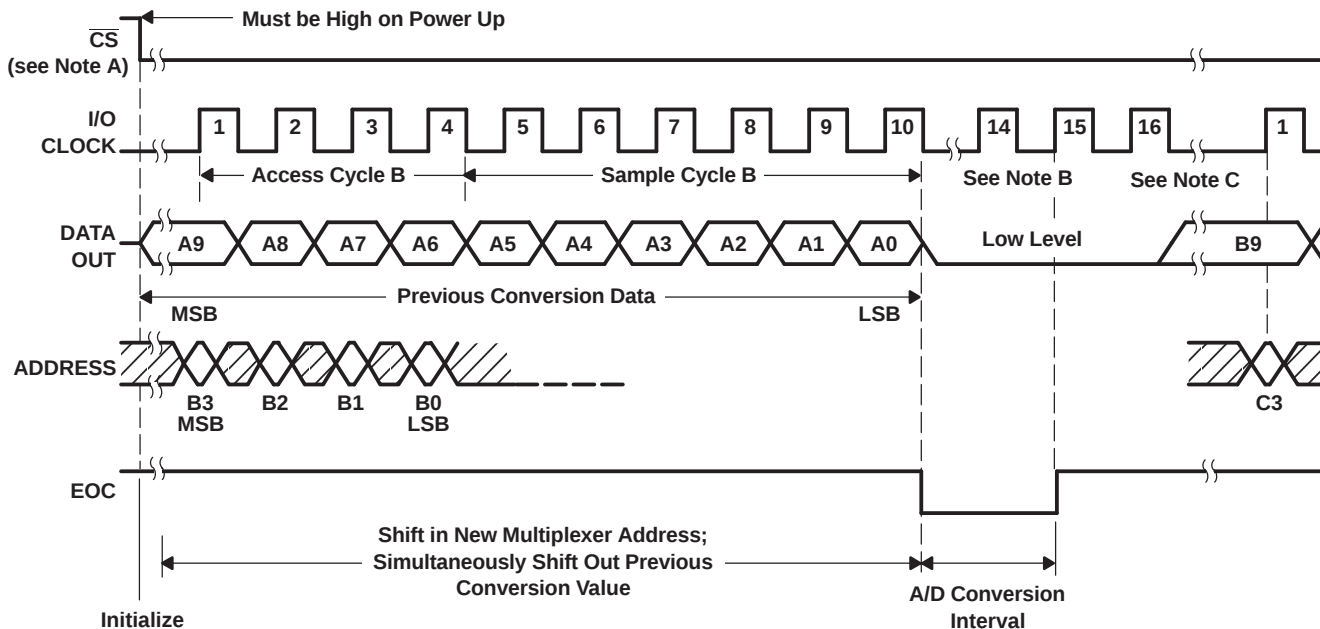
## PARAMETER MEASUREMENT INFORMATION (continued)



- A. To minimize errors caused by noise at  $\overline{CS}$ , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after  $\overline{CS}\downarrow$  before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum  $\overline{CS}$  setup time has elapsed.
- B. The 11th rising edge of the I/O CLOCK sequence must occur before the conversion is complete to prevent losing serial interface synchronization.

**Figure 13. Timing for 11- to 16-Clock Transfer Using  $\overline{CS}$  (Serial Transfer Interval Longer Than Conversion)**

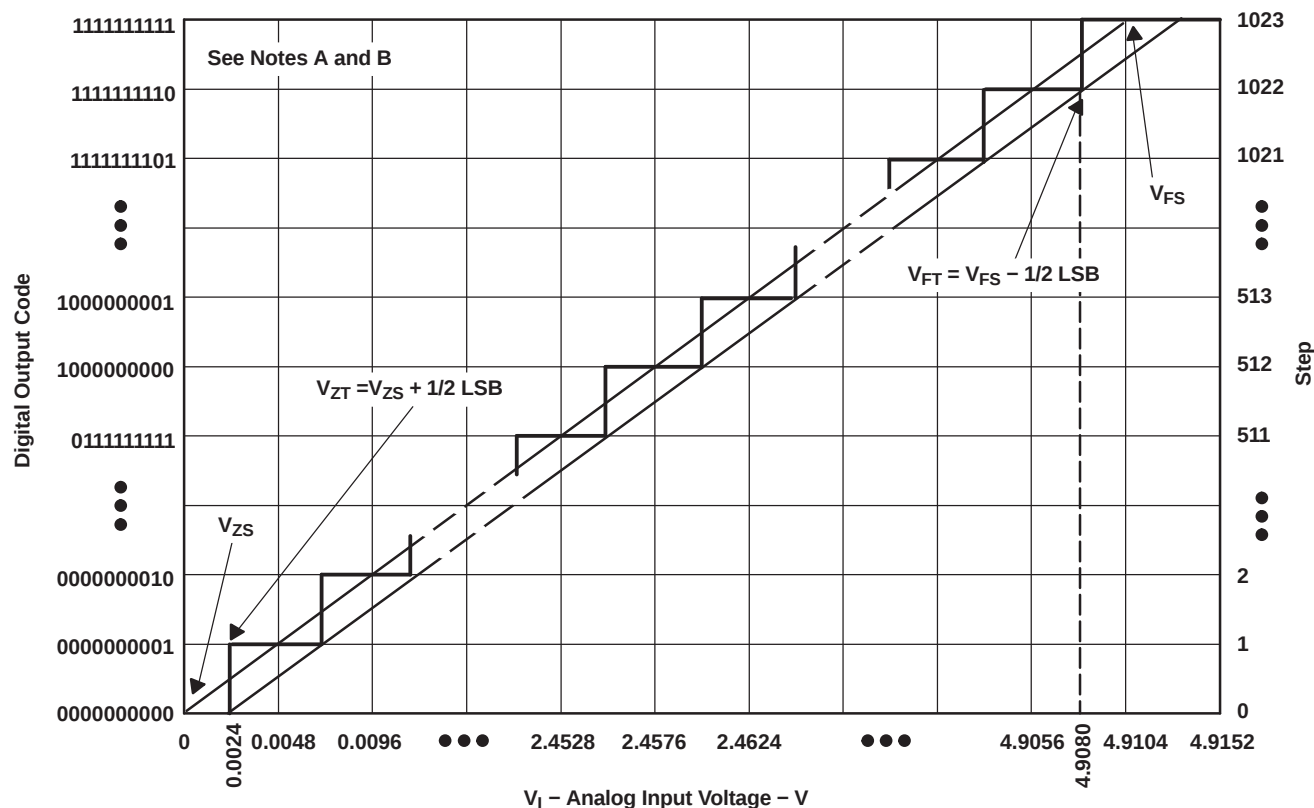
## PARAMETER MEASUREMENT INFORMATION (continued)



- A. A. To minimize errors caused by noise at  $\overline{CS}$ , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after  $\overline{CS}\downarrow$  before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum  $\overline{CS}$  setup time has elapsed.
- B. The 11th rising edge of the I/O CLOCK sequence must occur before the conversion is complete to prevent losing serial interface synchronization.
- C. C. The I/O CLOCK sequence is exactly 16 clock pulses long.

**Figure 14. Timing for 16-Clock Transfer Not Using  $\overline{CS}$  (Serial Transfer Interval Longer Than Conversion)**

## APPLICATION INFORMATION



- A. This curve is based on the assumption that  $V_{ref+}$  and  $V_{ref-}$  have been adjusted so that the voltage at the transition from digital 0 to 1 ( $V_{ZT}$ ) is 0.0024 V and the transition to full scale ( $V_{FT}$ ) is 4.908 V. 1 LSB = 4.8 mV.
- B. The full-scale value ( $V_{FS}$ ) is the step whose nominal midstep value has the highest absolute value. The zero-scale value ( $V_{ZS}$ ) is the step whose nominal midstep value equals zero.

Figure 15. Ideal Conversion Characteristics

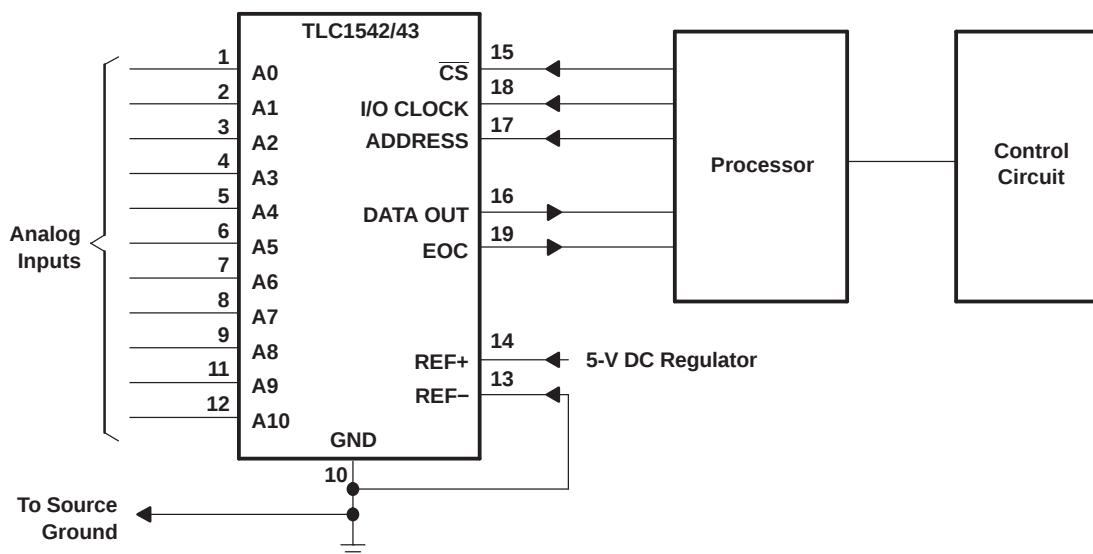


Figure 16. Serial Interface

## APPLICATION INFORMATION (continued)

### SIMPLIFIED ANALOG INPUT ANALYSIS

Using the equivalent circuit in [Figure 17](#), the time required to charge the analog input capacitance from 0 to  $V_S$  within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S (1 - e^{-t_c / R_t C_i})$$

where

$$R_t = R_S + r_i \quad (1)$$

The final voltage to 1/2 LSB is given by

$$V_C (1/2 \text{ LSB}) = V_S - (V_S / 2048) \quad (2)$$

Equating equation 1 to equation 2 and solving for time  $t_c$  gives

$$V_S - (V_S / 2048) = V_S (1 - e^{-t_c / R_t C_i})$$

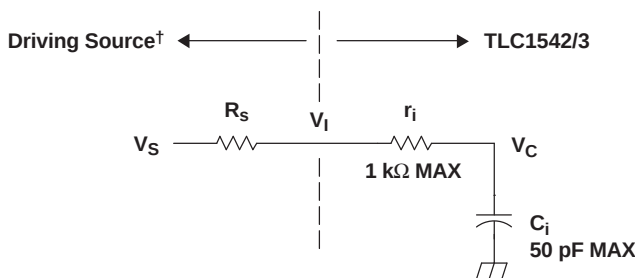
and

$$t_c (1/2 \text{ LSB}) = R_t \times C_i \times \ln(2048) \quad (3)$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c (1/2 \text{ LSB}) = (R_S + 1 \text{ k}\Omega) \times 60 \text{ pF} \times \ln(2048) \quad (4)$$

This time must be less than the converter sample time shown in the timing diagrams.



$V_I$  = Input Voltage at A0–A10  
 $V_S$  = External Driving Source Voltage  
 $R_S$  = Source Resistance  
 $r_i$  = Input Resistance  
 $C_i$  = Equivalent Input Capacitance

<sup>†</sup> Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- $R_S$  must be real at the input frequency.

**Figure 17. Equivalent Input Circuit Including the Driving Source**

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| 5962-9064202Q2A  | OBSOLETE      | LCCC         | FK                 | 20   |                | TBD                        | Call TI                 | Call TI              | -55 to 125   |                         |                         |
| 5962-9064202QRA  | OBSOLETE      | CDIP         | J                  | 20   |                | TBD                        | Call TI                 | Call TI              | -55 to 125   |                         |                         |
| TLC1542CDW       | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | TLC1542C                | <a href="#">Samples</a> |
| TLC1542CDWG4     | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | TLC1542C                | <a href="#">Samples</a> |
| TLC1542CDWR      | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TLC1542C                | <a href="#">Samples</a> |
| TLC1542CFN       | ACTIVE        | PLCC         | FN                 | 20   | 46             | Green (RoHS<br>& no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   |              | TLC1542C                | <a href="#">Samples</a> |
| TLC1542CN        | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   |              | TLC1542CN               | <a href="#">Samples</a> |
| TLC1542CNE4      | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   |              | TLC1542CN               | <a href="#">Samples</a> |
| TLC1542IDW       | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | TLC1542I                | <a href="#">Samples</a> |
| TLC1542IDWR      | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | TLC1542I                | <a href="#">Samples</a> |
| TLC1542IDWRG4    | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | TLC1542I                | <a href="#">Samples</a> |
| TLC1542IFN       | OBSOLETE      | PLCC         | FN                 | 20   |                | TBD                        | Call TI                 | Call TI              |              |                         |                         |
| TLC1542IN        | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   |              | TLC1542IN               | <a href="#">Samples</a> |
| TLC1542INE4      | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   |              | TLC1542IN               | <a href="#">Samples</a> |
| TLC1542MFKB      | OBSOLETE      | LCCC         | FK                 | 20   |                | TBD                        | Call TI                 | Call TI              | -55 to 125   |                         |                         |
| TLC1542MJB       | OBSOLETE      | CDIP         | J                  | 20   |                | TBD                        | Call TI                 | Call TI              | -55 to 125   |                         |                         |
| TLC1542QFN       | ACTIVE        | PLCC         | FN                 | 20   |                | Green (RoHS<br>& no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   | -40 to 125   | TLC1542Q                | <a href="#">Samples</a> |
| TLC1543CDB       | ACTIVE        | SSOP         | DB                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | P1543                   | <a href="#">Samples</a> |
| TLC1543CDBG4     | ACTIVE        | SSOP         | DB                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | P1543                   | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLC1543CDBLE     | OBSOLETE      | SSOP         | DB                 | 20   |                | TBD                        | Call TI                 | Call TI              |              |                         |                         |
| TLC1543CDBR      | ACTIVE        | SSOP         | DB                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | P1543                   | <a href="#">Samples</a> |
| TLC1543CDBRG4    | ACTIVE        | SSOP         | DB                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | P1543                   | <a href="#">Samples</a> |
| TLC1543CDW       | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | TLC1543C                | <a href="#">Samples</a> |
| TLC1543CDWG4     | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | TLC1543C                | <a href="#">Samples</a> |
| TLC1543CDWR      | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | TLC1543C                | <a href="#">Samples</a> |
| TLC1543CDWRG4    | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | TLC1543C                | <a href="#">Samples</a> |
| TLC1543CFN       | ACTIVE        | PLCC         | FN                 | 20   | 46             | Green (RoHS<br>& no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   |              | TLC1543C                | <a href="#">Samples</a> |
| TLC1543CFNR      | ACTIVE        | PLCC         | FN                 | 20   | 1000           | Green (RoHS<br>& no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   | 0 to 70      | TLC1543C                | <a href="#">Samples</a> |
| TLC1543CFNRG3    | ACTIVE        | PLCC         | FN                 | 20   | 1000           | Green (RoHS<br>& no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   | 0 to 70      | TLC1543C                | <a href="#">Samples</a> |
| TLC1543CN        | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   |              | TLC1543CN               | <a href="#">Samples</a> |
| TLC1543IDB       | ACTIVE        | SSOP         | DB                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | Y1543                   | <a href="#">Samples</a> |
| TLC1543IDBG4     | ACTIVE        | SSOP         | DB                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | Y1543                   | <a href="#">Samples</a> |
| TLC1543IDBLE     | OBSOLETE      | SSOP         | DB                 | 20   |                | TBD                        | Call TI                 | Call TI              |              |                         |                         |
| TLC1543IDBR      | ACTIVE        | SSOP         | DB                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | Y1543                   | <a href="#">Samples</a> |
| TLC1543IDBRG4    | ACTIVE        | SSOP         | DB                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | Y1543                   | <a href="#">Samples</a> |
| TLC1543IDW       | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | TLC1543I                | <a href="#">Samples</a> |
| TLC1543IDWG4     | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | TLC1543I                | <a href="#">Samples</a> |
| TLC1543IDWR      | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | TLC1543I                | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLC1543IDWRG4    | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | TLC1543I                | <a href="#">Samples</a> |
| TLC1543IFN       | ACTIVE        | PLCC         | FN                 | 20   | 46             | Green (RoHS<br>& no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   |              | TLC1543I                | <a href="#">Samples</a> |
| TLC1543IFNG3     | ACTIVE        | PLCC         | FN                 | 20   | 46             | Green (RoHS<br>& no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   |              | TLC1543I                | <a href="#">Samples</a> |
| TLC1543IN        | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   |              | TLC1543IN               | <a href="#">Samples</a> |
| TLC1543INE4      | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   |              | TLC1543IN               | <a href="#">Samples</a> |
| TLC1543QDB       | ACTIVE        | SSOP         | DB                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | 1543Q                   | <a href="#">Samples</a> |
| TLC1543QDBG4     | ACTIVE        | SSOP         | DB                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | 1543Q                   | <a href="#">Samples</a> |
| TLC1543QDBR      | ACTIVE        | SSOP         | DB                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | 1543Q                   | <a href="#">Samples</a> |
| TLC1543QDBRG4    | ACTIVE        | SSOP         | DB                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | 1543Q                   | <a href="#">Samples</a> |
| TLC1543QDW       | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | TLC1543Q                | <a href="#">Samples</a> |
| TLC1543QDWG4     | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | TLC1543Q                | <a href="#">Samples</a> |
| TLC1543QDWR      | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | TLC1543Q                | <a href="#">Samples</a> |
| TLC1543QDWRG4    | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | TLC1543Q                | <a href="#">Samples</a> |
| TLC1543QFN       | ACTIVE        | PLCC         | FN                 | 20   |                | Green (RoHS<br>& no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   | -40 to 125   | TLC1543Q                | <a href="#">Samples</a> |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### **OTHER QUALIFIED VERSIONS OF TLC1543 :**

- Enhanced Product: [TLC1543-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLC1542CDWR   | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| TLC1542IDWR   | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| TLC1543CDBR   | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| TLC1543IDBR   | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| TLC1543QDBR   | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| TLC1543QDBRG4 | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| TLC1543QDWR   | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLC1542CDWR   | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| TLC1542IDWR   | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| TLC1543CDBR   | SSOP         | DB              | 20   | 2000 | 367.0       | 367.0      | 38.0        |
| TLC1543IDBR   | SSOP         | DB              | 20   | 2000 | 367.0       | 367.0      | 38.0        |
| TLC1543QDBR   | SSOP         | DB              | 20   | 2000 | 367.0       | 367.0      | 38.0        |
| TLC1543QDBRG4 | SSOP         | DB              | 20   | 2000 | 367.0       | 367.0      | 38.0        |
| TLC1543QDWR   | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



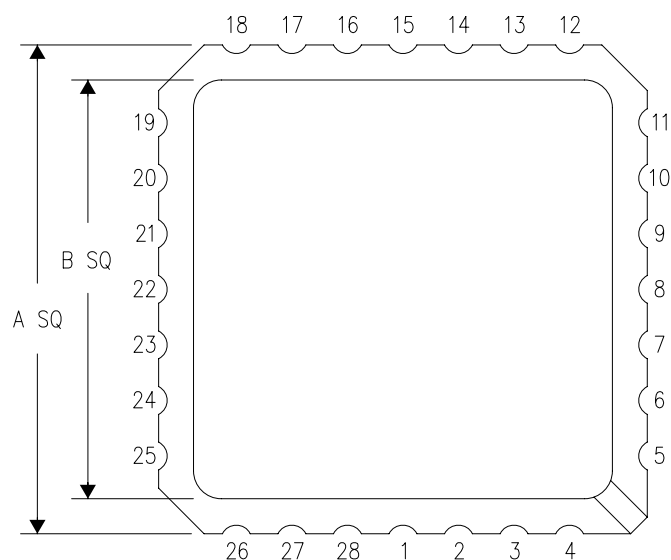
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF<br>TERMINALS<br>** | A                |                  | B                |                  |
|---------------------------|------------------|------------------|------------------|------------------|
|                           | MIN              | MAX              | MIN              | MAX              |
| 20                        | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                        | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                        | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                        | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                        | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                        | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



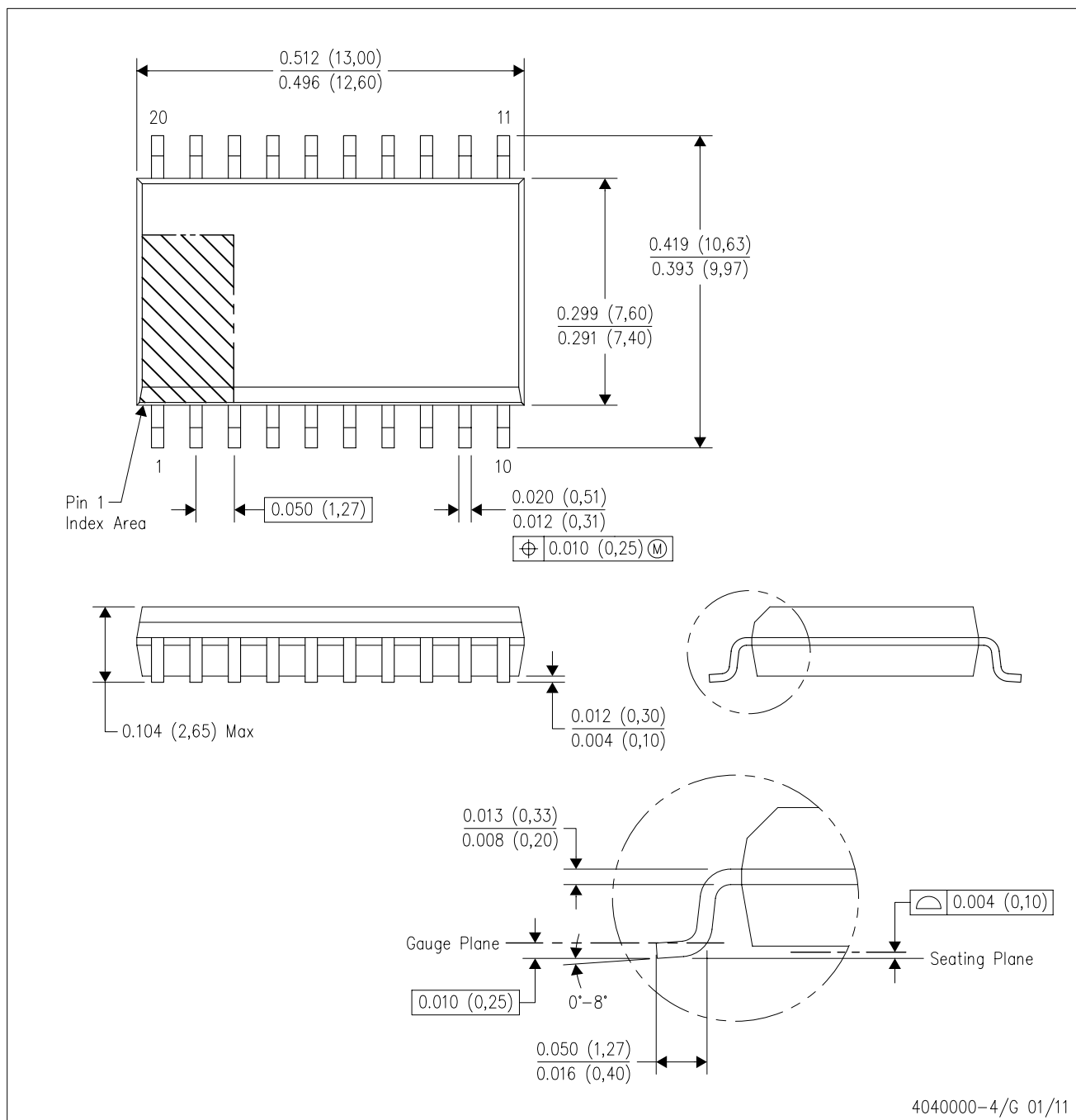
14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

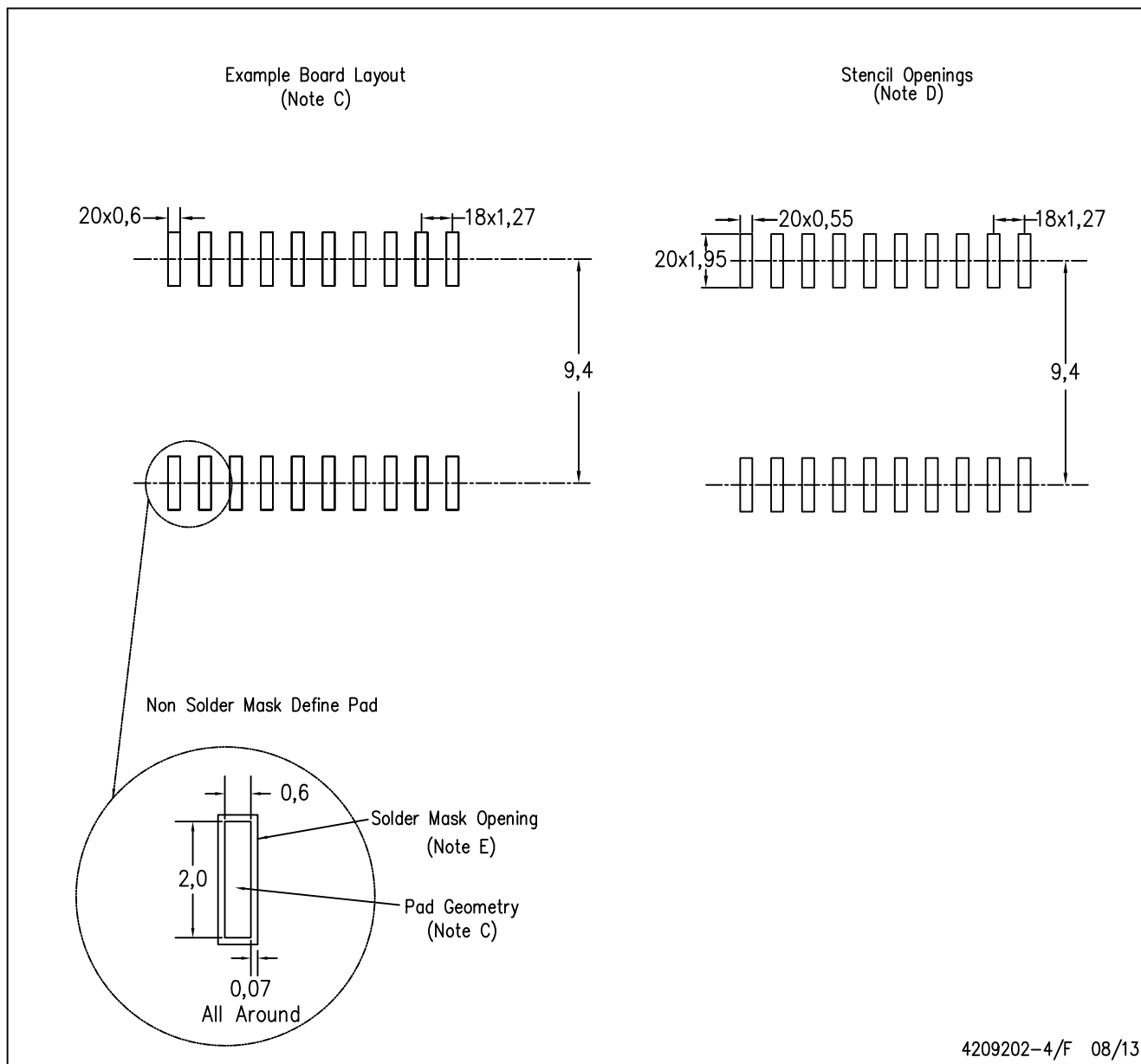
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

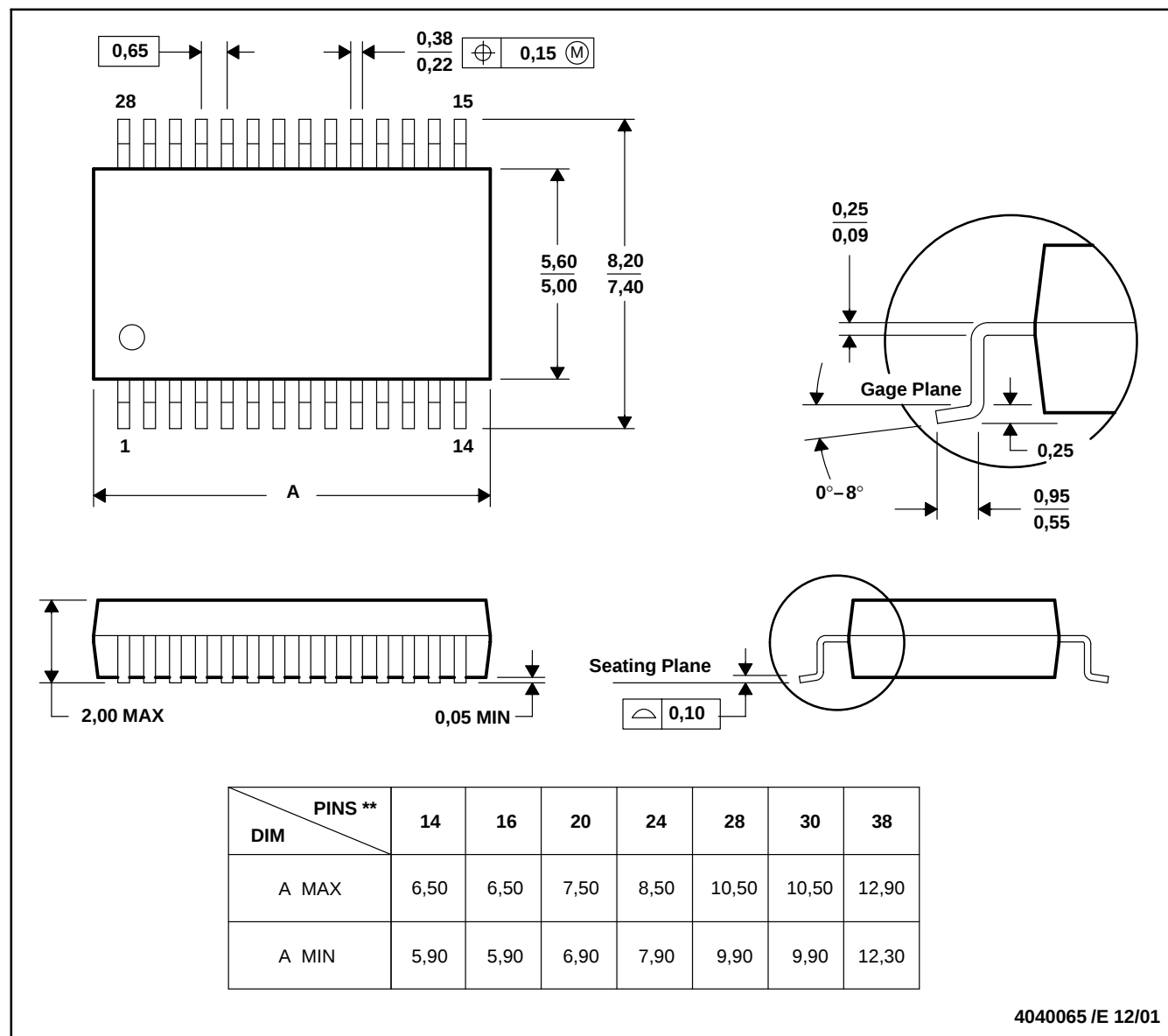


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN

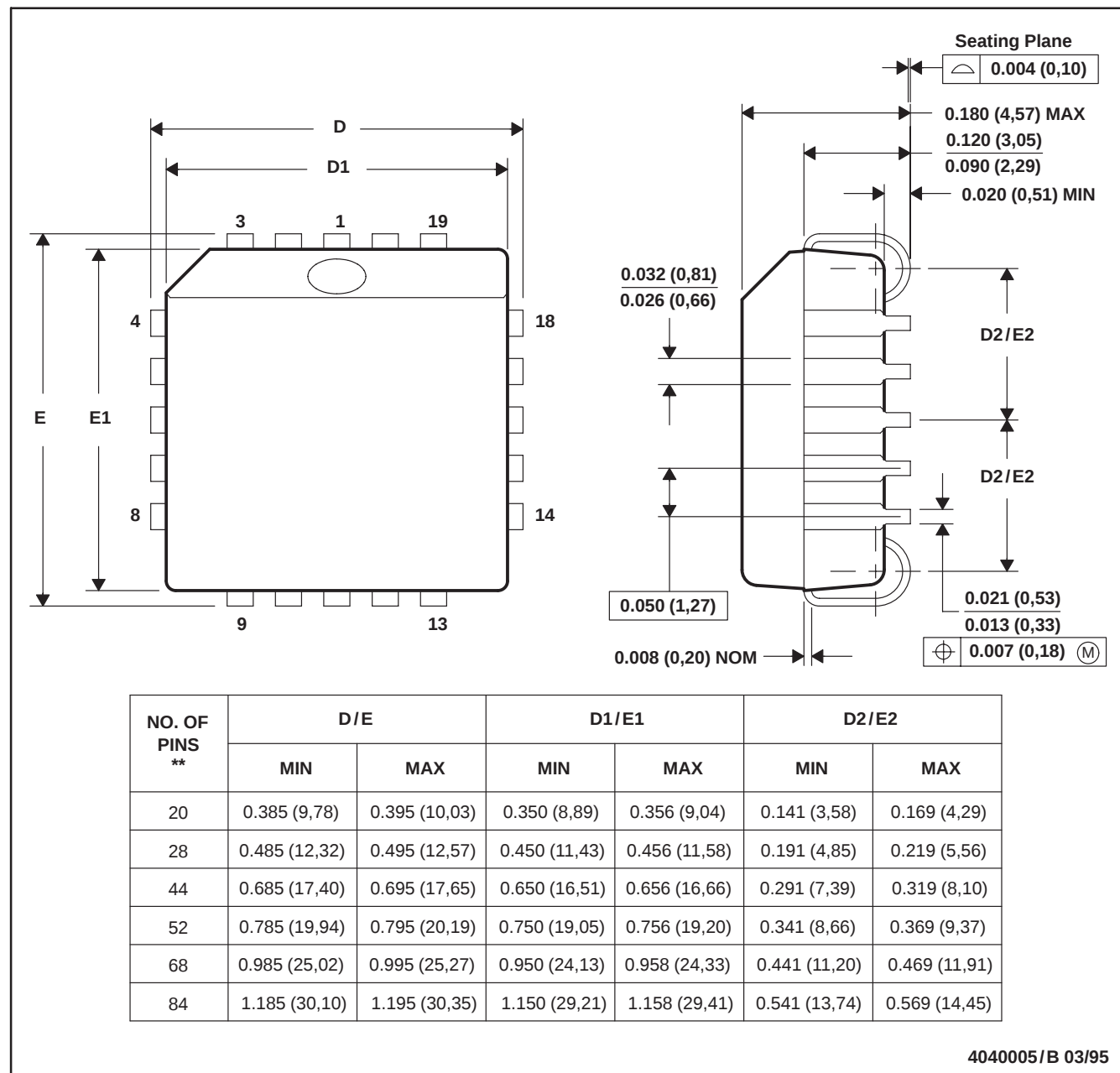


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## FN (S-PQCC-J\*\*)

## PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-018

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

|                              |                                                                                      |
|------------------------------|--------------------------------------------------------------------------------------|
| Audio                        | <a href="http://www.ti.com/audio">www.ti.com/audio</a>                               |
| Amplifiers                   | <a href="http://amplifier.ti.com">amplifier.ti.com</a>                               |
| Data Converters              | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>                       |
| DLP® Products                | <a href="http://www.dlp.com">www.dlp.com</a>                                         |
| DSP                          | <a href="http://dsp.ti.com">dsp.ti.com</a>                                           |
| Clocks and Timers            | <a href="http://www.ti.com/clocks">www.ti.com/clocks</a>                             |
| Interface                    | <a href="http://interface.ti.com">interface.ti.com</a>                               |
| Logic                        | <a href="http://logic.ti.com">logic.ti.com</a>                                       |
| Power Mgmt                   | <a href="http://power.ti.com">power.ti.com</a>                                       |
| Microcontrollers             | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a>                   |
| RFID                         | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>                                 |
| OMAP Applications Processors | <a href="http://www.ti.com/omap">www.ti.com/omap</a>                                 |
| Wireless Connectivity        | <a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a> |

### Applications

|                               |                                                                                          |
|-------------------------------|------------------------------------------------------------------------------------------|
| Automotive and Transportation | <a href="http://www.ti.com/automotive">www.ti.com/automotive</a>                         |
| Communications and Telecom    | <a href="http://www.ti.com/communications">www.ti.com/communications</a>                 |
| Computers and Peripherals     | <a href="http://www.ti.com/computers">www.ti.com/computers</a>                           |
| Consumer Electronics          | <a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>                   |
| Energy and Lighting           | <a href="http://www.ti.com/energy">www.ti.com/energy</a>                                 |
| Industrial                    | <a href="http://www.ti.com/industrial">www.ti.com/industrial</a>                         |
| Medical                       | <a href="http://www.ti.com/medical">www.ti.com/medical</a>                               |
| Security                      | <a href="http://www.ti.com/security">www.ti.com/security</a>                             |
| Space, Avionics and Defense   | <a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a> |
| Video and Imaging             | <a href="http://www.ti.com/video">www.ti.com/video</a>                                   |

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)