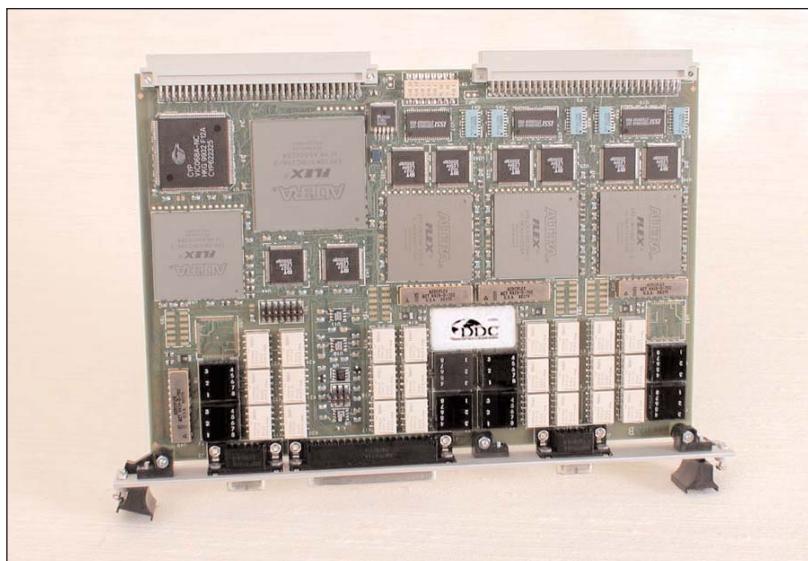


# BU-65570V, BU-65572V

## MIL-STD-1553B, BC/RT/MT VME/VXI

### QUAD TESTER/SIMULATOR CARD



#### DESCRIPTION

DDC's BU-65570V/72V is a versatile, VME/VXI Card designed for the test and simulation of MIL-STD-1553 systems. It provides full, intelligent interfacing for one to four serial dual redundant MIL-STD-1553 data buses and a VME/VXI chassis. The BU-65570V is a fixed voltage output 1553 card, and the BU-65572V is a variable voltage output 1553 card.

The BU-65572V is designed with a variable voltage output transceiver for each of the four buses. The output of these transceivers is controlled by software with a minimum of 0 V and a maximum of 21.5 V over 1024 steps.

One of the new features designed into the BU-65570V/72V is VME Master Mode. The master mode provides the capability to transfer blocks of data to the host via Direct Memory Access.

The BU-65570V/72V cards provide software controllable bus connection and configuration (transformer or direct) as well as software configuration for bus termination. The bus termination is programmable to one of three values: None, Full (37.5 ohms), and Half (75.0 ohms).

'C' programming libraries are supplied with the card. These libraries provide complete control of the board's capabilities. Software control of bus loading, bus coupling and IRIG configuration is provided by the library functions developed for this card.

The software libraries also provide access to the playback capabilities of the board. Each of the four buses is able to simultaneously replay and monitor previously recorded bus activity in real time.

Make sure the next  
Card you purchase  
has...



#### FEATURES

- VME/VXI Format, One to Four 1553 Buses
- Variable Amplitude Transceivers
- 64K Words of Shared RAM per Bus
- Simultaneous Emulation of BC, 31 RT's, and MT for Each Bus
- IRIG-B Interface
- DMA Data Transfers via VME Master Operation
- Software Configuration of Bus Coupling and Termination
- VXI Plug and Play Compatible
- 32-Bit Time Tag with 1 $\mu$ sec resolution
- Support for VxWorks® (Power PC) and Windows NT®
- Replay of previously recorded Bus Traffic via Menu and Runtime Library

#### FOR MORE INFORMATION CONTACT:

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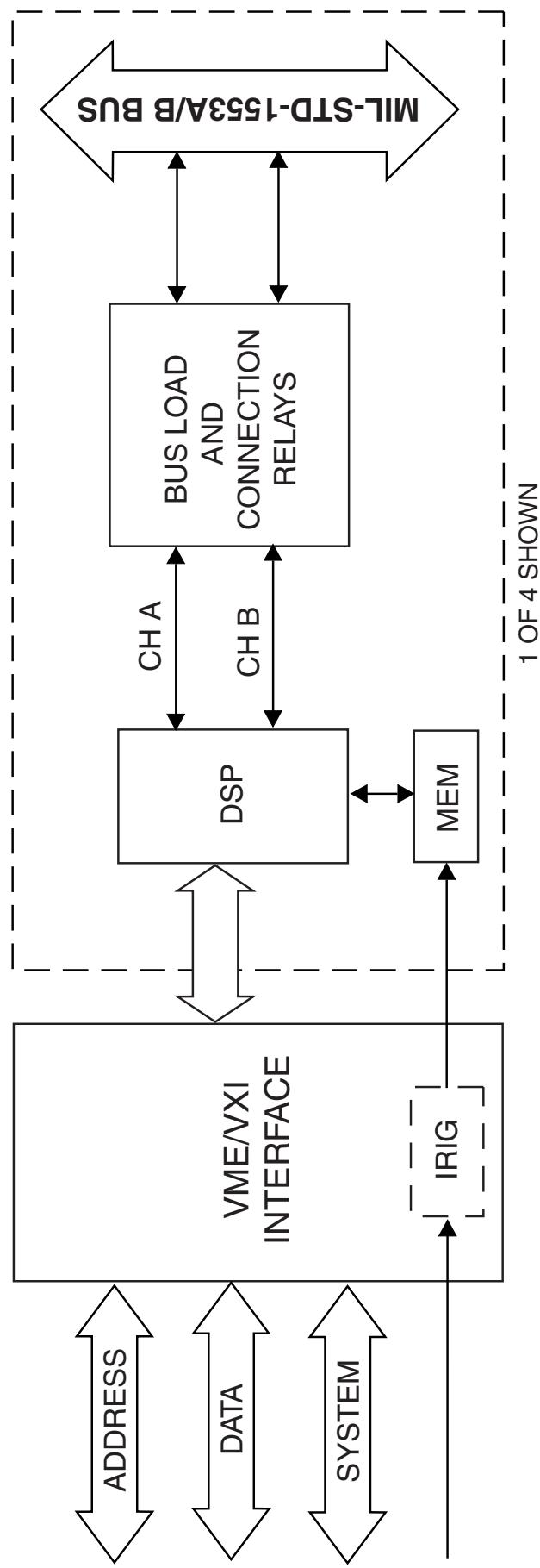


FIGURE 1. BU-65570V / BU-65572V BLOCK DIAGRAM

TABLE 1. BU-65570V/72V REQUIREMENTS AND CAPABILITIES				
<b>HARDWARE REQUIREMENTS</b>				
<ul style="list-style-type: none"> <li>• VME or VXI Chassis with Controller Card and one free slot minimum required, 233 MHz Processor or better recommended.</li> </ul>				
<b>SOFTWARE REQUIREMENTS</b>				
<ul style="list-style-type: none"> <li>• Windows® 95/98 or Windows NT® or WindRiver VxWorks®II</li> <li>• DDC's BU-69068S0 or BUS-69068S2 software diskettes/CD-ROM</li> </ul>				
<b>AVAILABLE OPERATIONS FOR EACH CHANNEL</b>				
<ul style="list-style-type: none"> <li>• Tests and Simulates MIL-STD-1553 BC and all 31 RT's</li> <li>• Provides independent Monitor Mode Operation</li> <li>• Error injection and Detection</li> </ul>				

TABLE 2. BU-65570V/65572V SPECIFICATIONS				
PARAMETER	MIN	TYP	MAX	UNITS
<b>ABSOLUTE MAXIMUM RATING</b>				
Supply Voltage • +5 V	-0.3		7.0	V
<b>RECEIVER</b>				
Threshold Voltage, Transformer Coupled, Measured on Stub		0.56		V <sub>p-p</sub>
<b>TRANSMITTER</b>				
Differential Output Voltage BU-65570V (See NOTE 5) BU-65572V (See NOTES 5 and 6)	18 0	20	27 21.5	V <sub>p-p</sub> V <sub>p-p</sub>
<b>POWER SUPPLY REQUIREMENTS</b>				
<b>PER 1553 BUS</b>				
Voltages/Tolerances • +5V	4.5		5.5	V
Current Drain @ +5.0V • Idle	220		240	mA
• 50% Transmitter Duty Cycle	720		800	mA
• 100% Transmitter Duty Cycle (See NOTE 1)	870		1000	mA
<b>1553 MESSAGE TIMING</b>				
RT Response Time (See NOTE 2)		10		μsec
BC Intermessage Gap (See NOTE 3)	25			μsec
BC/RT/MT Response Timeout (See NOTE 4)	2		29	μsec
Transmitter Watchdog Timeout		668		μsec
MT Minimum gap for capture	4			μsec
<b>THERMAL</b>				
• BU-65570V/72V	0		+55	°C
Operating Temperature	-40		+85	°C
Storage Temperature				
<b>PHYSICAL CHARACTERISTICS</b>				
Size "B"	9.2(W) X 6.3(H) (223.7 X 160)			in (mm)
Weight	20.0 (567)			oz (g)

#### NOTES for TABLE 2:

1. 100% Duty Cycle at MAX Transmit Amplitude [28 V<sub>p-p</sub>]
2. This time assumes that this card is not emulating BC.
3. This hardware time is enforced by the firmware. If an attempt to reduce this time is made, the time will be stretched to 25 μsec.
4. This time is programmable from 2 μsec to 29 μsec in 1 μsec increments.
5. Transformer Coupled, Measured on Stub.
6. Programmable in 1024 steps, within approximate range listed.

## GENERAL

The BU-65570V/72V is DDC's next generation VME/VXI Tester/Simulator which can concurrently simulate a MIL-STD-1553 Bus Controller (BC), multiple (up to 31) Remote Terminals (RT's), and an intelligent Monitor (MT) simultaneously on all four 1553 buses.

The BU-65570V/72V supports VXI "Plug and Play" installation by providing the signal MODID at J2. This signal can be enabled by an on-board jumper to allow the host to signal the card during the bus enumeration process. If it is not desirable to enable this signal, the jumper can be removed.

Full error detection features are provided in all modes of operation. In addition, user specified errors - including bit count, and Manchester II errors - may be injected in BC and any of the emulated RT modes.

Operational characteristics of the BU-65570V/72V such as variable output voltage level, bus termination, and coupling configuration are all software controllable using functions provided in the software library.

## BUS CONTROLLER MODE

The BU-6557VI/72V Bus Controller supports all MIL-STD-1553B message formats. Up to 1024 unique receive, transmit, mode code, and RT to RT messages may be defined at one time for each of the installed channels.

Programmable attributes within a message include time to next message, bus (channel A or channel B), intermessage routines, and injected error. The time to next message defines the time from the start of the present message to the start of the next message. The time to next message is programmable up to 65,535 msec in 1 μsec increments.

## MINOR AND MAJOR FRAMES

The execution of messages is controlled by a message list referred to as a frame. The frame specifies the contents and timing of complete communication runs by the BC. Each entry in the frame is either a reference to a message or a special frame symbol. The entire frame is referred to as a major frame and is divided into minor frames each of equal time duration.

The minor frame time is based on a programmable 32-bit counter with 1 μsec resolution. The BU-65570V/72V supports major frames of up to 1024 messages per installed channel, with a period of up to 72 minutes.

## BC ERROR INJECTION

Error conditions may be injected on a message by message basis. The BU-65570V/72V supports three categories of injected BC Errors: length errors, encoding errors, and gap errors. Length Errors include both word count errors and bit count errors.

**TABLE 3. J1 - DISCRETE I/O, TRIGGERS, AND IRIG**

PIN	DESCRIPTION	PIN	DESCRIPTION
1	+5VDC (fuse protected)	19	Channel 1, BC Trigger In
2	IRIG Mod In	20	Chassis Ground
3	Chassis Ground	21	IRIG (Pulse) In
4	Discrete Out 16	22	Discrete Out 15
5	Discrete Out 14	23	Discrete Out 13
6	Discrete Out 12	24	Discrete Out 11
7	Discrete Out 10	25	Discrete Out 9
8	Discrete Out 8	26	Discrete Out 7
9	Discrete Out 6	27	Discrete Out 5
10	Discrete Out 4	28	Discrete Out 3
11	Discrete Out 2	29	Discrete Out 1
12	Channel 4, BC Trigger Out	30	Channel 4, Monitor Trigger Out
13	Channel 4, BC Trigger In	31	Channel 4, Monitor Trigger In
14	Channel 3, BC Trigger Out	32	Channel 3, Monitor Trigger Out
15	Channel 3, BC Trigger In	33	Channel 3, Monitor Trigger In
16	Channel 2, BC Trigger Out	34	Channel 2, Monitor Trigger Out
17	Channel 2, BC Trigger In	35	Channel 2, Monitor Trigger In
18	Channel 1, BC Trigger Out	36	Channel 1, Monitor Trigger Out
		37	Channel 1, Monitor Trigger In

Word Counts of -32 to +1 words may be programmed. Bit counts of +3, +2, +1, -3, -2, or -1 bit may be programmed on any word within the message.

Encoding errors are implemented through the use of two simple yet powerful mechanisms for modifying the output of the BU-65570V/72V's Manchester encoder. The two modifying functions are glitch and inverse. A glitch error will force the output of the encoder to an idle bus condition for the specified period of time.

An inverse error will invert the output of the encoder for the specified period of time. The word number, starting time, and width specify the placement of the error. The error may be placed in any word within the message and its starting time may be programmed in 500 nsec with a width of up to 3  $\mu$ sec. This error injection is capable of generating a host of errors including invalid sync patterns, parity errors, and Manchester bi-phase errors.

A gap of 3, 4, or 5  $\mu$ sec (measured mid-parity crossing to mid-sync crossing) may be inserted between any two words in a message. This allows for a "dead time" gap between words of 1, 2, or 3  $\mu$ sec.

### INSERTING ASYNCHRONOUS MESSAGES

The BU-65570V/72V allows an asynchronous message to be inserted while the card is running. The inserted message will be

executed upon completion of the current message. The user will define all asynchronous messages after the End-Of-Major frame symbol and insert the message into the running frame by calling the insert message routine. The hardware does all of the work.

### BC INTERMESSAGE ROUTINES

Upon completion of a BC message, the BU-65570V/72V's on-board processor will execute up to 2 intermessage routines. Intermesssage routines are used to implement automatic retries on failed messages as well as other "end of message" functions. TABLE 5 provides a summary of the BU-65570V/72V's intermessage routines.

### RESPONSE TIMEOUT

The BU-65570V/72V BC, RT's, and MT support programmable response timeout values ranging from 2 to 29  $\mu$ secs in 1  $\mu$ sec increments.

### RT MODE

The BU-65570V/72V can concurrently simulate the operation of 31 unique remote terminals (RT's) plus a broadcast address for each of the installed channels. The BU-65570V/72V maintains 31 independent "last status" and "last command" words allowing for full support of transmit last command and transmit status

**TABLE 4. J2 - 1553 BUS 1 & 2 CONNECTOR**

PIN	DESCRIPTION
1	CH1_TXA
2	CH1_TXA
3	CH1_TXB
4	CH1_TXB
5	GND (connected to shell)
6	CH2_TXA
7	CH2_TXA
8	CH2_TXB
9	CH2_TXB

**TABLE 5. J3 - 1553 BUS 3 & 4 CONNECTOR**

PIN	DESCRIPTION
1	CH3_TXA
2	CH3_TXA
3	CH3_TXB
4	CH3_TXB
5	GND (connected to shell)
6	CH4_TXA
7	CH4_TXA
8	CH4_TXB
9	CH4_TXB

mode commands. The BU-65570V/72V supports full RT command illegalization for each transmit or receive message based on RT address and sub-address. In addition, individual mode commands may be illegalized.

### RT ERROR INJECTION

Error conditions may be injected on an individual RT/SA basis. The BU-65570V/72V supports five categories of injected RT errors: length errors, encoding errors, gap errors, status address errors, and response errors. Length errors include both word count errors and bit count errors. Word count errors of -32 to +1 words may be programmed. Bit counts of +3, +2, +1, -3, -2, or -1 bit may be programmed on any word within the message.

Encoding errors are implemented through the use of two simple yet powerful mechanisms for modifying the output of the BU-65570V/72V's Manchester encoder. The two modifying functions are glitch and inverse. A glitch will force the output of the encoder to an idle bus condition for the specified period of time. An inverse will invert the output of the encoder for the specified period of time. The word number, starting time, and width specify the placement of this error. The error may be placed in any word within the message. The starting time is programmed in 500 nsec increments from the beginning of the specified word.

The width of the error is specified in 50 nsec increments up to 3  $\mu$ sec. This error injection scheme lends itself to generating a host of errors including invalid sync patterns, parity errors, and Manchester bi-phase errors.

A gap of 3, 4, or 5  $\mu$ sec (measured mid parity crossing to mid-sync crossing) may be inserted between any two words in a message. This allows for a "dead time" gap between words of 1, 2, or 3  $\mu$ sec. A status address error may be injected in which the RT responds with a status word containing an RT address, which does not match the terminal's RT address. The RT may be programmed to respond with any value from zero to 31 in its status response.

The BU-65570V/72V supports three types of response errors: no response, a late response, or a response on the wrong bus. No response errors may be programmed for a single bus (Bus A or Bus B) or for both buses. Injecting a no response error on one bus provides a simple mechanism for testing bus controller retry conditions. A late response may be programmed in the range of 2 to 30  $\mu$ secs in 1  $\mu$ sec increments.

### RT INTERMESSAGE ROUTINES

The RT section of the BU-65570V/72V also supports intermessage routines. Upon completion of an RT message the BU-65570V/72V's on-board processor executes two intermessage routines. The data table that was used by the RT for a given message specifies which intermessage routines will be executed. Refer to TABLE 6 for a summary of the BU-65570V/72V's intermessage routines.

### BC/RT DATA TABLES

For each of the installed 1553 channels, the BU-65570V/72V maintains 1024 data tables within the shared RAM. Each data table may be up to 32 words in length. These data tables are common to both BC and RT. Internal lookup tables map each RT address, T/R, sub-address combination (RT mode) and message number (BC mode) to a chosen data table. Data tables may be read or written to in real time by the user and may be either single or double buffered. Double buffering can be used to avoid the memory access contention that occurs when the PC's application and the 1553 bus access data tables simultaneously. The BU-65570V/72V provides an optional block data mode in which the data table number associated with a given BC or RT message is incremented after completion of the message. The block data mode is implemented as a circular data structure. Each BC message and RT command (RT address, T/R, and sub-address) has three data table numbers associated with it: first, last, and current. The current data table number will be incremented after completion of a message until the value of 'last' is reached, at which point

**TABLE 6. BC/RT INTERMESSAGE ROUTINES**

NO OPERATION
RETRY CURRENT MESSAGE ON ALTERNATE BUS *
RETRY CURRENT MESSAGE AND REMAIN ON ALTERNATE BUS *
RETRY ON SAME BUS *
INTERRUPT ON END OF MESSAGE
INTERRUPT ON FRAME SYMBOL *
SET SERVICE REQUEST BIT IN STATUS **
RESET SERVICE REQUEST BIT IN STATUS **
INTERRUPT AFTER ACCESSING TX/RX DATA TABLE
INTERRUPT AFTER MODE COMMAND **
INTERRUPT AFTER TX/RX COMMAND TEMPLATE MATCH **
INTERRUPT AFTER MODE COMMAND TEMPLATE MATCH **
TIME-TAG (STORE RTC IN A CIRCULAR QUEUE)
RETRY ON SAME BUS AND THEN ON ALTERNATE BUS *
SET OUTPUT TRIGGER
WAIT FOR INPUT TRIGGER *
NO RESPONSE ON BOTH BUSES **
SET BUSY BIT IN STATUS **
RESET BUSY BIT IN STATUS **
SKIP NEXT MESSAGE *
SKIP NEXT MESSAGE ONCE *
BLOCK_DATA_BC *
BLOCK_DATA_RT **
SET_DISCRETE_0
RESET_DISCRETE_0
SET_DISCRETE_1
RESET_DISCRETE_1
SET_DISCRETE_2
RESET_DISCRETE_2
SET_DISCRETE_3
RESET_DISCRETE_3

\* Applicable to BC only.

\*\* Applicable to RT only.

the current table number will rollover to the value of first. The incrementing of the current data table is accomplished through the use of an intermessage routine.

## MONITOR MODE

The BU-65570V/72V contains an independent message monitor for each bus with the ability to filter messages in real time. Monitor selection or filtering is performed through the use of a lookup table based on the RT address, T/R bit, and sub-address

of command words. Monitored messages are stored in the shared RAM on the BU-65570V/72V. Each entry in the monitor buffer contains a header followed by a variable number of data words. Contained with the message header are the receive/transmit command(s), receive/transmit status, message format, Bus (A or B), a capture flag, word count (actual number of words in the message), a detected error field, and a 32-bit time tag (1  $\mu$ sec resolution).

The transfer of the messages from the card's circular buffer to the host memory/disk is determined by the capture flag, which is set upon detection of a predefined event. Capture events include immediate, command template match, exception, or trigger. The command template event is based on a 16-bit command word with a 16-bit mask. Exception events may be programmed for any exception: invalid command, invalid data, invalid status, gap preceding data, response time error, wrong RT address error, status set condition or an illegal command. The trigger event uses one of the four monitor input pins on the 9-pin D-type connector as a trigger input.

DMA transfers are possible using the PCI Master Mode. The Monitor mode can autonomously transfer monitored data to RAM in PCI address space without host CPU intervention. This greatly improves the efficiency of both the host and the BU-65570V/72V.

## INTERRUPTS

For each of the installed channels, both the BC/RT and the Monitor may request interrupts on a common output to the PCI back plane. The hardware interrupt level used by the BU-65570V/72V is selected by the Plug-and-Play capability of the PCI back plane and BIOS. An important aspect of PCI interrupts is that they are sharable. This means that the BU-65570V/72V can share an interrupt for all buses on the card.

## BC INTERRUPT GENERATION

BC interrupts may be enabled by a global interrupt mask for successful messages, communication errors, status set conditions, or on selected frame symbols (skip, break point, major frame, and minor frame symbols). The criteria for a status set condition are programmed globally through the use of a status mask. The status mask allows any of the 16 bits within the RT status word to be ignored. The status mask affects the generation of interrupts as well as the detected error field that is stored in the message structure.

BC interrupts are issued by the intermessage routines associated with messages allowing for selective interrupt generation on a message by message basis. A two-word vector is pushed onto a circular queue for each interrupt request and is transparent to the user. The queue can hold up to 64 interrupt vectors; thus, the host computer is not required to immediately acknowledge the interrupt request.

## RT INTERRUPT GENERATION

RT interrupts may be enabled by a global interrupt mask for transmit/receive messages with no message error, mode commands with no message error, transmit/receive messages with the message error bit set, or mode commands with the message error bit set.

RT interrupts are issued by intermessage routines associated with data tables allowing for selective interrupt generation on a message by message basis. A two-word vector is pushed onto a circular queue for each interrupt and is transparent to the user. The queue can hold up to 64 interrupt vectors; thus, the host computer is not required to immediately acknowledge the interrupt request.

## MONITOR INTERRUPTS

Monitor interrupts may be generated after each message is received or after one third of the monitor's circular buffer has been filled (approximately 4K words). This allows for either real-time analysis or mass collection/storage of monitored data.

## OTHER FEATURES

### VARIABLE AMPLITUDE TRANSCEIVER

The BU-65572V provides variable amplitude transceivers for each 1553 channel installed on the card. The output of the variable transceiver is software controllable in the range of 0 volts to 21.5 volts. This range is covered in 1024 steps. The user application is able to modify this amplitude in realtime by calling the appropriate library function.

The transceiver outputs can be individually controlled for each of the installed channels, while the two transceivers for a given channel will be varied simultaneously. Functions for controlling the transceiver outputs are added to the 'C' library that is provided with the card.

### IRIG-B SUPPORT

Inter-Range Instrument Group (IRIG) Standard 200-95 is provided in the BU-65570V/72V boards. The implementation of this standard into the 1553 tester/simulator board enables all messages to be tagged with time-of-day information, allowing accurate correlation between messaging on the 1553 bus and other hardware and software events that are occurring in the system. This is especially useful when trying to identify the cause of a system problem that may be directly related to message data sent over the 1553 bus. The IRIG-B timestamp for each of the installed channels may be individually selected. This allows one channel to use the internal 32 bit Time-Tag clock, while another channel will stamp the messages with the IRIG-B time. The IRIG-B timestamp, if enabled, will be combined with the internal timestamp to provide  $\mu$ sec accuracy.

## MONITOR DMA TO HOST BUFFER

The BU-65570V/72V is fully compliant to the PCI standards for both Target and Master applications. As a PCI master, the BU-65570V/72V is capable of performing DMA block data transfers from the monitor buffers on the card to a user buffer in the host memory. This will allow the transfer of data without interrupting the host processor, enabling it to perform other more important tasks.

### VXI PLUG AND PLAY

VXI Plug and Play is provided on the BU-65570V/72V with the signal MODID enabled on J2. When the jumper is in place to enable this signal, the system will query the card for information contained in the VXI registers of the card. These registers contain information such as Manufacturer ID, Card Address Space (A24 or A32), Required Memory, and Interrupt Vector Number. The manufacturer programs the card and manufacturer information, while a jumper on the card sets the Address Space.

### SOFTWARE CONTROL OF BUS CONFIGURATION

The BU-65570V/65572V has the capability of being connected to the bus as either Transformer Coupled or Direct Coupled. Transformer coupling enables the card to be connected to the 1553 bus with a long stub of up to 20 feet. Direct coupling requires that the card be connected to the 1553 bus by a stub of no more than 1 foot. The coupling configuration is dynamically configurable via functions provided in the 'C' library. Relays on the board are used to select the correct signal path direct or transformer coupled for each of the installed channels.

This card also has the capability of modifying the bus termination to one of three different loads. If the bus termination is set to None, then the effective impedance is infinite ohms. If the bus is set to Full, then the bus termination will be 37.5 ohms. A setting of Half will cause a bus termination of 75.0 ohms. This control makes it quite simple to connect the 65570V/72V directly to another 1553 device without the need of an external load. As with the bus coupling mode, the bus termination mode is dynamically configurable via software functions provided in the 'C' library which control relays for each installed channel.

### DISCRETE OUTPUTS

This new Tester/Simulator design will include four discrete outputs per channel. These four outputs are set to logic '1' and cleared to logic '0' by use of eight new intermessage routines. The format of the routine names is SET\_DISCRETE\_X and RESET\_DISCRETE\_X. These discrete outputs may be used for signaling external equipment when a specific event or message has occurred. The intermessage routine can be attached to any message, data table, or frame symbol providing a wide variety of debug possibilities.

## SOFTWARE SUPPORT

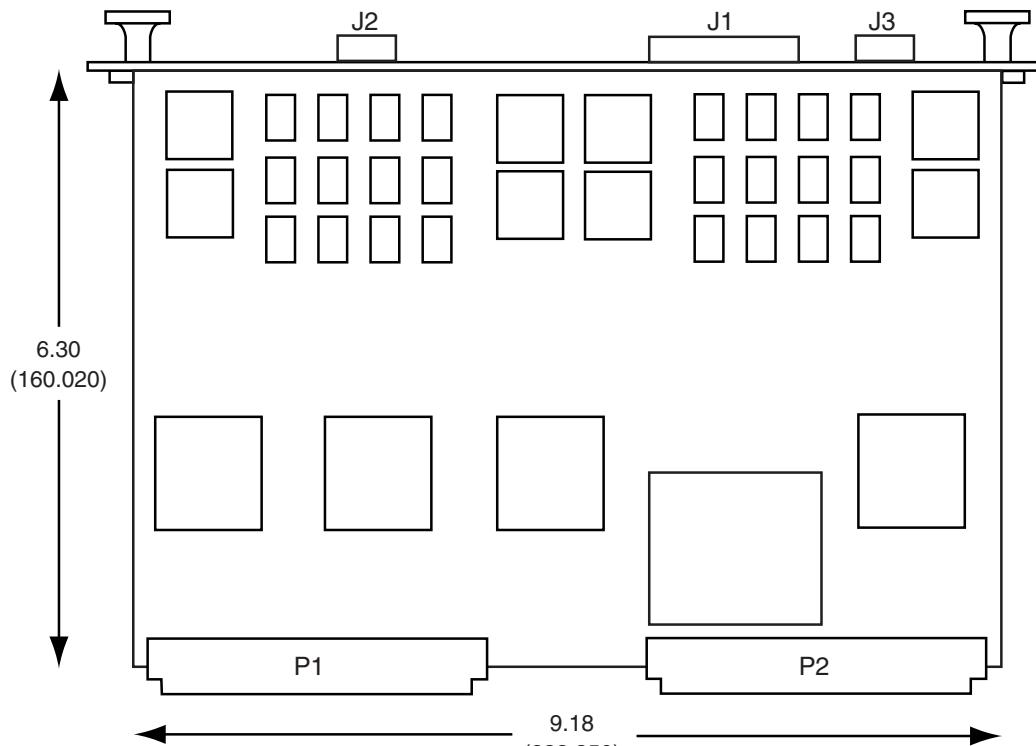
The BU-65570V/65572V is provided with a 32-bit 'C' library that supports all of the functionality of the previous versions of the DDC Tester/Simulator cards. This makes re-targeting of existing software as simple as a re-compile. The new library also contains new functions that enable full use of all of the new hardware functionality such as IRIG-B, Monitor DMA, Dynamic Bus Configuration, and Dynamic Bus Loading.

A full function Menu is also supplied with the BU-65570V/72V. This menu is for use with MXI-2 control of the VME/VXI card. Running on Windows NT, the new menu provides access to all hardware functions except DMA. The menu is an extension of

the existing Tester/Simulator menu and is completely compatible with setup and stack files that are used with the older version.

A new feature added to the menu is a "Ccode Generate" button that converts an entire setup to editable/compilable 'C' source code. This allows the major portion of Setup to be done in the menu, and any data reduction routines can be added to the generated source. The final product can then be compiled under any 'C' compiler and run.

Drivers for the BU-65570V/72V are provided for VxWorks Tornado running on a Motorola Power PC (BUS-69068S2), Windows 95/98/NT supporting an Intel platform with MXI-2 or connection to a VME/VXI chassis (BUS-69068S0).



**FIGURE 2. BU-65570V / BU-65572V MECHANICAL OUTLINE**

## ORDERING INFORMATION

### BU-6557X V X-300 Simulator and Tester PCI Card

#### Temperature Range:

3 = 0 to +55°C

#### Board Configuration:

- 1 = One Dual Redundant 1553 Channel
- 2 = Two Dual Redundant 1553 Channels
- 3 = Three Dual Redundant 1553 Channels
- 4 = Four Dual Redundant 1553 Channels

#### Transceiver Configuration:

- 0 = Fixed Bus Voltage Output
- 2 = Variable Bus Voltage Output

#### Software Included :

Windows NT Menu for MXI-II

32-bit Windows DLL/Driver supports Borland and Microsoft 32-bit C/C++ Compilers, WindRiver Tornado 6.X Drivers and Software Library.

These products contain tin-lead solder.

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