

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)}$ Max	I_D max $T_A = 25^\circ C$ (Notes 4)
-20V	495m Ω @ $V_{GS} = -4.5V$	-1.14A
	730m Ω @ $V_{GS} = -2.5V$	-0.94A
	960m Ω @ $V_{GS} = -1.8V$	-0.85A
	1300m Ω @ $V_{GS} = -1.5V$	-0.75A

Description and Applications

This MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

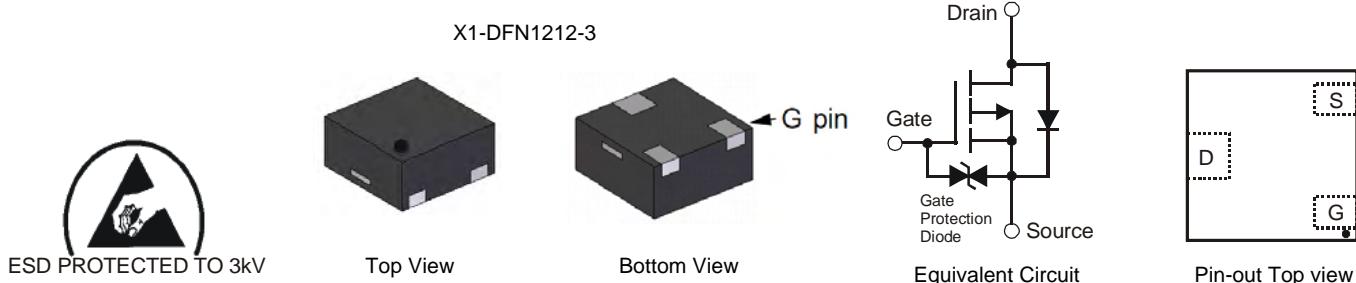
- Portable electronics

Features and Benefits

- Low Gate Threshold Voltage
- Fast Switching Speed
- ESD Protected Gate 3kV
- Totally Lead-Free & Fully RoHS compliant (Note 1)
- Halogen and Antimony Free. "Green" Device (Note 2)
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

- Case: X1-DFN1212-3
- Case Material: Molded Plastic, "Green" Molding Compound.
- UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.005 grams (approximate)



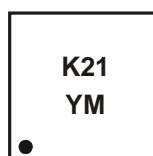
Ordering Information (Note 3)

Part Number	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
DMP21D0UFD-7	K21	7	8	3000

Notes:

- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- Halogen and Antimony free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- For packaging details, go to our website at <http://www.diodes.com>.

Marking Information



K21 = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: Y = 2011)
M = Month (ex: 9 = September)

Date Code Key

Year	2011	2012	2013	2014	2015	2016	2017					
Code	Y	Z	A	B	C	D	E					
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	± 8	V
Continuous Drain Current	Steady State	$T_A = 25^\circ\text{C}$ (Note 4)	I_D	A
		$T_A = 85^\circ\text{C}$ (Note 4)		
		$T_A = 25^\circ\text{C}$ (Note 5)		
Pulsed Drain Current (Note 6)		I_{DM}	-4.0	A

Thermal Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic		Symbol	Value	Unit
Power Dissipation	(Note 4)	P_D	930	mW
	(Note 5)		490	mW
Thermal Resistance, Junction to Ambient	(Note 4)	$R_{\theta JA}$	135	°C/W
	(Note 5)		256	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Notes:

- 4. For a device surface mounted on 15mm x 15mm x 1.6mm FR4 PCB with high coverage of 2oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
- 5. Same as note 4, except the device is mounted on minimum recommended pad layout.
- 6. Device mounted on minimum recommended pad layout test board, 10µs pulse duty cycle = 1%.

Thermal Characteristics

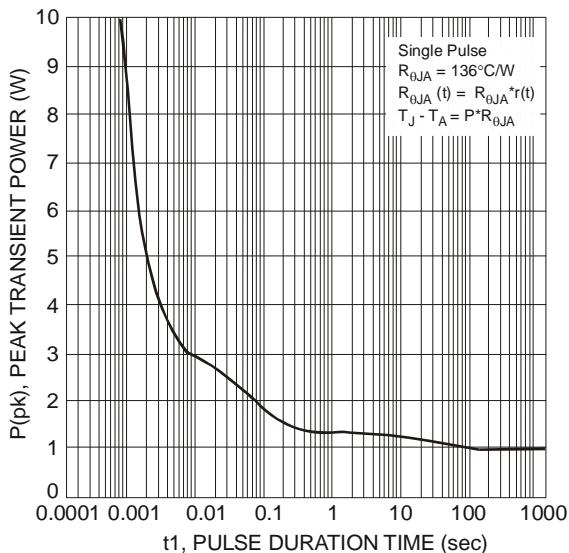


Fig. 1 Single Pulse Maximum Power Dissipation

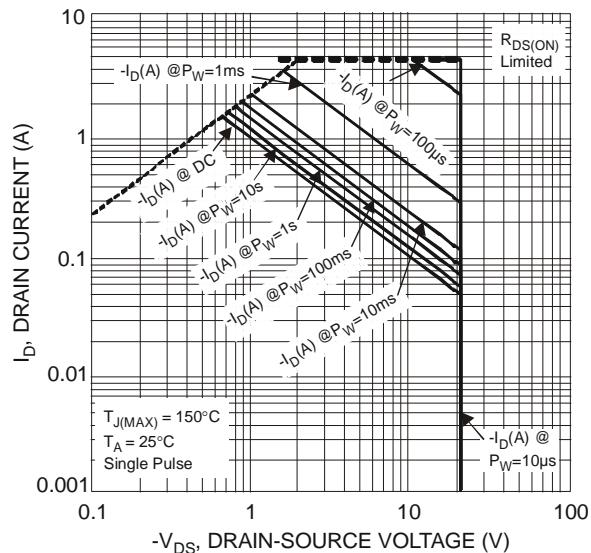


Fig. 2 SOA, Safe Operation Area

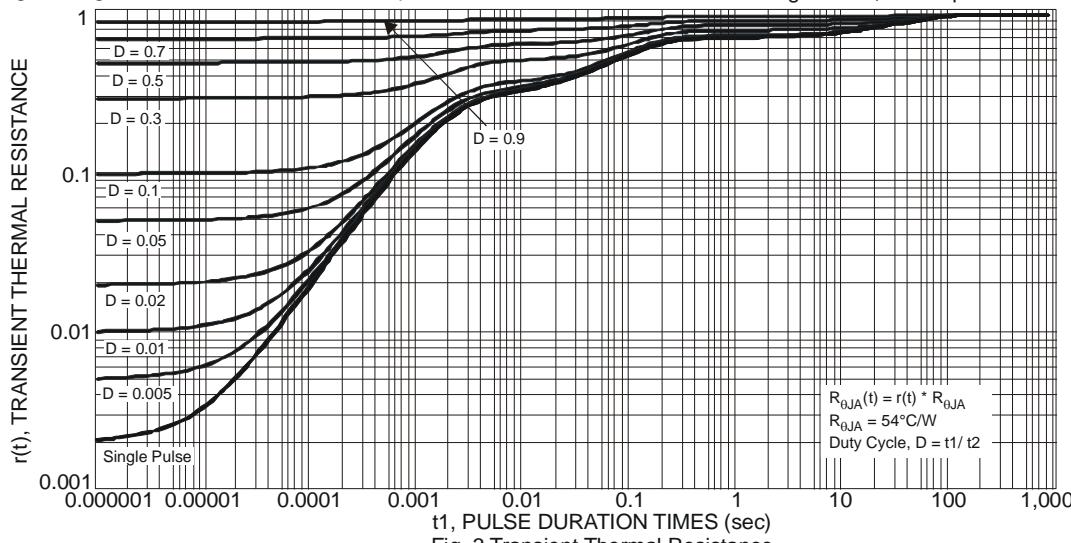


Fig. 3 Transient Thermal Resistance

Electrical Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	-	-	V	$\text{V}_{\text{GS}} = 0\text{V}$, $\text{I}_D = -250\mu\text{A}$
Zero Gate Voltage Drain Current $T_J = 25^\circ\text{C}$	I_{DSS}	-	-	-1	μA	$\text{V}_{\text{DS}} = -20\text{V}$, $\text{V}_{\text{GS}} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	-	-	± 10	μA	$\text{V}_{\text{GS}} = \pm 8\text{V}$, $\text{V}_{\text{DS}} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$\text{V}_{\text{GS(th)}}$	-0.45	-0.7	-1.2	V	$\text{V}_{\text{DS}} = \text{V}_{\text{GS}}$, $\text{I}_D = -250\mu\text{A}$
Static Drain-Source On-Resistance	$\text{R}_{\text{DS(ON)}}$	-	-	495	$\text{m}\Omega$	$\text{V}_{\text{GS}} = -4.5\text{V}$, $\text{I}_D = -800\text{mA}$
				730		$\text{V}_{\text{GS}} = -2.5\text{V}$, $\text{I}_D = -700\text{mA}$
				960		$\text{V}_{\text{GS}} = -1.8\text{V}$, $\text{I}_D = -100\text{mA}$
				1300		$\text{V}_{\text{GS}} = -1.5\text{V}$, $\text{I}_D = -100\text{mA}$
Forward Transfer Admittance	$ \text{Y}_{\text{fs}} $	50	-	-	mS	$\text{V}_{\text{DS}} = -3\text{V}$, $\text{I}_D = -300\text{mA}$
Diode Forward Voltage	V_{SD}	-	-	-1.2	V	$\text{V}_{\text{GS}} = 0\text{V}$, $\text{I}_S = -300\text{mA}$
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	-	76.5	-	pF	
Output Capacitance	C_{oss}	-	13.7	-	pF	$\text{V}_{\text{DS}} = -10\text{V}$, $\text{V}_{\text{GS}} = 0\text{V}$, $f = 1.0\text{MHz}$
Reverse Transfer Capacitance	C_{rss}	-	10.7	-	pF	
Gate Resistance	R_{g}	-	195	-	Ω	$\text{V}_{\text{DS}} = 0\text{V}$, $\text{V}_{\text{GS}} = 0\text{V}$, $f = 1\text{MHz}$
Total Gate Charge (Note 8)	Q_{g}	-	1.5	-	nC	$\text{V}_{\text{GS}} = -8\text{V}$, $\text{V}_{\text{DS}} = -15\text{V}$, $\text{I}_D = -1\text{A}$
Total Gate Charge (Note 8)	Q_{g}	-	1.0	-	nC	
Gate-Source Charge	Q_{qs}	-	0.2	-	nC	$\text{V}_{\text{GS}} = -4.5\text{V}$, $\text{V}_{\text{DS}} = -15\text{V}$, $\text{I}_D = -1\text{A}$
Gate-Drain Charge	Q_{gd}	-	0.3	-	nC	
Turn-On Delay Time	$\text{t}_{\text{D(on)}}$	-	7.1	-	ns	
Turn-On Rise Time	t_r	-	8.0	-	ns	$\text{V}_{\text{DS}} = -10\text{V}$, $-\text{I}_D = 1\text{A}$
Turn-Off Delay Time	$\text{t}_{\text{D(off)}}$	-	31.7	-	ns	$\text{V}_{\text{GS}} = -4.5\text{V}$, $\text{R}_{\text{G}} = 6\Omega$
Turn-Off Fall Time	t_f	-	18.5	-	ns	

Notes:
7. Short duration pulse test used to minimize self-heating effect.
8. Guarantee by design.

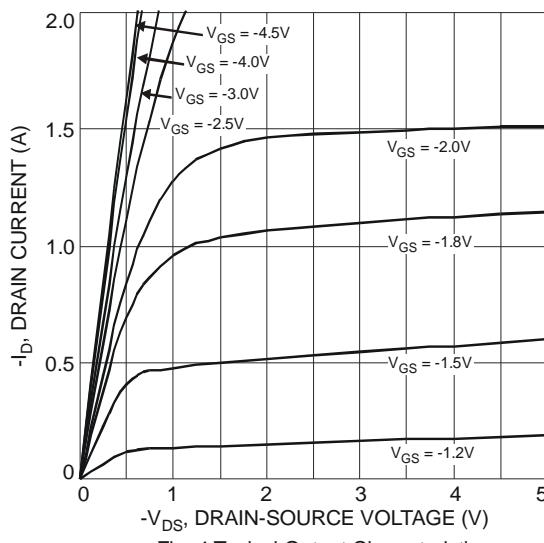


Fig. 4 Typical Output Characteristic

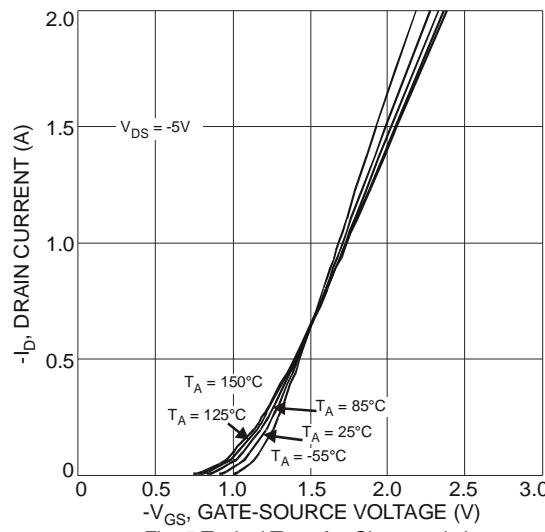


Fig. 5 Typical Transfer Characteristic

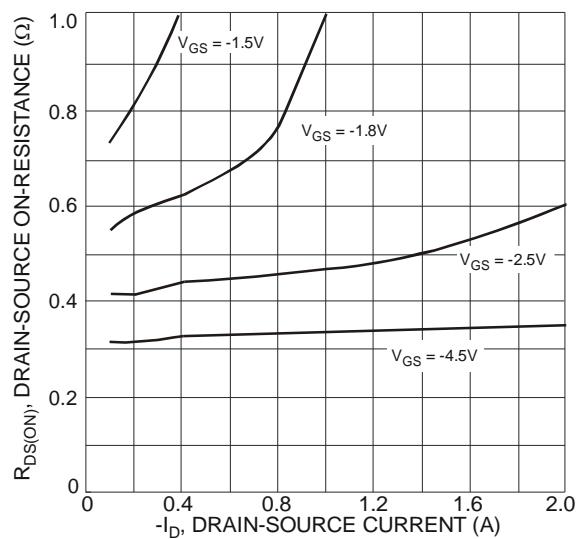


Fig. 6 Typical On-Resistance
vs. Drain Current and Gate Voltage

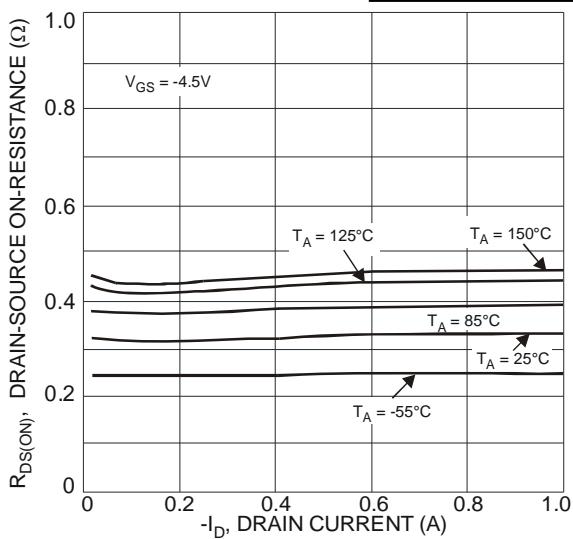


Fig. 7 Typical On-Resistance
vs. Drain Current and Temperature

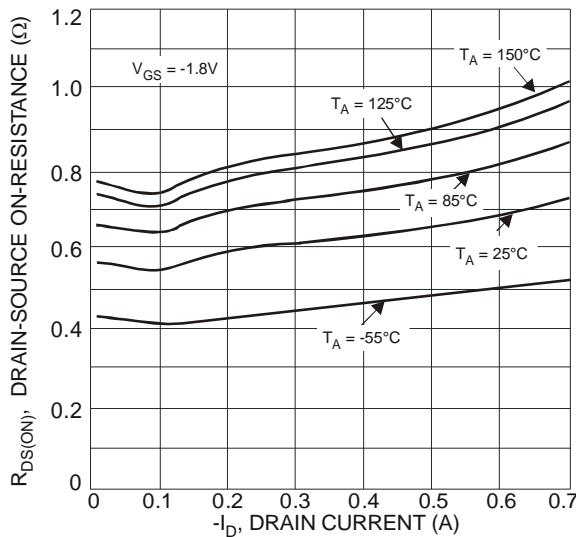


Fig. 8 Typical On-Resistance
vs. Drain Current and Temperature

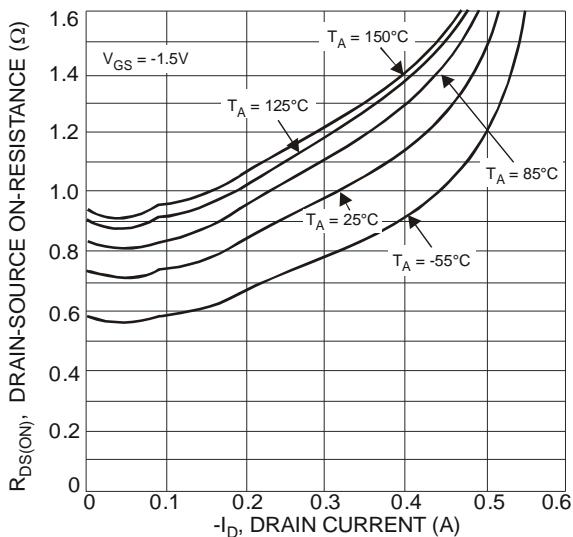


Fig. 9 Typical On-Resistance
vs. Drain Current and Temperature

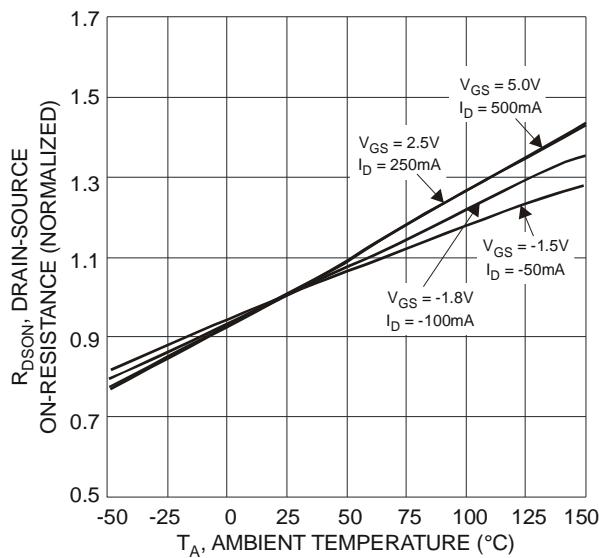


Fig. 10 On-Resistance Variation with Temperature

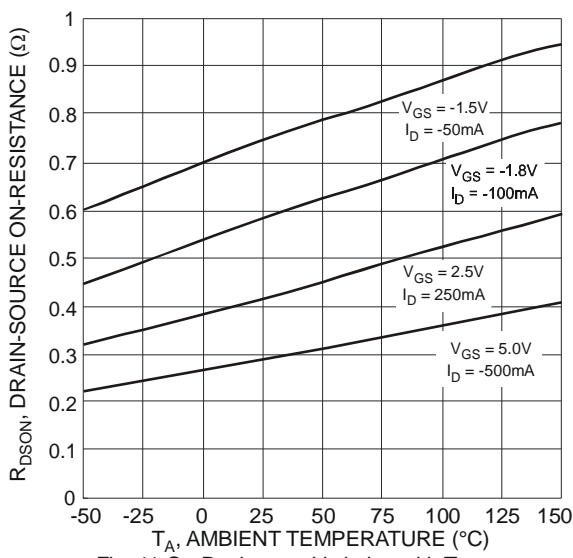


Fig. 11 On-Resistance Variation with Temperature

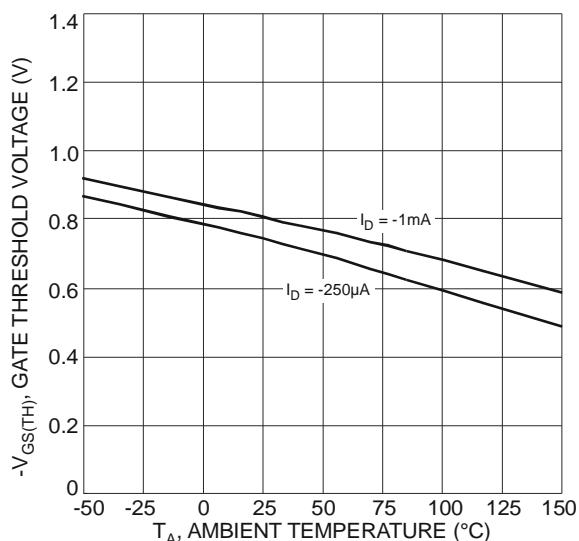


Fig. 12 Gate Threshold Variation vs. Ambient Temperature

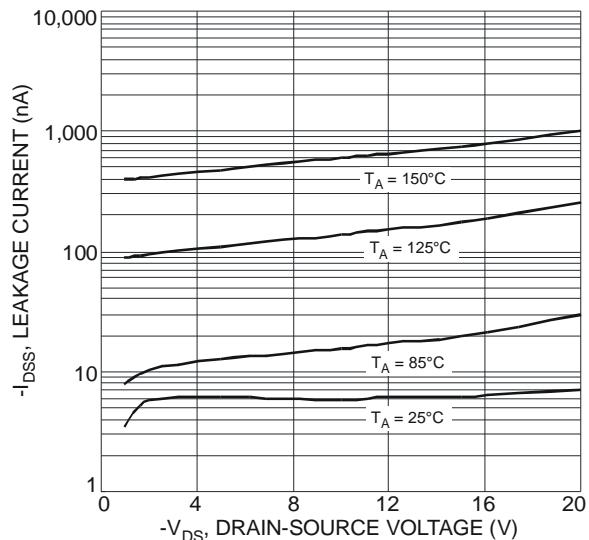


Fig. 14 Typical Leakage Current vs. Drain-Source Voltage

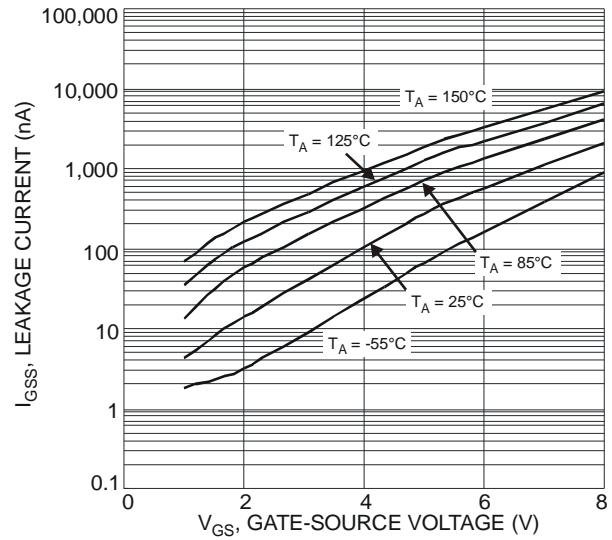


Fig. 16 Leakage Current vs. Gate-Source Voltage

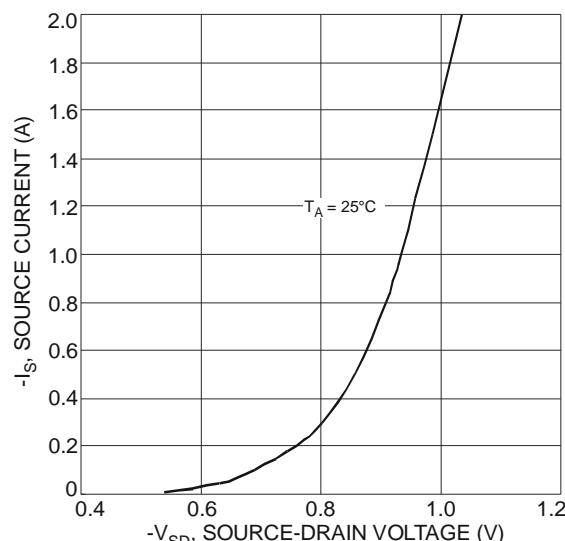


Fig. 13 Diode Forward Voltage vs. Current

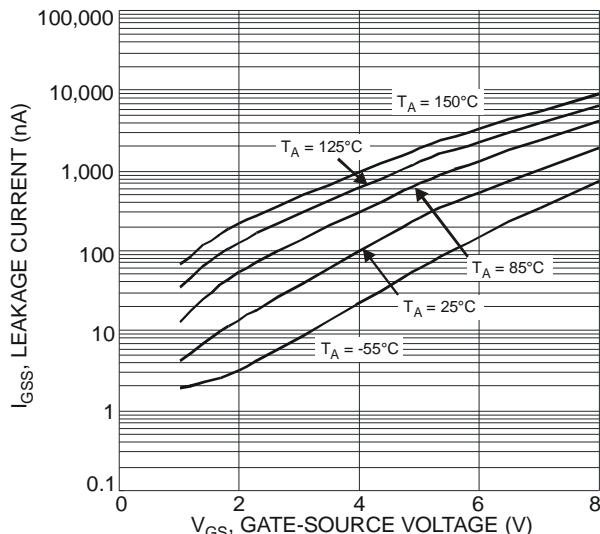


Fig. 15 Leakage Current vs. Gate-Source Voltage

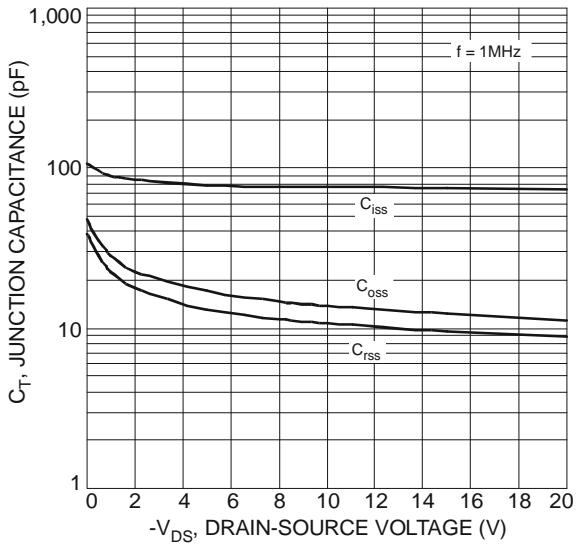


Fig. 17 Typical Junction Capacitance

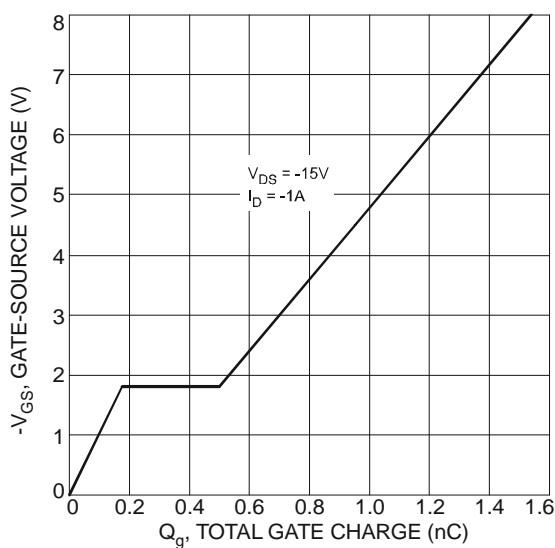
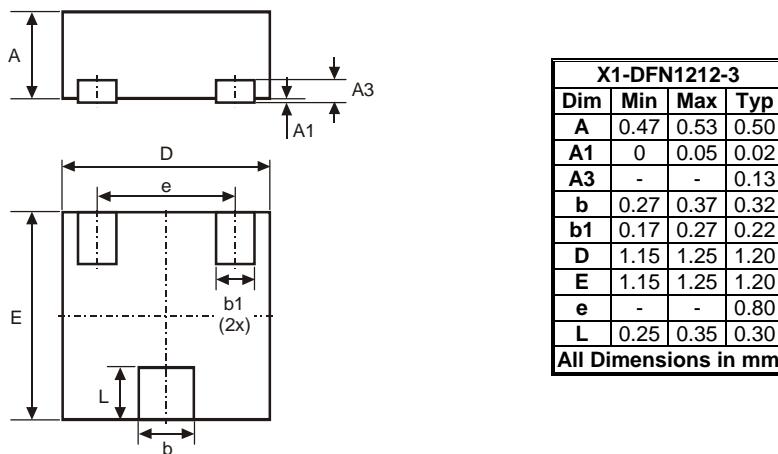
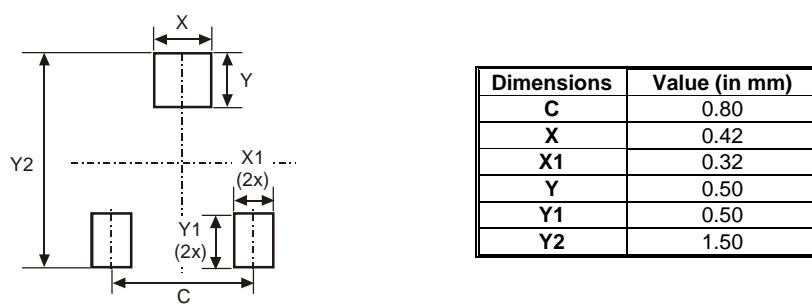


Fig. 18 Gate-Charge Characteristics

Package Outline Dimensions



Suggested Pad Layout



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