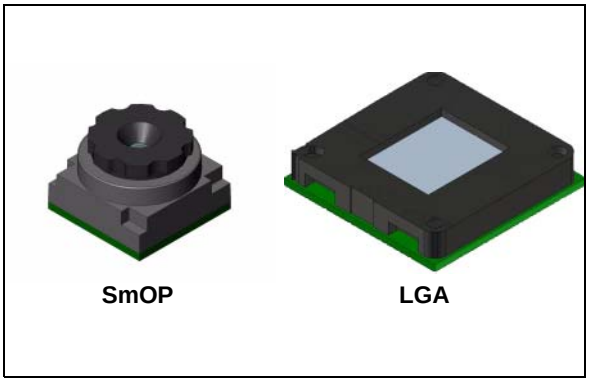
VL6524
VS6524

VGA single-chip camera module

Preliminary Data

Features

- 640H x 480V active pixels
- 3.6 µm pixel size, 1/6 inch optical format
- RGB Bayer color filter array
- Integrated 10-bit ADC
- Integrated digital image processing functions, including defect correction, lens shading correction, demosaic function, sharpening, gamma correction and color space conversion
- Embedded camera controller for automatic exposure control, automatic white balance control, black level compensation, 50/60 Hz flicker cancellation and flashgun support
- Up to 30 fps progressive scan, flexible subsampling and cropping modes
- ITU-R BT.656-4 YUV (YCbCr) 4:2:2 with embedded syncs, RGB 565, RGB 444 or Bayer 10-bit output formats
- Viewlive feature allows different sizes, formats and reconstruction settings to be applied to alternate frames
- 8-bit parallel video interface, horizontal and vertical syncs, 24 MHz clock
- Two-wire serial control interface (I^2C)
- On-chip PLL, 6.5 to 26 MHz clock input
- Analog power supply, from 2.4 V to 3.0 V
- Separate I/O power supply, 1.8 V or 2.8 V levels
- 3.3 V tolerant I/O for power supply > 2.7 V
- Integrated power management with power switch, automatic power-on reset and power-safe pins
- Low power consumption, ultra low standby current
- Dual-element plastic lens, F# 2.8, ~59° DFOV (VS6524)



SmOP **LGA**

Description

The VL6524/VS6524 is a general purpose VGA resolution CMOS color digital camera featuring low size and low power consumption. This complete camera module is ready to connect to camera enabled baseband processors, back-end IC devices or PDA engines.

Applications

- Mobile phone
- Videophone
- Video surveillance
- Medical
- Machine Vision
- Toys
- PDA
- Biometry
- Bar Code Reader
- Lighting Control

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1 Overview

1.1 Description

The VL6524/VS6524 is a VGA resolution CMOS imaging device designed for low power systems.

Video data is output from the VS6524 over an 8-bit parallel bus in RGB, YCbCr or bayer formats and is controlled via an I²C interface.

The VL6524/VS6524 requires an analogue power supply of between 2.4 V to 3.0 V and a digital supply of either 1.8 V or 2.8 V (dependant on interface levels required). An input clock is required in the range 6.5 MHz to 26 MHz.

The device contains an embedded video processor and delivers fully color processed images at up to 30 frames per second. The video processor integrates a wide range of image enhancement functions, designed to ensure high image quality, these include:

- Automatic exposure control
- Automatic white balance
- Lens shading compensation
- Defect correction algorithms
- Demosaic (Bayer to RGB conversion)
- Matrix compensation
- Sharpening
- Gamma correction
- Flicker cancellation

2 Electrical interface

The device has 20 electrical connections as listed in *Table 1*. The physical orientation of the pins on the device is shown in *Figure 36 on page 63*.

Table 1. VL6524/VS6524 signal description

Pad socket	Pad name	I/O	Description
1	GND	PWR	Analogue ground
2	D02	OUT	Data output D2
3	D03	OUT	Data output D3
4	HSYNC	OUT	Horizontal synchronization output
5	VSYNC	OUT	Vertical synchronization output
6	D07	OUT	Data output D7
7	D06	OUT	Data output D6
8	D05	OUT	Data output D5
9	D04	OUT	Data output D4
10	CLK	IN	Clock input - 6.5 MHz to 26 MHz
11	GND	PWR	Digital ground
12	FSO	OUT	Flash output
13	CE	IN	Chip enable signal active HIGH
14	SCL	IN	I²C clock input
15	SDA	I/O	I²C data line
16	AVDD	PWR	Analogue supply 2.4 V to 3.0 V
17	D01	OUT	Data output D1
18	D00	OUT	Data output D0
19	PCLK	OUT	Pixel qualification clock
20	VDD	PWR	Digital supply 1.8 V OR 2.8 V

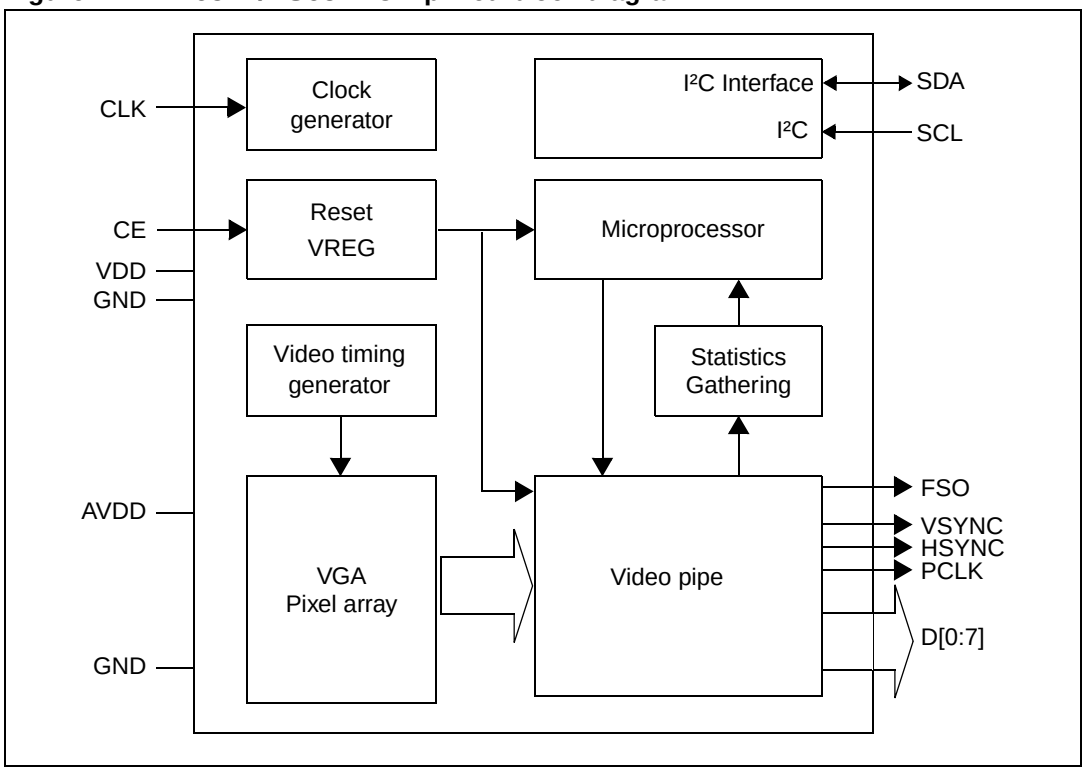
3 System architecture

The VL6524/VS6524 consists of the following main blocks:

- VGA-sized pixel array
- Video timing generator
- Video pipe
- Statistics gathering unit
- Clock generator
- Microprocessor

A simplified block diagram is shown in *Figure 1*.

Figure 1. VL6524/VS6524 simplified block diagram



3.1 Operation

A video timing generator controls a VGA-sized pixel array to produce raw images at up to 30 frames per second. The analogue pixel information is digitized and passed into the video pipe. The video pipe contains a number of different functions (explained in detail later). At the end of the video pipe data is output to the host system over an 8-bit parallel interface along with qualification signals.

The whole system is controlled by an embedded microprocessor that is running firmware stored in an internal ROM. The external host communicates with this microprocessor over an I²C interface. The microprocessor does not handle the video data itself but is able to control all the functions within the video pipe. Real-time information about the video data is gathered by a statistics engine and is available to the microprocessor. The processor uses this information to perform real-time image control tasks such as automatic exposure control.

3.1.1 Video pipe

The main functions contained within the VL6524/VS6524 video processing pipe are as follows.

Gain and offset: This function is used to apply gain and offset to data coming from the sensor array. The required gain and offset values result from the automatic exposure and white balance functions from the microprocessor.

Anti-vignette: This function is used to compensate for the radial roll-off in intensity caused by the lens. By default the anti-vignette setting matches the lens used in this module and does not need to be adjusted.

Crop: This function allows the user to select an arbitrary Window Of Interest (WOI) from the VGA-sized pixel array. It is fully accessible to the user.

Defect correction: This function runs a defect correction filter over the data in order to remove defects from the final output. This function has been optimized to attain the minimum level of defects from the system and does not need to be adjusted.

Demosaic: This module performs an interpolation on the Bayer data from the sensor array to produce an RGB image. It also applies an anti-alias filter.

Subsampler: This module allows the image to be sub-sampled in the X and Y directions by 2, 3, 4, 5 or 6.

Matrix: This function performs a color-space conversion from the sensor RGB data to standard RGB color space.

Sharpening: This module increases the high frequency content of the image in order to compensate for the low-pass filtering effects of the previous modules.

Gamma: This module applies a programmable gain curve to the output data. It is user adjustable.

YUV conversion: This module performs color space conversion from RGB to YUV. It is used to control the contrast and color saturation of the output image as well as the fade to black feature.

Dither: This module is used to reduce the contouring effect seen in RGB images with truncated data.

Output formatter: This module controls the embedded codes which are inserted into the data stream to allow the host system to synchronize with the output data. It also controls the optional HSYNC and VSYNC output signals.

3.2 Microprocessor functions

The microprocessor inside the VL6524/VS6524 performs the following tasks:

Host communication: handles the I²C communication with the host processor.

Video pipe configuration: configures the video pipe modules to produce the output required by the host.

Automatic exposure control: In normal operation the VL6524/VS6524 determines the appropriate exposure settings for a particular scene and outputs correctly exposed images.

Flicker cancellation: The 50/60Hz flicker frequency present in the lighting (due to fluorescent lighting) can be cancelled by the system.

Automatic white balance: The microprocessor adjusts the gains applied to the individual color channels in order to achieve a correctly color balanced image.

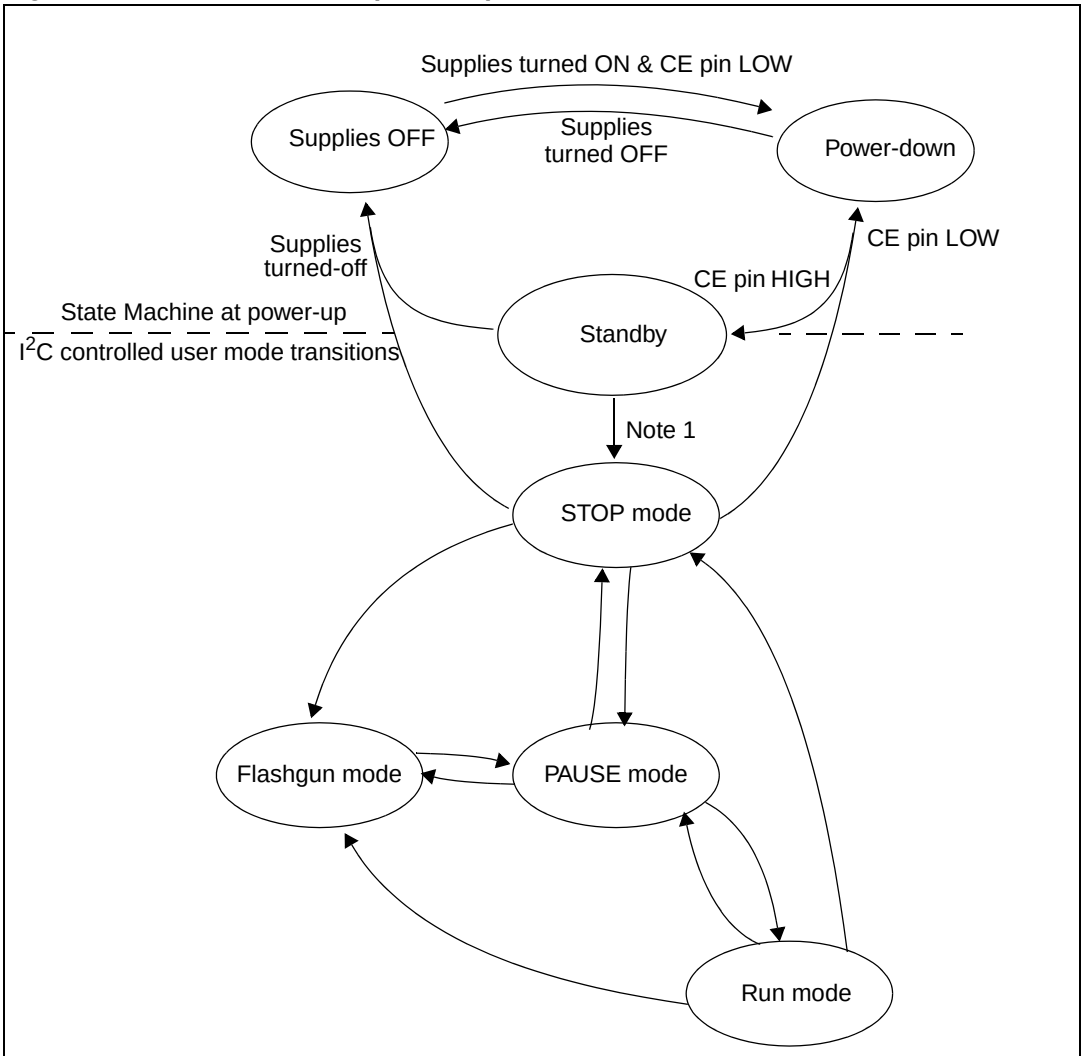
Dark calibration: The microprocessor uses information from special dark lines within the pixel array to apply an offset to the video data and ensure a consistent ‘black’ level.

Active noise management: The microprocessor is able to modify certain video pipe functions according to the current exposure settings determined by the automatic exposure controller. The main purpose of this is to improve the noise level in the system under low lighting conditions. Functions that require a reduction in strength under low lighting conditions (e.g. sharpening) are controlled by ‘dampers’. Functions that require an increase in strength under low lighting conditions are controlled by ‘promoters’. The fade to black operation is also controlled by the microprocessor

4 Operational modes

The VL6524/VS6524 has a number of operational modes. The STANDBY mode is entered and exited by driving the hardware CE signal. Transitions between all other modes are initiated by I²C transactions from the host system or automatically after time-outs.

Figure 2. State machine at power -up and user mode transitions



Note: 1 It is possible to enter any of the user modes direct from Standby via an I2C command

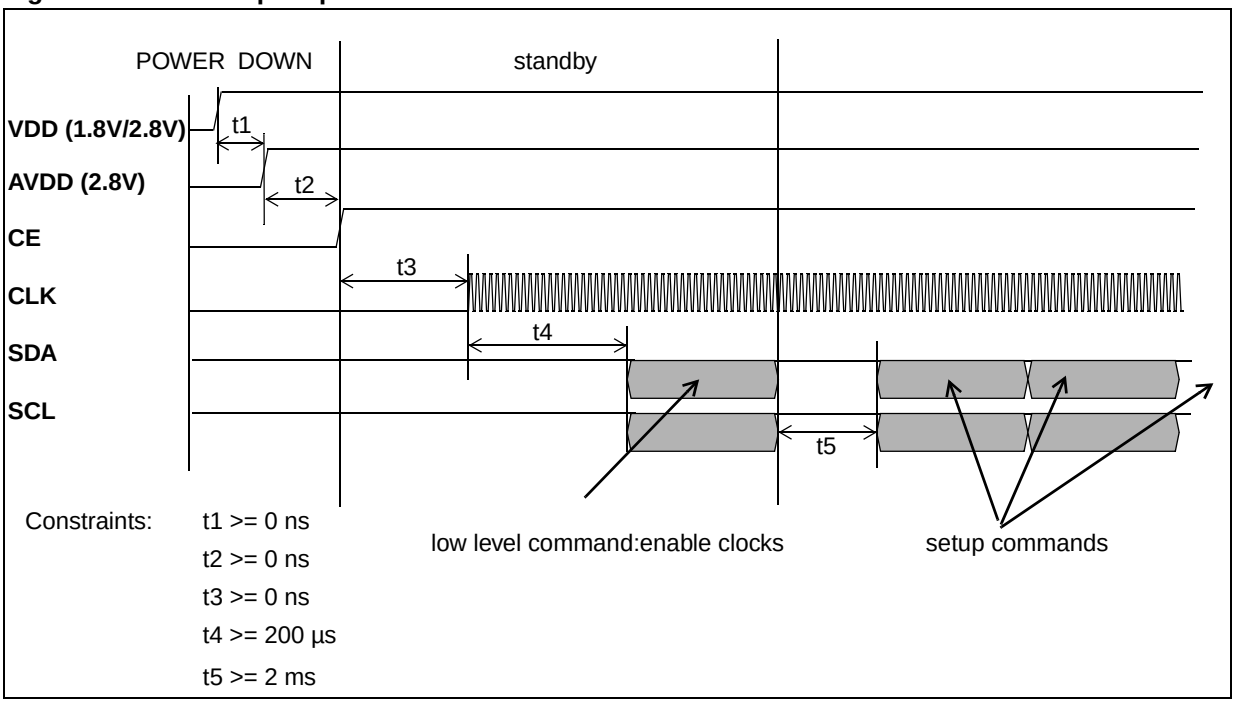
Power Down/Up: The power down state is entered from all other modes when CE is pulled low or the supplies are removed.
During the power-down state (CE = logic 0)

- The internal digital supply of the VL6524/VS6524 is shut down by an internal switch mechanism. This method allows a very low power-down current value.
- The device inputs / outputs are fail-safe, and consequently can be considered high impedance.

During the power-up sequence (CE = logic 1)

- The digital supplies must be on and stable.
- The internal digital supply of the VL6524/VS6524 is enabled by an internal switch mechanism.
- All internal registers are reset to default values by an internal power on reset cell.

Figure 3. Power up sequence



STANDBY mode: The VL6524/VS6524 enters STANDBY mode when the CE pin on the device is pulled HIGH. Power consumption is very low, most clocks inside the device are switched off.
In this state I²C communication is possible when CLK is present and when the microprocessor is enabled by writing the value 0x06 to the *MicroEnable* register 0xC003 (*Table 7 on page 43*).

All registers are reset to their default values. The device I/O pins have a very high-impedance.

Note: On exit from STANDBY mode, the VL6524/VS6524 is in a transient mode called UNINITIALISED, this mode is not a user mode.

STOP mode: This is a low power mode. The analogue section of the VL6524/VS6524 is switched off and all registers are accessed over the I²C interface. A run command received in this state automatically sets a transition through the PAUSE state to the run mode.

PAUSE mode: In this mode all VL6524/VS6524 clocks are running and all registers are accessible but no data is output from the device. The device is ready to start streaming but is halted. This mode is used to set up the required output format before outputting any data.

Note: The PowerManagement register bTimeToPowerdown can be adjusted in PAUSE mode but has no effect until the next RUN to PAUSE transition (Table 13 on page 45).

RUN mode: This is the fully operational mode.

ViewLive: this feature allows different sizes, formats and reconstruction settings to be applied to alternate frames of data, while in run mode.

FLASHGUN mode: In flashgun mode, the array is configured for use with an external flashgun. A flash is triggered and a single frame of data is output and the device automatically switches to Pause Mode.

4.1 Mode transitions

Transitions between operating modes are normally controlled by the host by writing to the *mode control* register (*Section 11.4 on page 43*). Some transitions can occur automatically after a time out. If there is no activity in the PAUSE state then an automatic transition to the STOP state occurs. This function is controlled by the *power management control* register (*Section 11.8 on page 45*). Writing 0xFF disables the automatic transition to STOP mode.

5 Clock control

5.1 Input clock

The VL6524/VS6524 contains an internal PLL allowing it to produce accurate frame rates from a wide range of input clock frequencies. The allowable input range is from 6.5 MHz to 26 MHz. The input clock frequency must be programmed in the *uwExtClockFreqNum (MSB)*, *uwExtClockFreqNum (LSB)* and *bExtClockFreqDen* registers (*Table 12: Clock manager input control on page 44*). To program an input frequency of 6.5 MHz, the numerator can be set to 13 and the denominator to 2. The default input frequency is 12 MHz.

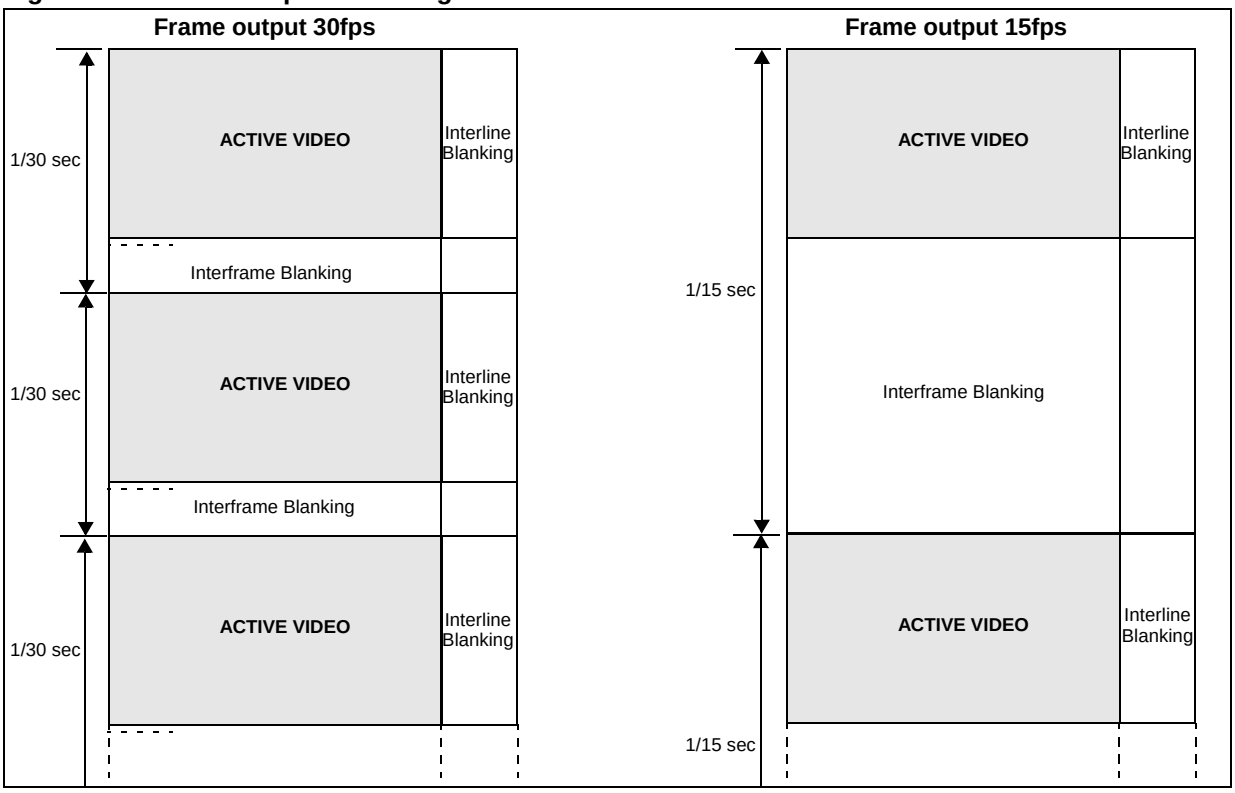
5.2 System clock division

It is possible to set an overall system clock division of 2 in the *bEnableGlobalSystemClockDivision* register (*Table 12: Clock manager input control on page 44*). This results in a PCLK of 12MHz and a maximum frame rate of 15fps VGA.

5.3 Pixel clock (PCLK)

All data output from the VL6524/VS6524 is qualified by the PCLK output. The PCLK frequency is 24 MHz (equivalent to a 12 MHz pixel rate as each pixel is represented by 2 bytes of data). For frame rates less than 30 fps the PCLK frequency is not reduced, instead additional interframe lines are added into the output data stream.

Figure 4. Frame output format against framerate



Similarly when using sub-sampled output modes the PCLK frequency is not reduced but instead pairs of PCLKs are 'dropped', see *Section 6.1.2: Subsampling module* for details.

The PCLK edge used to qualify the output data is fully programmable. It is also possible to program the state of the PCLK line (high or low) for the times when it is inactive.

5.4 PCLK gating

By default the PCLK output from the VL6524/VS6524 is *not* continuous. The PCLK qualifies all video data (and embedded codes if selected) on each video line and each interframe line but does *not* qualify the interline blanking data. In non-subsampled modes the PCLK is continuous *during* the video data output. The operation of the PCLK can be controlled using the *bPClkSetup* register (*Table 29: Output formatter control on page 53*).

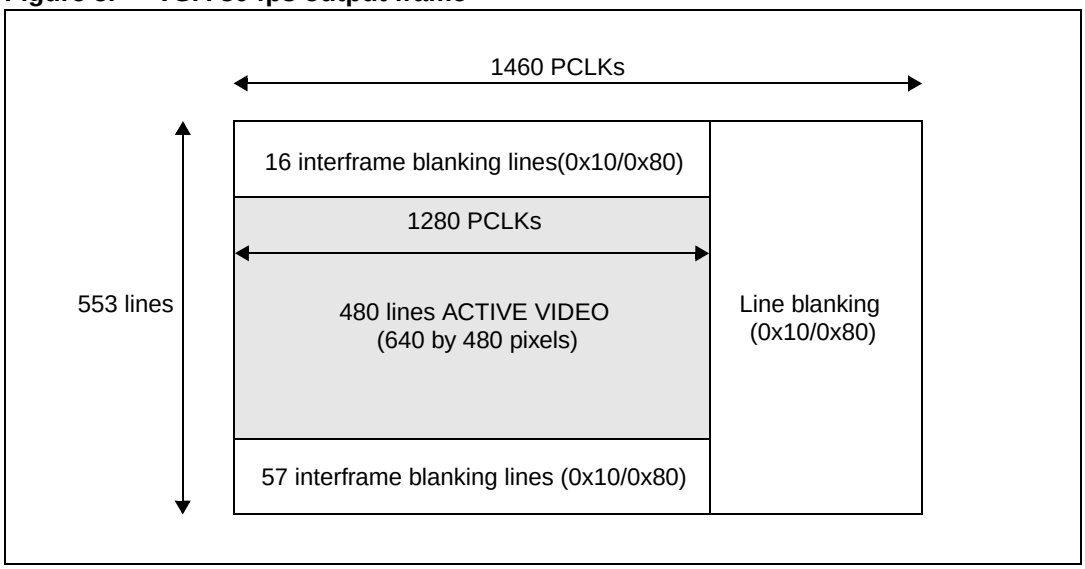
6 Output frame size control

6.1 Frame format

An output frame consists of a number of active lines and a number of interframe lines. Each line consists of embedded line codes (if selected), active pixel data and interline blank data. Note that by default the interline blanking data is *not* qualified by the PCLK and therefore is not captured by the host system.

The default 30 fps VGA output frame is shown in *Figure 5*.

Figure 5. VGA 30 fps output frame



If embedded codes are enabled then 8 additional clocks are required in every line to qualify the codes and 8 fewer interline clocks are output leaving the total constant at 1460 clocks per line.

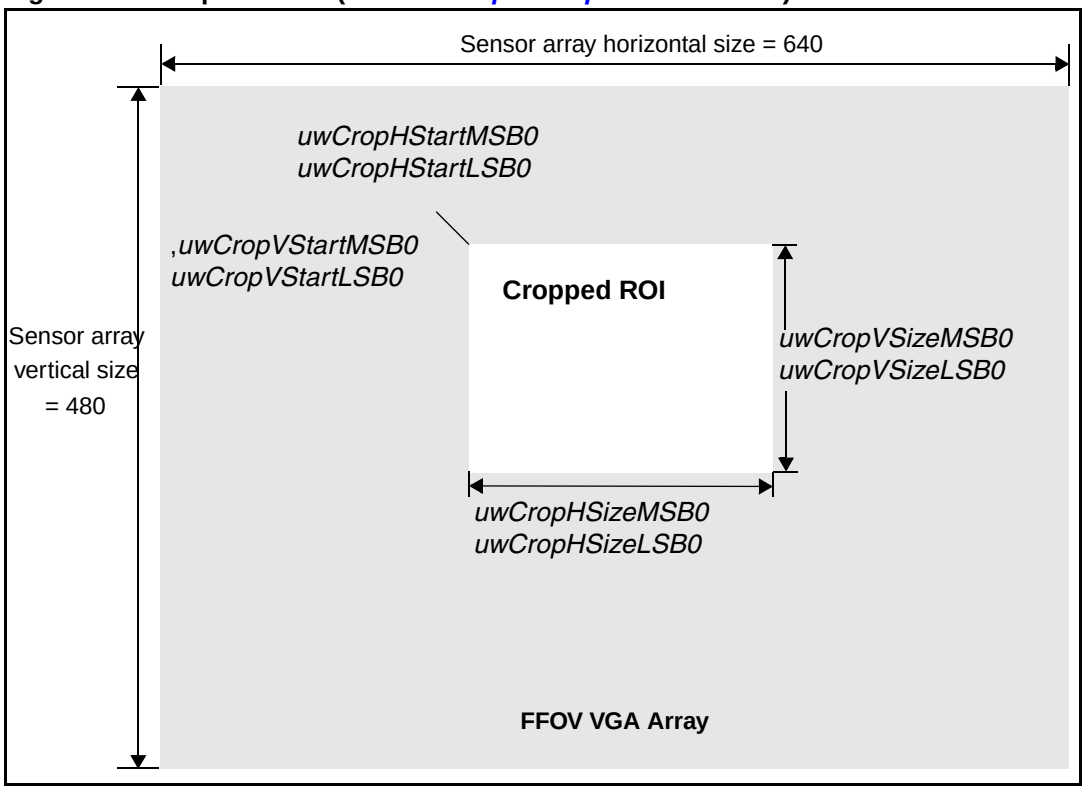
By default the PCLK output does not qualify the line blanking data and so each line contains only 1280 clocks (or 1288 if embedded codes are enabled).

The values which are output during line and frame blanking are an alternating pattern of 0x10 and 0x80 by default. These values can be changed by writing to the BlankData_MSB and BlankData_LSB registers in the *Output formatter control* bank (*Table 29 on page 53*).

6.1.1 Cropping module

The VL6524/VS6524 contains a cropping module which can be used to define a window of interest within the full VGA array size. The user can set a start location and the required output size. *Figure 6* shows the example with pipe setup bank0.

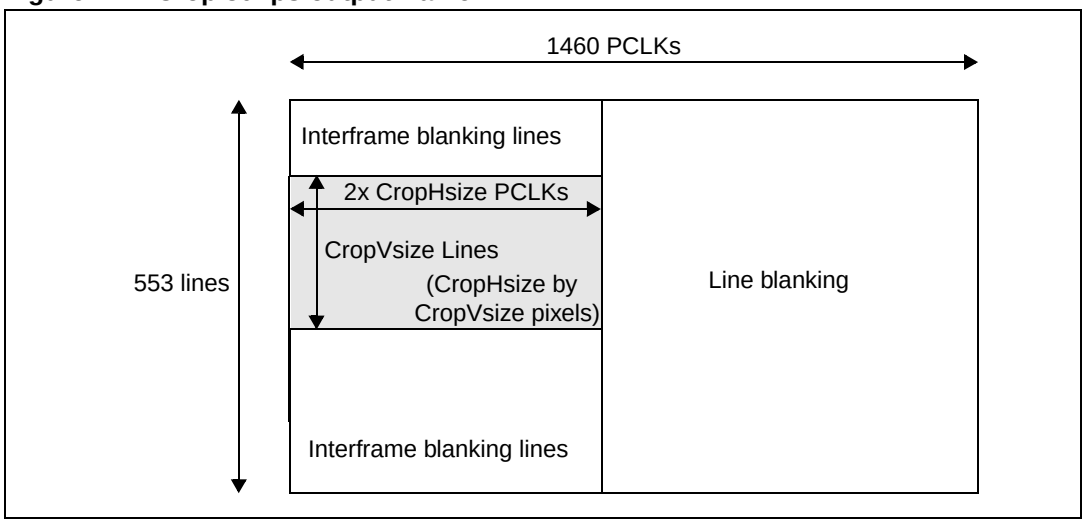
Figure 6. Crop controls (*Table 16: Pipe setup bank0 control*)



Complete lines which fall outside the window of interest are replaced in the output data frame with lines of blanking data thus the overall frame length is *not* reduced.

The portion of the output line which contains video data is reduced in length to contain only those pixels defined by the window of interest. However the *overall* line length remains unchanged as the number of interline clocks increases by the same amount.

Figure 7. Crop 30 fps output frame



6.1.2 Subsampling module

The VL6524/VS6524 has a built in sub-sampler which can divide the image by 1, 2, 3, 4, 5, or 6.

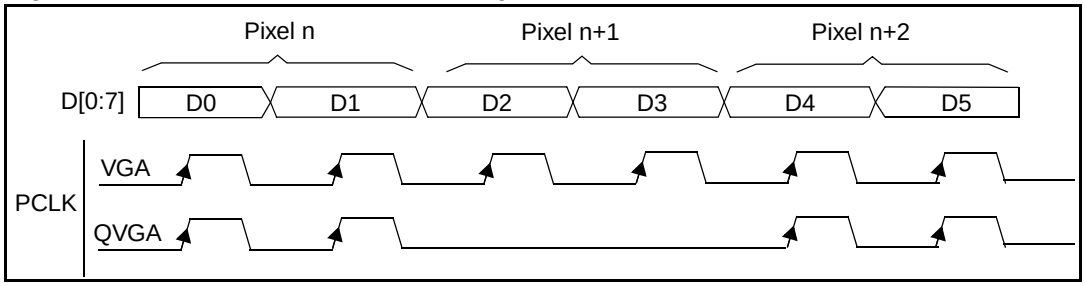
Using the sub-sampler gives output images with reduced resolution but the same field of view as the full VGA image or the region of interest defined in the cropping module. *Table 2* lists the available image sizes.

Table 2. Subsampled image sizes

Subsample ratio	Image format	Image dimensions
1 (default)	VGA	640 by 480
2	QVGA	320 by 240
3	-	213 by 160
4	QQVGA	160 by 120
5	SQCIF	128 by 96
6	-	106 by 80

Subsampled images are produced by 'dropping' PCLKs so that only certain pixels are qualified in the output data stream. The figure below indicates a portion of the PCLK waveform for VGA and QVGA images. The effect of this is that the *time* taken to readout one line of the image remains constant in all subsampled modes - it is just the number of clocks that changes.

Figure 8. PCLK waveform in subsampled modes



It is possible to use the crop module and the sub-sampler together to achieve almost any required image size. When using the crop *and* subsampling functions together then the number of lines in a frame must be an integer multiple of the subsample ratio.

6.2 Frame rate control

The VL6524/VS6524 features an extremely flexible frame rate controller. Using registers *uwDesiredFrame Rate_Num (MSB)*, *uwDesiredFrame Rate_Num (LSB)* and *bDesiredFrameRate_ Den* any desired frame rate between 1 and 30 fps can be selected (see *Table 14 on page 45* for register description). To program a required frame rate of 7.5 fps the numerator can be set to 15 and the denominator to 2. The default frame rate is 30 fps.

Slower frame rates are achieved by adding interframe lines. This results in a longer frame period and therefore a longer period over which integration is possible. Due to the longer

integration time available, slower frame rates have improved performance in low light conditions.

6.2.1 Horizontal mirror and vertical flip

The image data output from the VL6524/VS6524 can be mirrored horizontally or flipped vertically (or both).

These functions are available in the *Pipe setup bank0 control* register bank (*Table 16 on page 45*).

6.3 ViewLive Operation

ViewLive is an option which allows different size, format and image settings to be applied to alternate frames of the output data.

The controls for ViewLive function are found in the *View live control* register bank where the *fEnable* register allows the host to enable or disable the function and the *InitalPipeSetupBank* register selects which pipe setup bank is output first (see *Table 18: View live control on page 48* for register description).

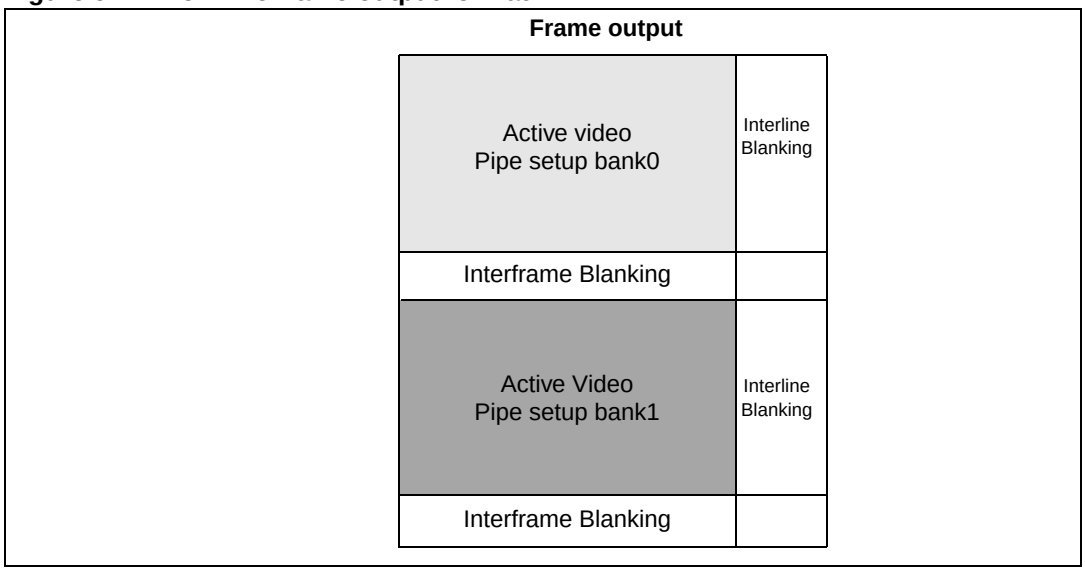
6.3.1 Video pipe setup

The key controls for VL6524/VS6524 video pipe setup are grouped into register banks called *Pipe setup bank0 control* and *Pipe setup bank1 control* (*Section 11.11* and *Section 11.12*).

Pipe setup bank0 control setup is used when ViewLive is disabled.

When ViewLive is enabled the output data switches between *Pipe setup bank0 control* and *Pipe setup bank1 control* on each alternate frame.

Figure 9. ViewLive frame output format



6.4 Context switching

It is possible to control which pipe setup bank is used and to switch between banks without the need to pause streaming, the change will occur at the next frame boundary after the change to the register has been made.

For example this function allows the VL6524/VS6524 to stream an output targeting a display (e.g. RGB 444) and switch to capture an image (e.g. YUV 4:2:2) with no need to pause streaming or enter any other operating mode.

The register *bNonViewLive_ ActivePipeSetupBank* allows selection of the pipe setup bank (*Table 15 on page 45*).

7 Output data formats

The VL6524/VS6524 supports the following data formats:

- YUV4:2:2
- RGB565
- RGB444 (encapsulated as 565)
- RGB444 (zero padded)
- Bayer 10-bit

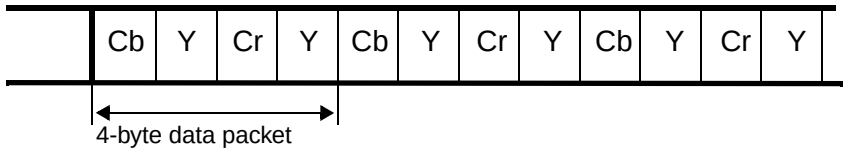
In all output formats there are 2 output bytes per pixel.

The required data format is selected using the *bdataFormat0* register described in *Table 16: Pipe setup bank0 control on page 45*. The various options available for each format are controlled using the *bRgbSetup* and *bYuvSetup* registers (*Table 29: Output formatter control on page 53*).

7.1 YUV 4:2:2 data format

YUV 422 data format requires 4 bytes of data to represent 2 adjacent pixels. ITU601-656 defines the order of the Y, Cb and Cr components as shown in *Figure 10*.

Figure 10. Standard Y Cb Cr data order



The VL6524/VS6524 *bYuvSetup* register (*Table 29: Output formatter control on page 53*) can be programmed to change the order of the components as follows:

Figure 11. Y Cb Cr data swapping options

	Y first	Cb first	Components order in 4-byte data packet 1st	2nd	3rd	4th
	1	1	Y	Cb	Y	Cr
DEFAULT	0	1	Cb	Y	Cr	Y
	1	0	Y	Cr	Y	Cb
	0	0	Cr	Y	Cb	Y

7.2 RGB and Bayer data formats

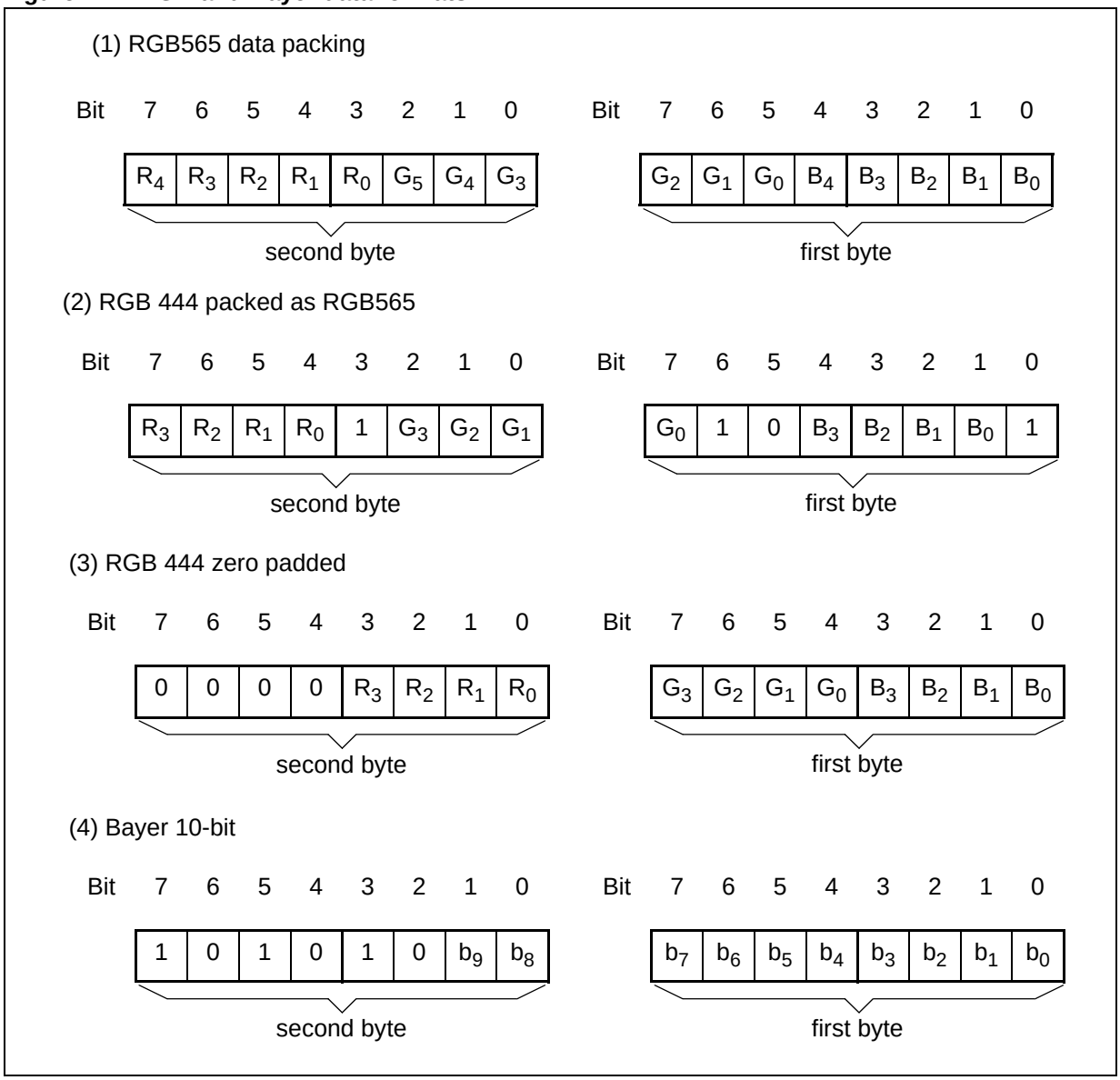
The VL6524/VS6524 can output RGB data in the following formats:

- RGB565
- RGB444 (encapsulated as RGB565)
- RGB444 (zero padded)
- Bayer 10-bit

Note: Pixels in Bayer 10-bit data output are defect corrected, correctly exposed and white balanced. Any or all of these functions can be disabled.

In each of these modes, two bytes of data are required for each output pixel. The encapsulation of the data is shown in *Figure 12*.

Figure 12. RGB and Bayer data formats



7.2.1 Manipulation of RGB data

It is possible to modify the encapsulation of the RGB data in a number of ways:

- swap the location of the RED and BLUE data
- reverse the bit order of the individual color channel data
- reverse the order of the data bytes themselves

7.2.2 Dithering

An optional dithering function can be enabled for each RGB output mode to reduce the appearance of contours produced by RGB data truncation. This is enabled through the *DitherControl* register (*Table 28 on page 52*).

8 Data synchronization methods

External capture systems can synchronize with the data output from VL6524/VS6524 in one of two ways:

1. Synchronization codes are embedded in the output data
2. Via the use of two additional synchronization signals: VSYNC and HSYNC

Both methods of synchronization can be programmed to meet the needs of the host system.

8.1 Embedded codes

The embedded code sequence can be inserted into the output data stream to enable the external host system to synchronize with the output frames. The code consists of a 4-byte sequence starting with 0xFF, 0x00, 0x00. The final byte in the sequence depends on the mode selected.

Two types of embedded codes are supported by the VL6524/VS6524: Mode 1 (ITU656) and Mode 2. The *bSyncCodeSetup* register is used to select whether codes are inserted or not and to select the type of code to insert (*Table 29: Output formatter control on page 53*).

When embedded codes are selected each line of data output contains 8 additional clocks: 4 before the active video data and 4 after it.

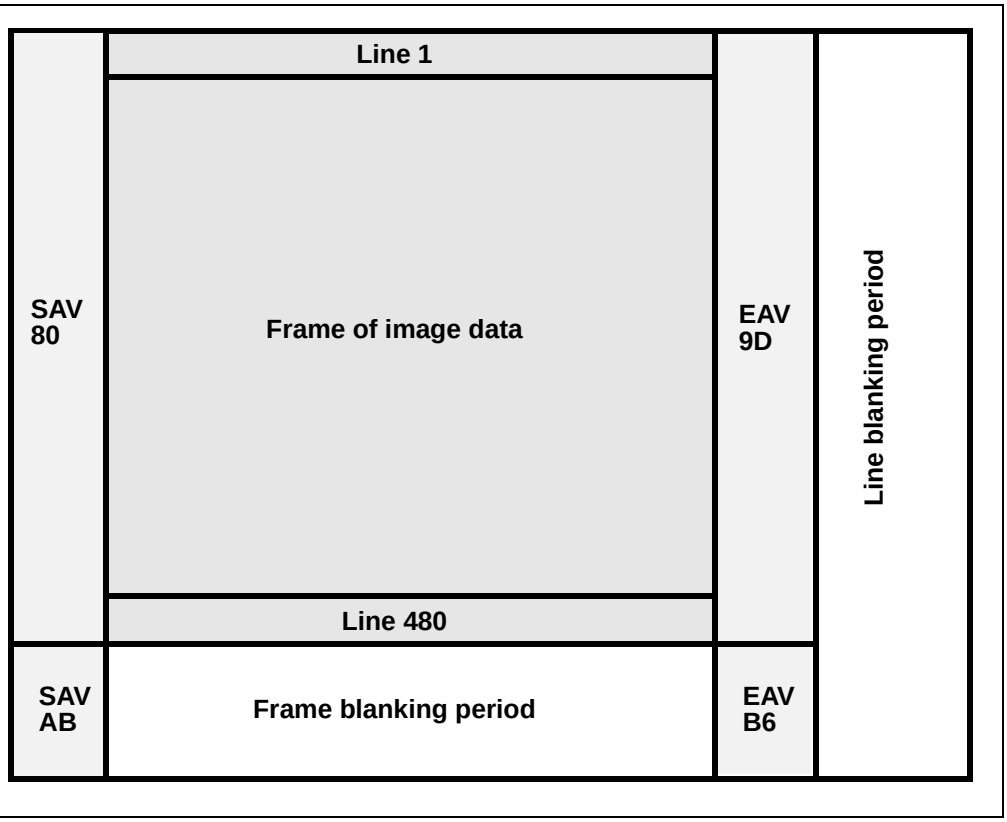
8.1.1 Prevention of false synchronization codes

The VL6524/VS6524 is able to prevent the output of 0xFF and/or 0x00 data from being misinterpreted by a host system as the start of synchronization data. This function is controlled the *bCodeCheckEnable* register (*Table 29: Output formatter control on page 53*).

8.1.2 Mode 1(ITU656 compatible)

The structure of an image frame with ITU656 codes is shown in *Figure 13*.

Figure 13. ITU656 frame structure with even codes



The synchronization codes for odd and even frames are listed in *Table 3 on page 27* and *Table 4 on page 28*. By default all frames output from the VL6524/VS6524 are EVEN. It is possible to set all frames to be ODD or to alternate between ODD and EVEN using the *SyncCodeSetup* register in the *Output formatter control* register bank (*Section 11.24 on page 53*).

Table 3. ITU656 embedded synchronization code definition (even frames)

Name	Description	4-byte sequence
SAV	Line start - active	FF 00 00 80
EAV	Line end - active	FF 00 00 9D
SAV (blanking)	Line start - blanking	FF 00 00 AB
EAV (blanking)	Line end - blanking	FF 00 00 B6

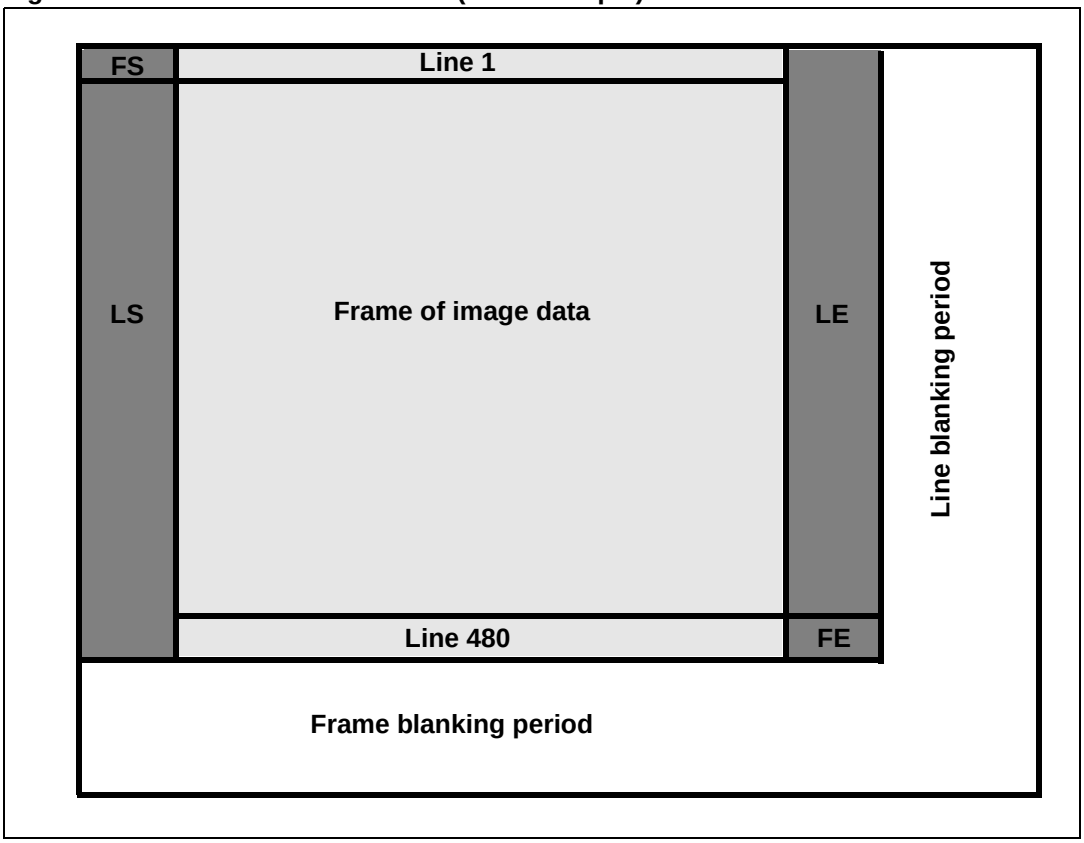
8.1.3 Mode 2

Table 4. ITU656 embedded synchronization code definition (odd frames)

Name	Description	4-byte sequence
SAV	Line start - active	FF 00 00 C7
EAV	Line end - active	FF 00 00 DA
SAV (blanking)	Line start - blanking	FF 00 00 EC
EAV (blanking)	Line end - blanking	FF 00 00 F1

The structure of a mode 2 image frame is shown *Figure 14*.

Figure 14. Mode 2 frame structure (VGA example)



For mode 2, the synchronization codes are as listed in *Table 5*.

Table 5. Mode 2 - embedded synchronization code definition

Name	Description	4-byte sequence
LS	Line start	FF 00 00 00
LE	Line end	FF 00 00 01
FS	Frame Start	FF 00 00 02
FE	Frame End	FF 00 00 03

8.2 VSYNC and HSYNC

The VL6524/VS6524 can provide two programmable hardware synchronization signals: VSYNC and HSYNC. The position of these signals within the output frame can be programmed by the user or an automatic setting can be used where the signals track the active video portion of the output frame regardless of its size.

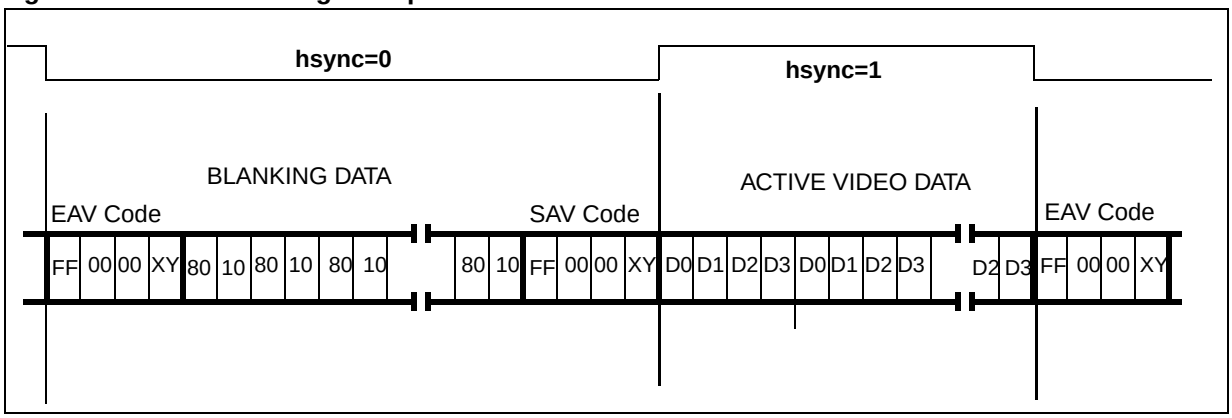
8.2.1 Horizontal synchronization signal (HSYNC)

The HSYNC signal is controlled by the *bHSyncSetup* register (*Table 29: Output formatter control on page 53*). The following options are available:

- enable/disable
- select polarity
- all lines or active lines only
- manual or automatic

In automatic mode the HSYNC signal envelops all the active video data on every line in the output frame regardless of the programmed image size. Line codes (if selected) fall outside the HSYNC envelope as shown in *Figure 15*.

Figure 15. HSYNC timing example



If manual mode is selected then the pixel positions for HSYNC rising edge and falling edge are programmable. The pixel position for the rising edge of HSYNC is programmed in the *bHsyncRisingH*, *bHsyncRisingL* registers. The pixel position for the falling edge of HSYNC is programmed in the *bHsyncFallingH* and *bHsyncFallingL* registers (*Table 29: Output formatter control on page 53*).

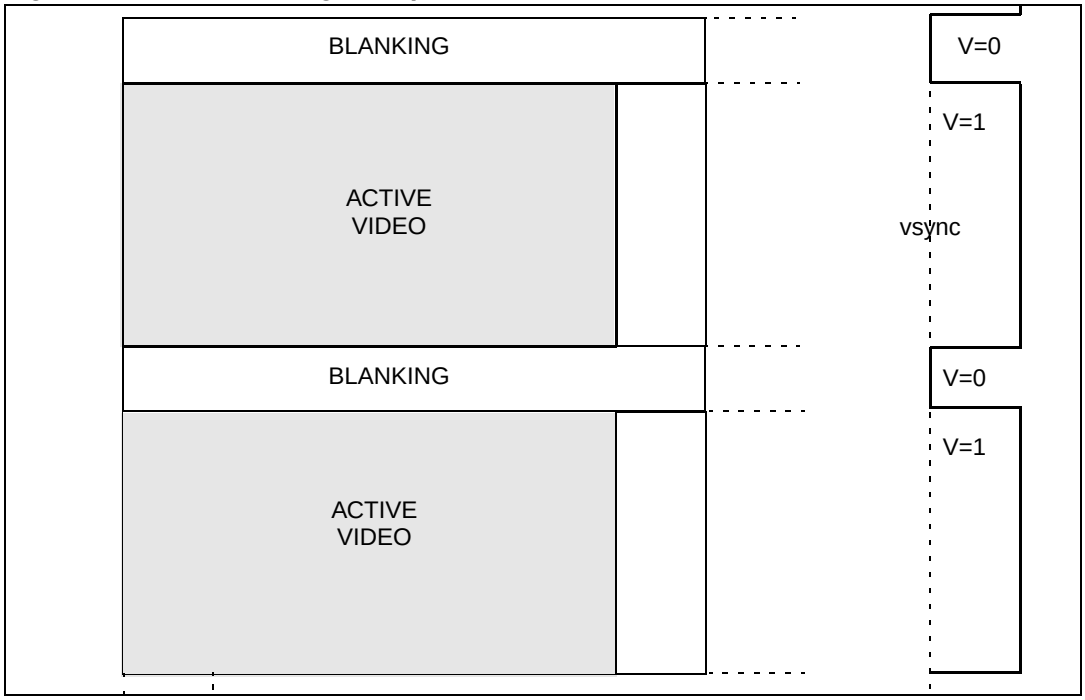
8.2.2 Vertical synchronization (VSYNC)

The VSYNC signal is controlled by the *bVSyncSetup* register. The following options are available:

- enable/disable
- select polarity
- manual or automatic

In automatic mode the VSYNC signal envelops all the active video lines in the output frame regardless of the programmed image size as shown in *Figure 16*.

Figure 16. VSYNC timing example



If manual mode is selected then the line number for VSYNC rising edge and falling edge is programmable. The rising edge of VSYNC is programmed in the *bVsyncRisingLineH*, *bVsyncRisingLineL* registers, the pixel position for VSYNC rising edge is programmed in the *bVsyncRisingPixelH* and *bVsyncRisingPixelL* registers. Similarly the line count for the falling edge position is specified in the *bVsyncFallingLineH* and *bVsyncFallingLineL* registers, and the pixel count is specified in the *bVsyncFallingPixelH* and *bVsyncFallingPixelL* registers described in *Table 29: Output formatter control on page 53*.

9 Getting started

9.1 Initial power up

Before any communication is possible with the VL6524/VS6524 the following steps must take place:

1. Apply VDD (1.8V or 2.8V)
2. Apply AVDD (2.8V)
3. Assert CE line HIGH
4. Apply an external CLOCK (6.5 MHz to 26 MHz)

These steps can all take place simultaneously. After these steps are complete a delay of 200 µs is required before any I²C communication can take place, see *Figure 3: Power up sequence on page 14*.

9.2 Minimum startup command sequence

1. Enable the microprocessor - before any commands can be sent to the VL6524/VS6524, the internal microprocessor must be enabled by writing the value 0x06 to the *MicroEnable* register 0xC003 (*Table 7: Low-level control registers on page 43*).
2. Enable the digital I/O - after power up the digital I/O of the VL6524/VS6524 is in a high-impedance state ('tri-state'). The I/O are enabled by writing the value 0x01 to the *Enable I/O* register 0xC034 (*Table 7: Low-level control registers on page 43*).
3. The user can then program the system clock frequency and setup the required output format before placing the VL6524/VS6524 in RUN mode by writing 0x02 to the *bUserCommand* register 0x0180 (*Table 9: Mode control on page 43*).

The above three commands represent the absolute minimum required to get video data output.

The default configuration results in an output of VGA, 30 fps, YUV data format with ITU embedded codes requiring a external clock frequency of 12 MHz.

In practice the user is likely to require to write some additional setup information prior to receiving the required data output.

10 Host communication - I²C control interface

The interface used on the VL6524/VS6524 is a subset of the I²C standard. Higher level protocol adaptations have been made to allow for greater addressing flexibility. This extended interface is known as the V2W interface.

10.1 V2W protocol layer

10.1.1 Protocol

A message contains two or more bytes of data preceded by a START (S) condition and followed by either a STOP (P) or a repeated START (Sr) condition followed by another message.

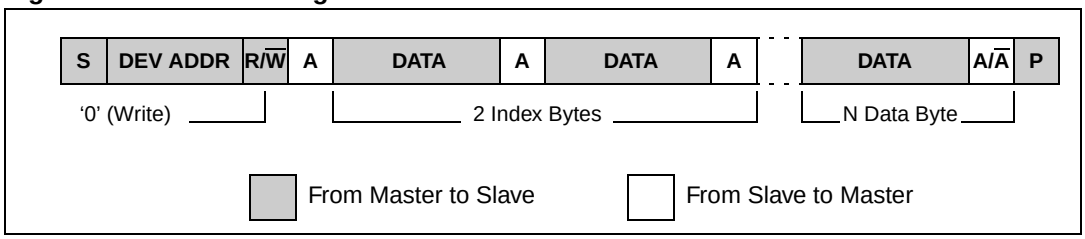
STOP and START conditions can only be generated by a V2W master.

After every byte transferred the receiving device must output an acknowledge bit which tells the transmitter if the data byte has been successfully received or not.

The first byte of the message is called the device address byte and contains the 7-bit address of the V2W slave to be addressed plus a read/write bit which defines the direction of the data flow between the master and the slave.

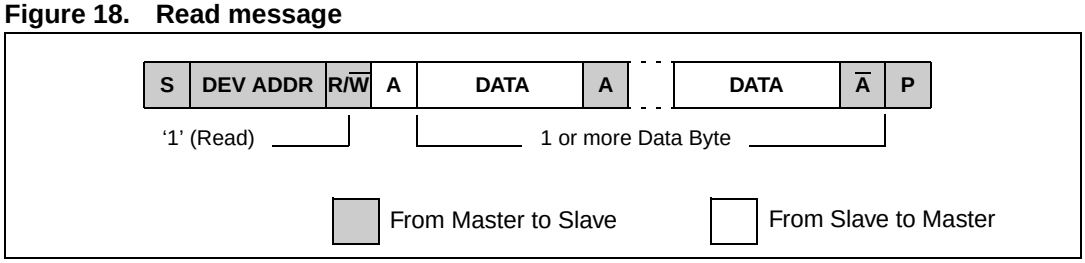
The meaning of the data bytes that follow the device address changes, depending whether the master is writing to or reading from the slave.

Figure 17. Write message



For the master writing to the slave, the device address byte is followed by 2 bytes which specify the 16-bit internal location (index) for the data write. The next byte of data contains the value to be written to that register index. If multiple data bytes are written then the internal register index is automatically incremented after each byte of data transferred. The master can send data bytes continuously to the slave until the slave fails to provide an acknowledge or the master terminates the write communication with a STOP condition or sends a repeated START (Sr).

Figure 18. Read message

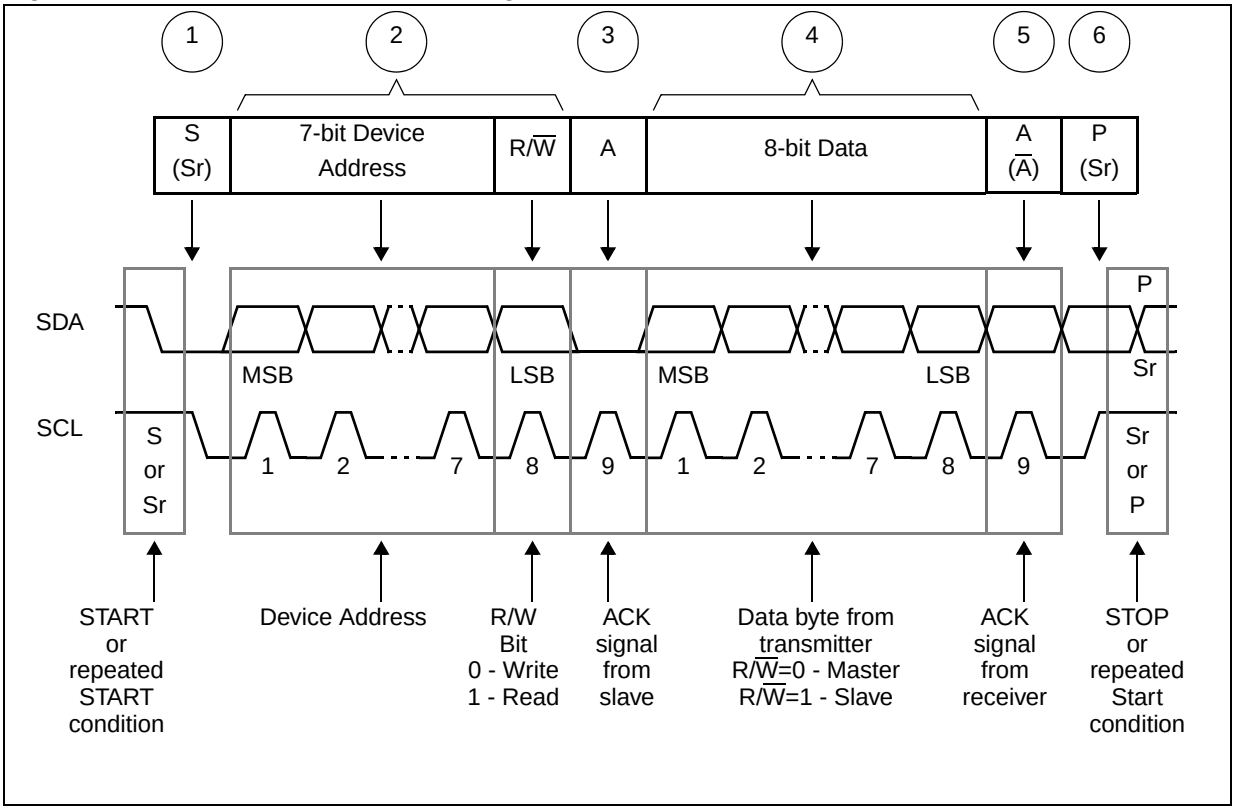


For the master reading from the slave, the device address is followed by the contents of the last register index that the previous read or write message accessed. If multiple data bytes are read then the internal register index is automatically incremented after each byte of data read. A read message is terminated by the bus master generating a negative acknowledge after reading a final byte of data.

A message can only be terminated by the bus master, either by issuing a stop condition, a repeated start condition or by a negative acknowledge after reading a complete byte during a read operation.

10.1.2 Detailed overview of the message format

Figure 19. Detailed overview of message format



The V2W generic message format consists of the following sequence

1. Master generates a START condition to signal the start of new message.
2. Master outputs, MS bit first, a 7-bit device address of the slave the master is trying to communicate with followed by a R/$\overline{W}$ bit.

Figure 20. Device addresses

Sensor Address	0	0	1	0	0	0	0	R/$\overline{W}$
Sensor write Address 20_H	0	0	1	0	0	0	0	0
Sensor read Address 21_H	0	0	1	0	0	0	0	1

a) R/$\overline{W}$ = 0 then the master (transmitter) is writing to the slave (receiver).

b) R/$\overline{W}$ = 1 the master (receiver) is reading from the slave (transmitter).

3. The addressed slave acknowledges the device address.
4. Data transmitted on the bus
   a) When a write is performed, the master outputs 8-bits of data on SDA (MS Bit first).
   b) When a read is performed, the slave outputs 8-bits of data on SDA (MS Bit First).
5. Data receive acknowledge
   a) When a write is performed, the slave acknowledges data.
   b) When a read is performed, the master acknowledges data.

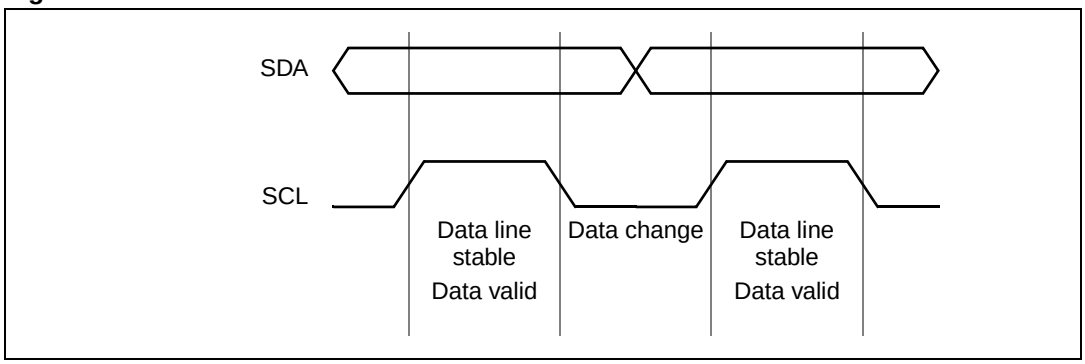
- Repeat 4 and 5 until all the required data has been written or read.
- Minimum number of data bytes for a read =1 (Shortest Message length is 2-bytes).
- The master outputs a negative acknowledge for the data when reading the last byte of data. This causes the slave to stop the output of data and allows the master to generate a STOP condition.

6. Master generates a STOP condition or a repeated START.

10.1.3 Data valid

The data on SDA is stable during the high period of SCL. The state of SDA is changed during the low phase of SCL. The only exceptions to this are the start (S) and stop (P) conditions as defined below. (See also *Figure 33: Timing specification on page 61* and *Table 38: Timing specification on page 60*.)

Figure 21. SDA data valid



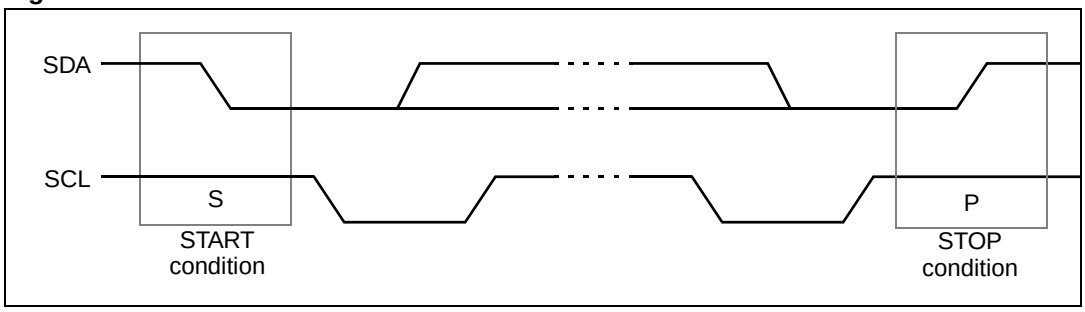
10.1.4 Start (S) and Stop (P) conditions

A START (S) condition defines the start of a V2W message. It consists of a high to low transition on SDA while SCL is high.

A STOP (P) condition defines the end of a V2W message. It consists of a low to high transition on SDA while SCL is high.

After STOP condition the bus is considered free for use by other devices. If a repeated START (Sr) is used instead of a stop then the bus stays busy. A START (S) and a repeated START (Sr) are considered to be functionally equivalent.

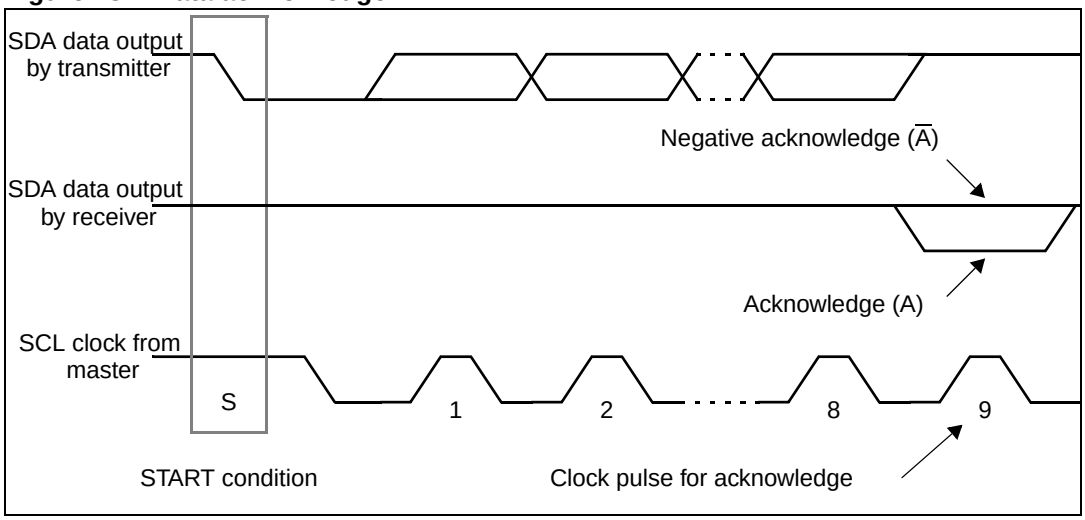
Figure 22. START and STOP conditions



10.1.5 Acknowledge

After every byte transferred the receiver must output an acknowledge bit. To acknowledge the data byte receiver pulls SDA during the 9th SCL clock cycle generated by the master. If SDA is not pulled low then the transmitter stops the output of data and releases control of the bus back to the master so that it can either generate a STOP or a repeated START condition.

Figure 23. Data acknowledge

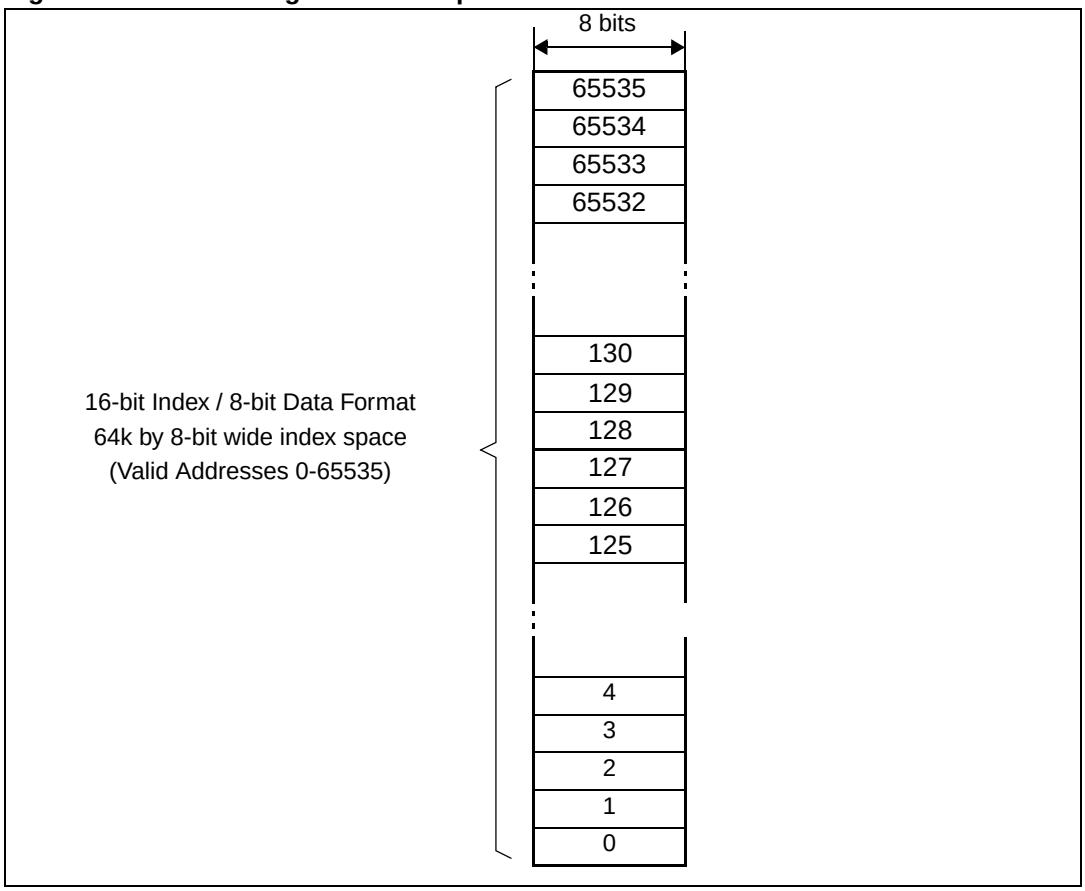


10.1.6 Index space

Communication using the serial bus centres around a number of registers internal to either the sensor or the co-processor. These registers store sensor status, set-up, exposure and system information. Most of the registers are read/write allowing the receiving equipment to change their contents. Others (such as the chip id) are read only.

The internal register locations are organized in a 64k by 8-bit wide space. This space includes “real” registers, SRAM, ROM and/or micro controller values.

Figure 24. Internal register index space



10.1.7 Types of message

This section gives guidelines on the basic operations to read data from and write data to VL6524/VS6524.

The serial interface supports variable length messages. A message contains no data bytes or one data byte or many data bytes. This data can be written to or read from common or different locations within the sensor. The range of instructions available are detailed below.

Single location, single byte data read or write.

Write no data byte. Only sets the index for a subsequent read message.

Multiple location, multiple data read or write for fast information transfers.

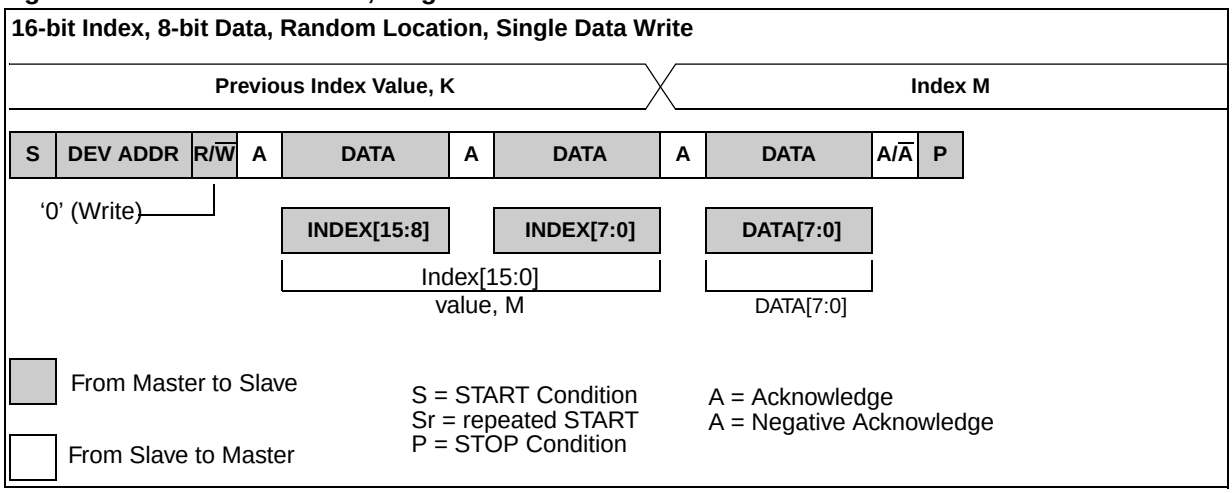
Any message formats other than those specified in the following section should be considered illegal.

10.1.8 Random location, single data write

For the master writing to the slave the R/$\overline{W}$ bit is set to zero.

The register index value written is preserved and is used by a subsequent read. The write message is terminated with a stop condition from the master.

Figure 25. Random location, single write



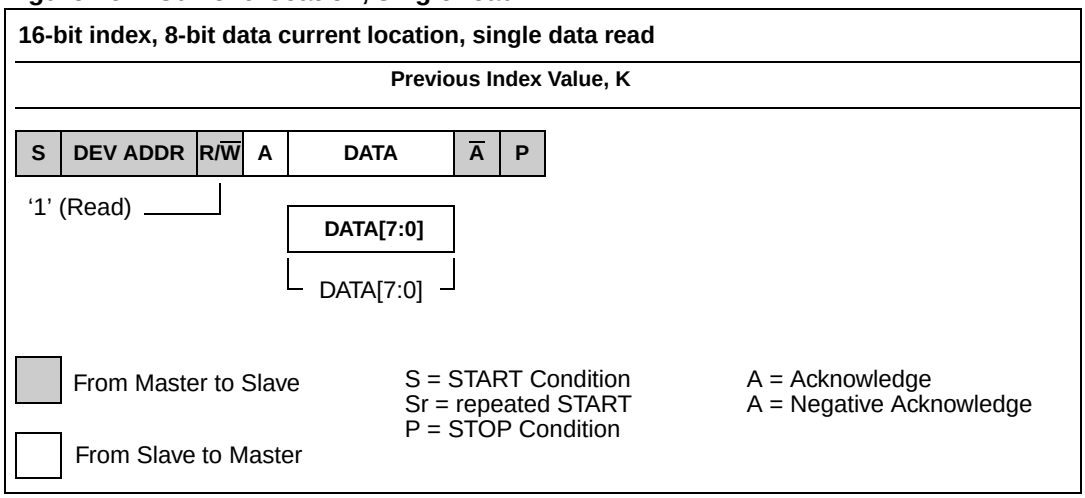
10.1.9 Current location, single data read

For the master reading from the slave the R/$\overline{W}$ bit is set to one. The register index of the data returned is that accessed by the previous read or write message.

The first data byte returned by a read message is the contents of the internal index value and NOT the index value. This was the case in older V2W implementations.

Note that the read message is terminated with a negative acknowledge ($\overline{A}$) from the master: it is not guaranteed that the master will be able to issue a stop condition at any other time during a read message. This is because if the data sent by the slave is all zeros, the SDA line cannot rise, which is part of the stop condition.

Figure 26. Current location, single read

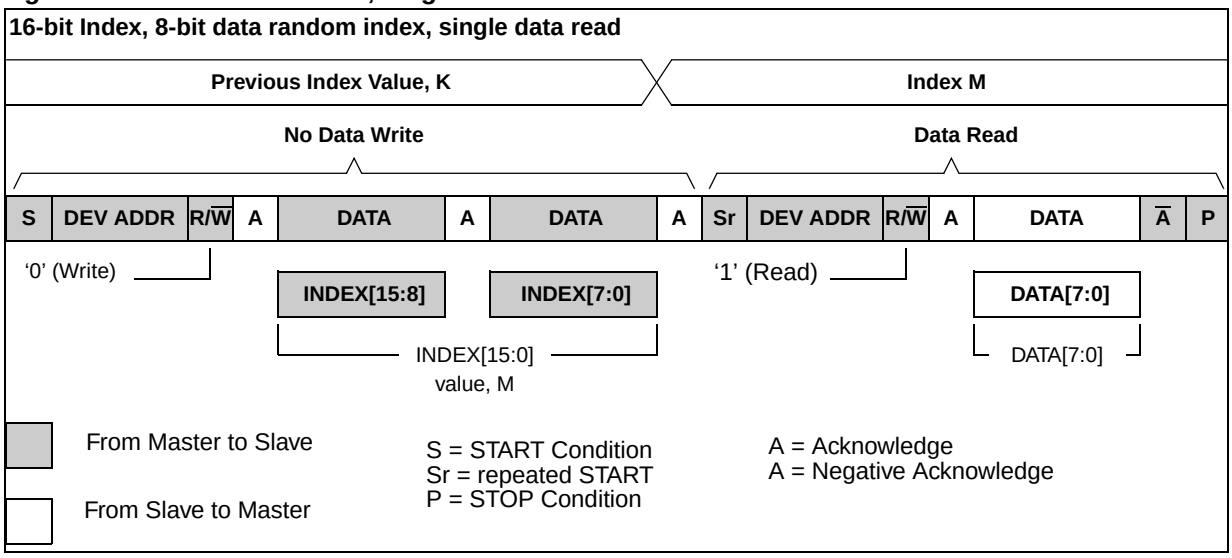


10.1.10 Random location, single data read

When a location is to be read, but the value of the stored index is not known, a write message with no data byte must be written first, specifying the index. The read message then completes the message sequence. To avoid relinquishing the serial to bus to another master a repeated start condition is asserted between the write and read messages.

As mentioned in the previous example, the read message is terminated with a negative acknowledge ($\overline{A}$) from the master.

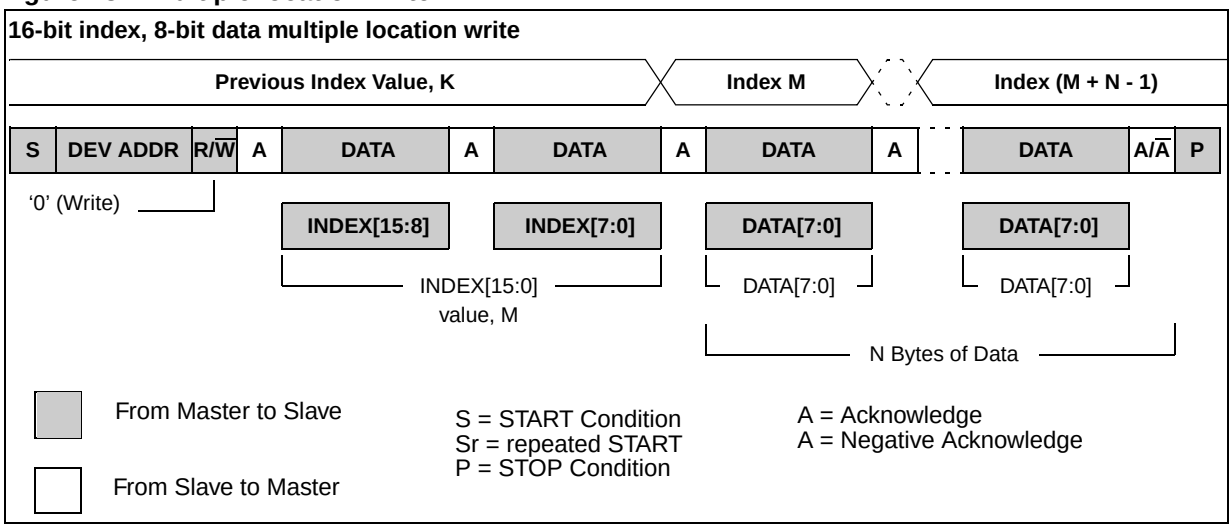
Figure 27. Random location, single data read



10.1.11 Multiple location write

For messages with more than 1 data byte the internal register index is automatically incremented for each byte of data output, making it possible to write data bytes to consecutive adjacent internal registers without having to send explicit indexes prior to sending each data byte.

Figure 28. Multiple location write



10.1.12 Multiple location read stating from the current location

In the same manner as with multiple location writes, multiple locations can be read with a single read message.

Figure 29. Multiple location read

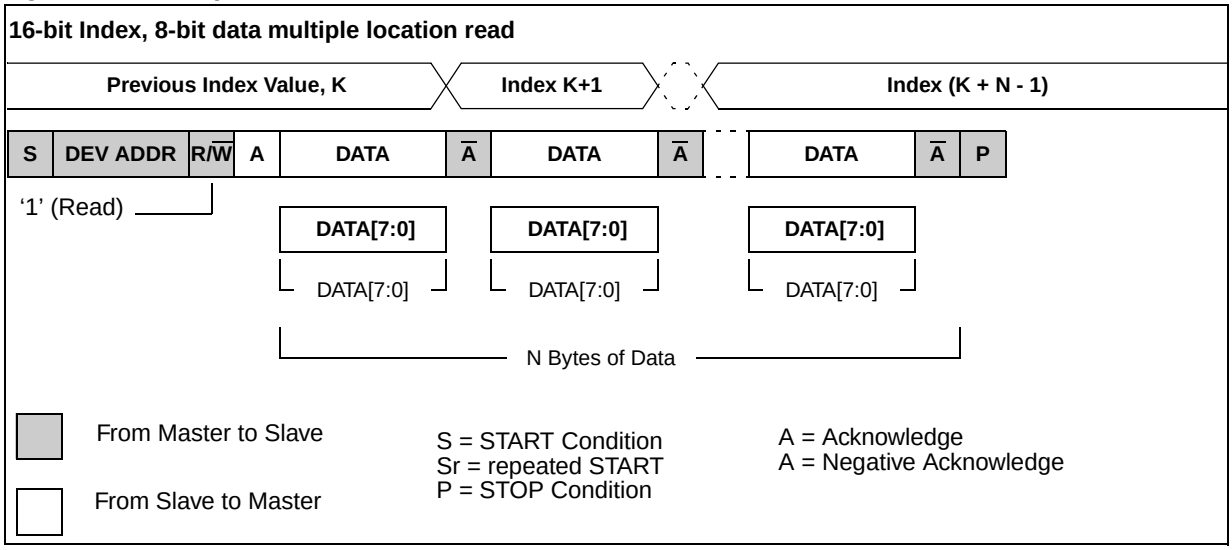
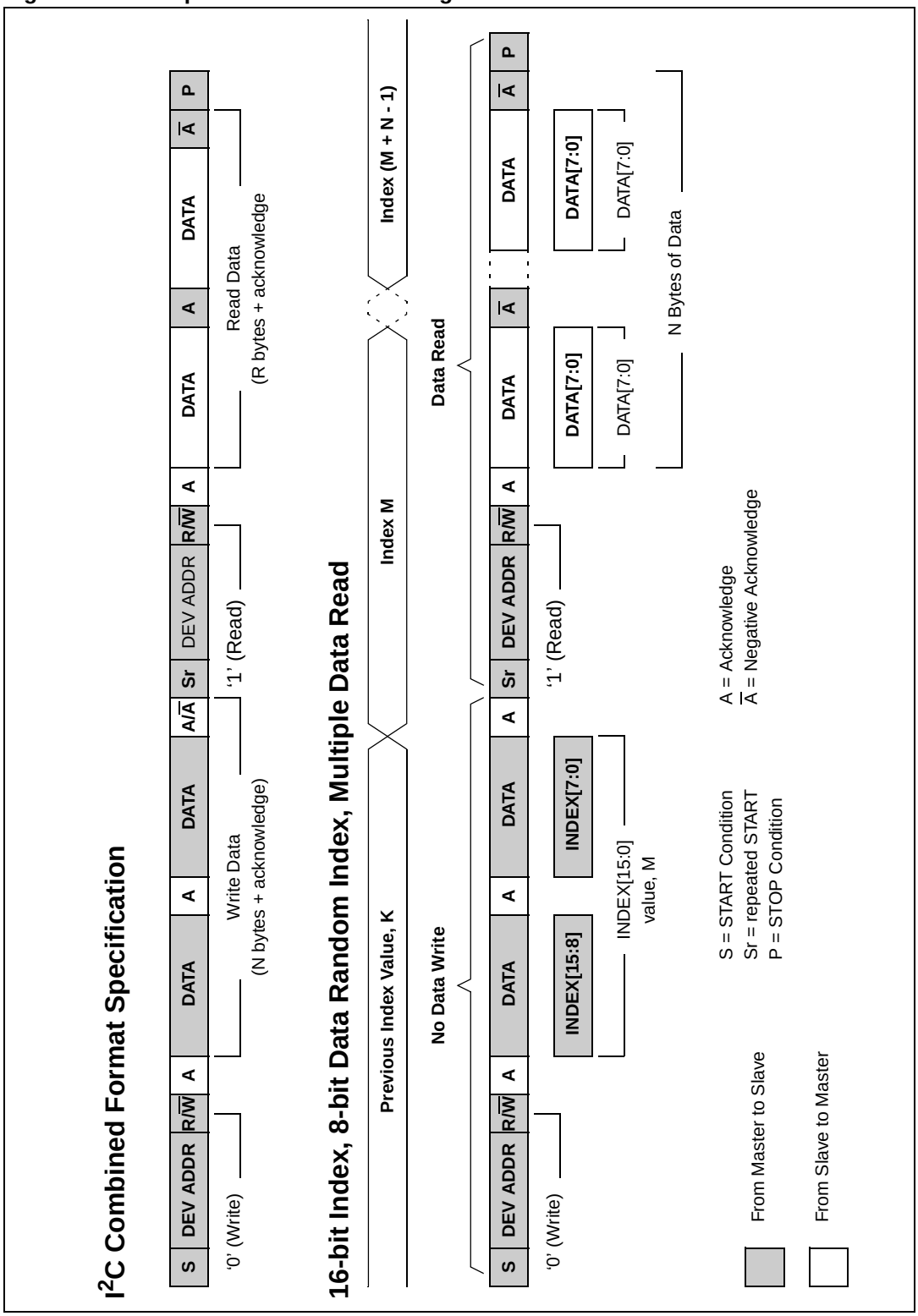


Figure 30. Multiple location read starting from a random location



11 Register map

The VL6524/VS6524 I²C write address is 0x20.

All I²C locations contain an 8-bit byte. However, certain parameters require 16 bits to represent them and are therefore stored in more than 1 location.

Note: For all 16 bit parameters the MSB register must be written before the LSB register.

The data stored in each location can be interpreted in different ways as shown below. Register contents represent different data types as described in *Table 6*.

Table 6. Data type

Data Type	Description
I	Integer parameter.
M	Multiple field registers - 16 bit parameter
B	Bit field register - individual bits must be set/cleared
C	Coded register - function depends on value written
F	Float Value

11.1 Float number format

Float 900 is used in ST co-processors to represent floating point numbers in 2 bytes of data. It conforms to the following structure:

Bit[15] = Sign bit (1 represents negative)

Bit[14:9] = 6 bits of exponent, biased at decimal 31

Bit[8:0] = 9 bits of mantissa

To convert a floating point number to Float 900, use the following procedure:

- represent the number as a binary floating point number. Normalize the mantissa and calculate the exponent to give a binary scientific representation of 1.xxxxxxxxx * 2^y.
- The x symbols should represent 9 binary digits of the mantissa, round or pad with zeros to achieve 9 digits in total. Remove the leading 1 from the mantissa as it is redundant.
- To calculate the y value, bias the exponent by adding to 31 decimal then converting to binary.
- The data can then be placed in the structure above.

11.1.1 Example

Convert -0.41 to Float 900

Convert the fraction into binary by successive multiplication by 2 and removal of integer component

- 0.41 * 2 = 0.82 0
- 0.82 * 2 = 1.64 1
- 0.64 * 2 = 1.28 1
- 0.28 * 2 = 0.56 0
- 0.56 * 2 = 1.12 1
- 0.12 * 2 = 0.24 0
- 0.24 * 2 = 0.48 0
- 0.48 * 2 = 0.96 0
- 0.96 * 2 = 1.92 1
- 0.92 * 2 = 1.84 1
- 0.84 * 2 = 1.68 1
- 0.68 * 2 = 1.36 1
- 1.36 * 2 = 0.72 0

This gives us -0.0110100011110.

We then normalize by moving the decimal point to give - 1.10100011110 * 2^-2.

The mantissa is rounded and the leading zero removed to give 101001000.
We add the exponent to the bias of 31 that gives us 29 or 11101.
A leading zero is added to give 6 bits 011101.

The sign bit is set at 1 as the number is negative.

This gives us 1011 1011 0100 1000 as our Float 900 representation or BB48 in hex.

To convert the encoded representation back to a decimal floating point, we can use the following formula.

Real is = (-1)^sign * ((512+mantissae)>> 9) * 2^(exp-31)

Thus to convert BB48 back to decimal, the following procedure is followed:

Note that >>9 right shift is equal to division by 2^9.

Sign = 1

Exponent = 11101 (29 decimal)

Mantissa = 101001000 (328 decimal)

This gives us:

real = (-1)^1 * ((512+328)/2^9) * 2^(29-31)

real = -1 * (840/512) * 2^(-2)

real = -1 * 1.640625 * 0.25

real = -0.41015625

When compared to the original -0.41, we see that some rounding errors have been introduced.

11.2 Low level control registers

Table 7. Low-level control registers

Name	Index	R/W	Data Type	Format *default*	Description
MicroEnable	0xC003	R/W	C	0x38	0x06 - clocks enabled
Enable I/O	0xC034	R/W	B	0x00	set bit[0] to enable IO

Note: The default values for the above registers are true when the device is powered on, Ext. Clk input is present and the CE pin is high. All other registers can be read when the Clock enable register is set to 0x06.

11.3 Device parameters [read only]

Table 8. Device parameters

Name	Index	R/W	Data Type	Format *default*	Description
uwDeviceId (MSB)	0x0001	R	I	0x02	0x020c = 524
uwDeviceId (LSB)	0x0002	R	I	0x0c	
bFirmwareVsnMajor	0x0004	R	I	0x01	Firmware version 0x0101 = 1.1
bFirmwareVsnMinor	0x0006	R	I	0x01	
bPatchVsnMajor	0x0008	R	I	0x00	Patch version 0x0000
bPatchVsnMinor	0x000a	R	I	0x00	

11.4 Mode control

Table 9. Mode control

Name	Index	R/W	Data Type	Format *default*	Description
bUserCommand	0x0180	RW	C	0	0x00 - UNINITIALISED 0x01 - BOOT 0x02 - RUN 0x03 - PAUSE 0x04 - STOP 0x05 - FLASHGUN

11.5 Mode Status [read only]

Table 10. Mode status

Name	Index	R/W	Data Type	Format *default*	Description
bState	0x0202	R	C	0x10	0x10 - RAW 0x21 - Waiting for BOOT 0x22 - PAUSED 0x26 - Waiting for RUN 0x31 - RUNNING 0x32 - Waiting for PAUSE 0x40 - FLASHGUN 0x50 - STOPPED

11.6 RunModeControl

Table 11. RunModeControl

Name	Index	R/W	Data Type	Format *default*	Description
fMeteringOn	0x0280	R/W	B	0x01	0x00 = False 0x01 = True

11.7 Clock manager input control

Table 12. Clock manager input control

Name	Index	R/W	Data Type	Format *default*	Description
uwExtClockFreqNum (MSB)	0x060b	R/W	I	0x00	Specifies the external clock frequency numerator Default = 12 MHz
uwExtClockFreqNum (LSB)	0x060c	R/W	I	0x0c	
bExtClockFreqDen	0x060e	R/W	I	0x01	Specifies the external clock frequency denominator
bEnableGlobalSystemClockDivision	0x0610	R/W	B	0x00	0x00 = False 0x01 = True -system clock division by 2

11.8 Power management control

Table 13. Power management control

Name	Index	R/W	Data Type	Format *default*	Description
bTimeToPowerdown	0x0580	R/W	I	0x0f	Time (ms) from pausing streaming to entering stop. In the range 5 to 154 ms 0xff - disable

11.9 Frame rate control

Table 14. Frame rate control

Name	Index	R/W	Data Type	Format *default*	Description
uwDesiredFrame Rate_Num (MSB)	0x0d81	R/W	I	0x00	Numerator for the Frame Rate Default = 30 fps
uwDesiredFrame Rate_Num (LSB)	0x0d82	R/W	I	0x1e	
bDesiredFrameRate_ Den	0x0d84	R/W	I	0x01	Denominator for the Frame Rate

11.10 Pipe setup bank selection

Table 15. Pipe setup bank selection

Name	Index	R/W	Data Type	Format *default*	Description
bNonViewLive_ ActivePipeSetupBank	0x0302	R/W	I	0x00	0x00 -Pipe setup bank0 used 0x01 -Pipe setup bank1 used

11.11 Pipe setup bank0 control

Table 16. Pipe setup bank0 control

Name	Index	R/W	Data Type	Format *default*	Description
bImageSize0	0x0380	R/W	C	0x01	Required output dimension 0x01 - ImageSize_VGA 0x02 - ImageSize_QVGA 0x03 - ImageSize_QQVGA 0x04 - ImageSize_Manual
bSubSample0	0x0382	R/W	I	0x01	0x01 = Minimum sub-sample corresponding to no sub-sampling. MAX = 0x06
fEnableCrop0	0x0384	R/W	B	0x00	0x00 = False - 0x01 = True

Table 16. Pipe setup bank0 control (continued)

Name	Index	R/W	Data Type	Format *default*	Description
uwCropHStartMSB0	0x0387	R/W	M I	0x00	Horizontal start point for manual crop
uwCropHStartLSB0	0x0388	R/W	M I	0x00	
uwCropHSizeMSB0	0x038b	R/W	M I	0x00	Horizontal size for manual crop
uwCropHSizeLSB0	0x038c	R/W	M I	0x00	
uwCropVStartMSB0	0x038f	R/W	M I	0x00	Vertical start point for manual crop
uwCropVStartLSB0	0x0390	R/W	M I	0x00	
uwCropVSizeMSB0	0x0393	R/W	M I	0x00	Vertical size for manual crop
uwCropVSizeLSB0	0x0394	R/W	M I	0x00	
bdataFormat0	0x0396	R/W	C	0x01	0x00 = YCbCr_JFIF 0x01 = YCbCr_Rec601 0x02 = YCbCr_Custom 0x03 = RGB_565 0x04 = RGB_565_Custom 0x05 = RGB_444 0x06 = RGB_444_Custom 0x07 = reserved 0x08 = Bayer output VP
bBayerOutput Alignment0	0x398	R/W	C	0x04	0x04 = Bayer output right shifted 0x05 = Bayer output left shifted
bContrast0	0x039a		I	0x79	Contrast control (%)
bColorSaturation0	0x039c		I	0x7d	Color saturation control (%)
bGamma0	0x039e		I	0x0f	Gamma settings 0x00 = Gamma_Linear 0x10 = Gamma SMPTE 240M 0x1F = Gamma_Max
fHorizontaiMirror0	0x03a0		B	0x00	Horizontal mirror control, 0x00 = False - 0x01 = True
fVerticalFlip0	0x03a2		B	0x00	Vertical mirror control, 0x00 = False - 0x01= True

11.12 Pipe Setup Bank1 Control

Table 17. Pipe setup bank1 control

Name	Index	R/W	Data Type	Format *default*	Description
bImageSize1	0x0400	R/W	C	0x01	Required output dimension 0x01 = ImageSize_VGA 0x02 = ImageSize_QVGA 0x03 = ImageSize_QQVGA 0x04 = ImageSize_Manual
bSubSample1	0x0402	R/W	C	0x01	0x01 = Minimum sub-sample corresponding to no sub-sampling. MAX = 0x06
fEnableCrop1	0x0404	R/W	B	0x00	0x00 = False - 0x01 = True
uwCropHStartMSB1	0x0407	R/W	M I	0x00	Horizontal start point for manual crop
uwCropHStartLSB1	0x0408	R/W	M I	0x00	
uwCropHSizeMSB1	0x040b	R/W	M I	0x00	Horizontal size for manual crop
uwCropHSizeLSB1	0x040c	R/W	M I	0x00	
uwCropVStartMSB1	0x040f	R/W	M I	0x00	Vertical start point for manual crop
uwCropVStartLSB1	0x0410	R/W	M I	0x00	
uwCropVSizeMSB1	0x0413	R/W	M I	0x00	Vertical size for manual crop
uwCropVSizeLSB1	0x0414	R/W	M I	0x00	
bdataFormat1	0x0416	R/W	C	0x01	0x00 = YCbCr_JFIF 0x01 = YCbCr_Rec601 0x02 = YCbCr_Custom 0x03 = RGB_565 0x04 = RGB_565_Custom 0x05 = RGB_444 0x06 = RGB_444_Custom 0x07 = BayerVPBypass 0x08 = BayerThroughVP
bBayerOutput Alignment1	0x0418	R/W	C	0x04	0x04 = Bayer output right shifted 0x05 = Bayer output left shifted
bContrast1	0x041a	R/W	I	0x79	Contrast control (%)
bColorSaturation1	0x041c	R/W	I	0x7d	Color saturation control (%)
bGamma1	0x041e	R/W	I	0x0f	Gamma settings 0x00 = Gamma_Linear 0x10 = Gamma SMPTE 240M 0x1F = Gamma_Max
fHorizontalMirror1	0x0420	R/W	B	0x00	Horizontal mirror control 0x00 = False, 0x01 = True
fVerticalFlip1	0x0422	R/W	B	0x00	Vertical mirror control 0x00 = False, 0x01 = True

11.13 View live control

Table 18. View live control

Name	Index	R/W	Data Type	Format *default*	Description
fEnable	0x0480	R/W	B	0x00	Enable ViewLive mode 0x00 = False - 0x01 = True
InitalPipeSetupBank	0x0482	R/W	C	0x00	When ViewLive mode is enabled, this register selects which PipeSetupBank the first frame output uses, 0x00 = PipeSetupBank0 0x01 = PipeSetupBank1

11.14 White balance control

Table 19. White balance control

Name	Index	R/W	Data Type	Format *default*	Description
WhiteBalanceMode	0x1380	R/W	C	0x01	White balance mode selection: 0x00 = OFF - No White balance, all gains are unity in this mode 0x01 = AUTOMATIC 0x03 = MANUAL_RGB - gains are applied manually using registers below 0x04 = DAYLIGHT_PRESET 0x05 = TUNGSTEN_PRESET 0x06 = FLUORESCENT_PRESET 0x07 = HORIZON_PRESET 0x08 = MANUAL_COLOUR_TEMP 0x09 = FLASHGUN_PRESET
bManualRedGain	0x1382	R/W	I	0x00	User setting for Red Channel gain
bManualGreenGain	0x1384	R/W	I	0x00	User setting for Green Channel gain
bManualBlueGain	0x1386	R/W	I	0x00	User setting for Blue Channel gain
fpRedGainforFlashgun MSB	0x138b	R/W	M F	0x3e	Red Channel gain for Flashgun Code float - Default 0x3e66 = 1.199219
fpRedGainforFlashgun LSB	0x138c	R/W	M F	0x66	
fpGreenGainfor Flashgun MSB	0x138f	R/W	M F	0x3e	Green Channel gain for Flashgun Code float - Default 0x3e00 = 1.000000
fpGreenGainfor Flashgun LSB	0x1390	R/W	M F	0x00	
fpBlueGainfor Flashgun MSB	0x1393	R/W	M F	0x3e	Blue Channel gain for Flashgun Code float. Default 0x3e33 = 1.099609
fpBlueGainfor Flashgun LSB	0x1394	R/W	M F	0x33	

11.15 Exposure control

Table 20. Exposure control

Name	Index	R/W	Data Type	Format *default*	Description
bExposureMode	0x1080	R/W	C	0x00	0x00 = AUTOMATIC_MODE 0x01 = COMPILED_MANUAL_ MODE - The desired exposure time is set manually in the Manual Exposure registers and the exposure parameters are calculated by the algorithm. 0x02 = DIRECT_MANUAL_ MODE - The exposure parameters are input directly. 0x03 = FLASHGUN_MODE - The exposure parameters are set manually.
bExposureMetering	0x1082	R/W	C	0x00	Weights associated with the zones to calculate the mean statistics. Exposure Weight is Centered or Backlit or Flat. 0x00 = ExposureMetering_flat - Uniform gain associated with all pixels 0x01 = ExposureMetering_backlit: more gain associated with centre and bottom pixels 0x02 = ExposureMetering_centred - more gain associated with centre pixels
bManualExposure Time_Num	0x1084	R/W	I	0x01	Exposure Time for Compiled Manual Mode in seconds. Numerator / Denominator gives required exposure time
bManualExposure Time_Den	0x1086	R/W	I	0x1e	
iExposure Compensation	0x1090	R/W	I	0x00	Exposure Compensation - a user choice for setting the runtime target. A unit of exposure compensation corresponds to 1/6 EV. This is a signed register.
fFreezeAuto Exposure	0x10b4	R/W	B	0x00	Freeze auto exposure 0x00 = False 0x01 = True
fpUserMaximum IntegrationTime (MSB)	0x10b7	R/W	M F	0x64	User Maximum Integration Time in microseconds. This control takes in the maximum integration time that host would like to support. This in turn gives an idea of the degree of “wobbly pencil effect” acceptable by Host. Default 0x647f = 654336
fpUserMaximum IntegrationTime (LSB)	0x10b8	R/W	M F	0x7f	

11.16 Exposure status (Read only)

Table 21. Exposure status

Name	Index	R/W	Data Type	Format *default*	Description
fpCompiledTime (MSB)	0x121d	R	M F		Present exposure time as calculated by the compiler taking into account the framerate used.
fpCompiledTime (LSB)	0x121e	R	M F		

11.17 Exposure algorithm control

Table 22. Exposure algorithm control

Name	Index	R/W	Data Type	Format *default*	Description
bLeakShift	0x113c	R/W	I	0x02	Control exposure leaky integrator. Set to 0 for reactive systems. Set to 4 for more stable systems.

11.18 Flashgun control

Table 23. Flashgun control

Name	Index	R/W	Data Type	Format *default*	Description
bFlashgunMode	0x1780	R/W	C	0x00	Manual flashgun control(1) 0x00 = Flash off 0x01 = Torch (FSO pin high) 0x02 = Flash pulse
uwFlashgunOffLine MSB	0x1783	R/W	M I	0x02	This is used to set the duration of the flash. The value equals the line in the frame during which the flashgun pulse is switched off.
uwFlashgunOffLine LSB	0x1784	R/W	M I	0x1c	

1. The mode control register has priority over this function

11.19 Flicker frequency control

Table 24. Flicker frequency control

Name	Index	R/W	Data Type	Format *default*	Description
bAntiFlickerMode	0x10c0	R/W	C	0x01	Modes for anti-flicker compilation. 0x00 = Inhibit 0x01 = Manual Enable
bLightingFreqHz	0x0c80	R/W	I	0x64	Flicker free time period calculations this should be 2* AC mains frequency 0x64 = 100 = 50Hz AC freq 0x78 =120 = 60Hz AC freq
fFlickerComplatible FrameLength	0x0c82	R/W	B	0x00	Set to make the frame length compatible with the flicker free time period, 0x00 = FALSE 0x01 = TRUE

11.20 Defect correction control

Table 25. Defect correction control

Name	Index	R/W	Data Type	Format *default*	Description
fDisableScytheFilter	0x1a80	R/W	B	0x00	0x00 = False 0x01 = True
fDisableJackFilter	0x1b00	R/W	B	0x00	0x00 = False 0x01 = True

11.21 Sharpening control

Table 26. Sharpening control

Name	Index	R/W	Data Type	Format *default*	Description
bUserPeakGain	0x1d80	R/W	I	0x0f	Adjust gradient of sharpening system
bUserPeakLo Threshold	0x1d90	R/W	I	0x1e	The coring threshold is used to stop the sharpening gain being applied to very small changes in the image (i.e. Noise).

11.22 Fade to black damper control

Table 27. Fade to black damper control

Name	Index	R/W	Data Type	Format *default*	Description
fDisable	0x2000	R/W	B	0x00	Set to disable fade to black operation. 0x00 = False 0x01 = True
fpBlackValue (MSB)	0x2003	R/W	M F	0x00	Minimum possible damper output for the color matrix 0.0 fades to absolute black, 1.0 effectively disables fade to black. Default 0x0000 = 0
fpBlackValue (LSB)	0x2004	R/W	M F	0x00	
fpDamperLow Threshold (MSB)	0x2007	R/W	M F	0x63	Low threshold to calculate the damper slope Default 0x63d1 =500224
fpDamperLow Threshold (LSB)	0x2008	R/W	M F	0xd1	
fpDamperHigh Threshold (MSB)	0x200b	R/W	M F	0x65	High threshold to calculate the damper slope Default 0x656f = 900096
fpDamperHigh Threshold (LSB)	0x200c	R/W	M F	0x6f	
fpMinimumOutput (MSB)	0x200f	R	F		Status value showing damper strength used
fpMinimumOutput (LSB)	0x2010	R	F		

11.23 Dither control

Table 28. Dither control

Name	Index	R/W	Data Type	Format *default*	Description
DitherControl	0x2080	R/W	C	0x00	0x00 = Dither RGB modes only 0x01 = Dither function OFF 0x02 = Dither function ON

11.24 Output formatter control

Table 29. Output formatter control

Name	Index	R/W	Data Type	Format *default*	Description
bCodeCheckEnable	0x2100	R/W	C	0x07	0x00 - allow all output values 1 = suppress 0xFF 2 = suppress 0x00 3 = suppress 0x00 and 0xFF from output
bSyncCodeSetup	0x2104	R/W	B	0x01	[0] Enable Sync Codes [1] Sync Code Type (0 = ITU, 1 = mode2) [2] Odd/Even field (0 =even, 1 =odd) [3] Toggle (1 = Toggle) [4] Load (set high then low over a frame boundary to consume a change applied in [2] or [3])
bHSyncSetup	0x2106	R/W	B	0x0b	[0] Enable [1] Polarity [2] Active lines only [3] Automatic/manual
bVSyncSetup	0x2108	R/W	B	0x07	[0] Enable [1] Polarity [2] Automatic/Manual
bPClkSetup	0x210a	R/W	B	0x05	[0] Edge (1=positive, 0 =negative) [1] Non-active level (1=high. 0 = low) [2] Enable [7] Free-running
fpPclkEn	0x210c	R/W	B	0x01	0 = False - 1 = True
bBlankData_MSB	0x2110	R/W	I	0x10	Blanking MSB
bBlankData_LSB	0x2112	R/W	I	0x80	Blanking LSB
bRgbSetup	0x2114	R/W	B	0x00	[0] RGB 444 - zero packing [1] Swap R and B components [2] Reverse Bits
bYuvSetup	0x2116	R/W	B	0x00	[0] Cb_first [1] Y first
bVsyncRisingLineH	0x2118	R/W	M I	0x00	Line on which Vsync should rise (manual vsync must be selected)
bVsyncRisingLineL	0x211a	R/W	M I	0x00	
bVsyncRisingPixelH	0x211c	R/W	M I	0x01	Pixel on which Vsync should rise (manual vsync must be selected)
bVsyncRisingPixelL	0x211e	R/W	M I	0x01	
bVsyncFallingLineH	0x2120	R/W	M I	0x01	Line on which Vsync should fall (manual vsync must be selected)
bVsyncFallingLineL	0x2122	R/W	M I	0xf2	
bVsyncFallingPixelH	0x2124	R/W	M I	0x00	Pixel on which Vsync should fall (manual vsync must be selected)
bVsyncFallingPixelL	0x2126	R/W	M I	0x01	

Table 29. Output formatter control (continued)

Name	Index	R/W	Data Type	Format *default*	Description
bHsyncRisingH	0x2128	R/W	M I	0x00	Pixel on which Hsync should rise (manual Hsync must be selected)
bHsyncRisingL	0x212a	R/W	M I	0x03	
bHsyncFallingH	0x212c	R/W	M I	0x00	Pixel on which Hsync should fall (manual Hsync must be selected)
bHsyncFallingL	0x212e	R/W	M I	0x07	

12 Optical specifications

Table 30. Optical specifications(1)

Parameter	Min.	Typ.	Max.	Unit
Optical format		1/6		inch
Effective focal length		2.5		mm
Aperture (F number)		2.8		
Horizontal field of view	46	49	51	deg.
Vertical field of view	35	37	39	deg.
Diagonal field of view(2)	57	59	61	deg.
Depth of field(3)	20		infinity	cm
TV distortion	-1.5		1.5	%

1. All measurements made at 23°C ± 2°C
2. Value determined through calculation
3. By design the device has an acceptable quality between hyperfocal distance /2 and infinity.

12.1 Average sensitivity

The average sensitivity is a measure of the image sensor response to a given light stimulus. The optical stimulus is a white light source with a color temperature of 3200K, producing uniform illumination at the surface of the sensor package. An IR blocking filter is added to the light source. The analog gain of the sensor is set to x1. The exposure time, Δt, is set as 50% of maximum. The illuminance, I, is adjusted so the average sensor output code, Xlight, is roughly mid-range equivalent to a saturation level of 50%. Once Xlight has been recorded the experiment is repeated with no illumination to give a value Xdark.

The sensitivity is then calculated as $\frac{Xlight - Xdark}{\Delta t \cdot I}$.The result is expressed in volts per lux-second.

The sensitivity of the VS6524 is given in *Table 31*.

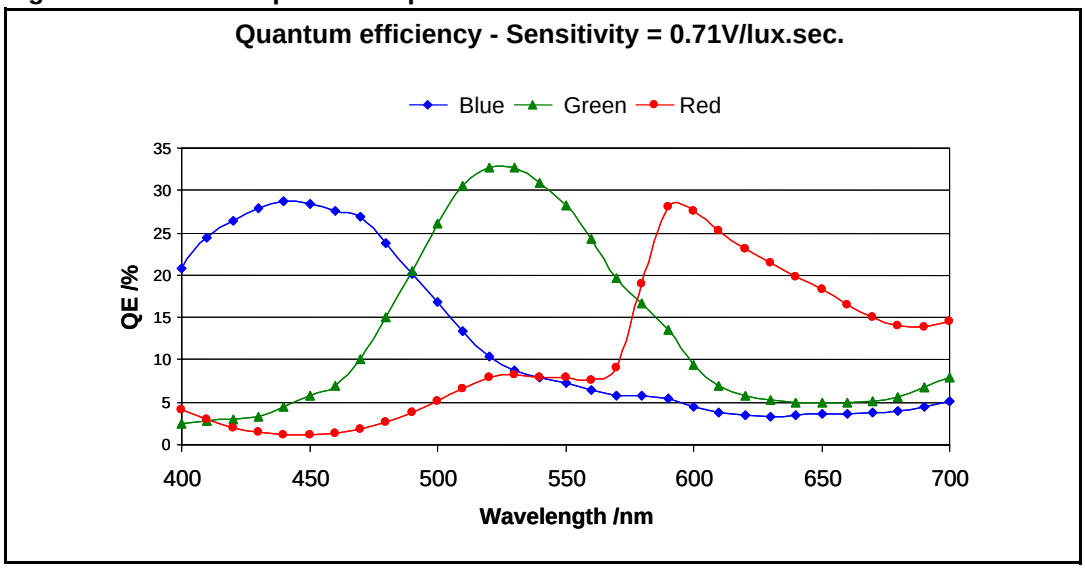
Table 31. VS6524 average sensitivity

Optical parameter	Value	Unit
Average sensitivity	0.71	V/lux.s

12.2 Spectral response

The spectral response for the VS6524 sensor is shown in *Figure 31*.

Figure 31. VS6524 spectral response



13 Electrical characteristics

13.1 Absolute maximum ratings

Table 32. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STO}	Storage temperature	-40	85	° C
V_{DD}	Digital power supplies	-0.5	3.3	V
AVDD	Analog power supplies	-0.5	3.3	V

Caution: Stresses above those listed under “Absolute Maximum Ratings” can cause permanent damage to the device. This is a stress rating only and functional operations of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

13.2 Operating conditions

Table 33. Supply specifications

Symbol	Parameter	Min.	Max.	Unit
T_{AF}	Operating temperature, functional (Camera is electrically functional)	-30	70	° C
T_{AN}	Operating temperature, nominal (Camera produces acceptable images)	-25	55	° C
T_{AO}	Operating temperature, optimal (Camera produces optimal optical performance)	5	30	° C
V_{DD}	Digital power supplies operating range (@ module pin(1))	1.7	2.0	V
		2.4	3.0	V
AVDD	Analog power supplies operating range (@ module pin(1))	2.4	3.0	V

1. Module can contain routing resistance up to 5 Ω

13.3 DC electrical characteristics

Note: Over operating conditions unless otherwise specified.

Table 34. DC electrical characteristics

Symbol	Description	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage	V_{DD} 1.7 ~ 2.0 V	-0.3		0.25 V_{DD}	V
		V_{DD} 2.4 ~ 3.0 V	-0.3		0.3 V_{DD}	
V_{IH}	Input high voltage	V_{DD} < 2.7 V	0.7 V_{DD}		V_{DD} + 0.3	V
		V_{DD} > 2.7 V	0.7 V_{DD}		3.46	V
V_{OL}	Output low voltage	I_{OL} < 2 mA I_{OL} < 4 mA			0.2 V_{DD} 0.4 V_{DD}	V
V_{OH}	Output high voltage	I_{OH} < 2 mA	0.8 V_{DD}			V
I_{IL}	Input leakage current Input pins I/O pins	0 < V_{IN} < V_{DD}	-10 -1		+10 +1	µA µA
	Input leakage current SDA and SCL pins	V_{IH} > V_{DD} + 0.3 V	-2		+500	µA
C_{IN}	Input capacitance, SCL	T_A = 25° C, freq = 1 MHz			6	pF
C_{OUT}	Output capacitance	T_A = 25° C, freq = 1 MHz			6	pF
$C_{I/O}$	I/O capacitance, SDA	T_A = 25° C, freq = 1 MHz			8	pF

Table 35. Typical current consumption

Symbol	Description	Test conditions	I_{AVDD}	I_{VDD}		Units
				V_{DD} = 1.8V	V_{DD} = 2.8V	
I_{PD}	Supply current in power down mode	CE=0, CLK = 12 MHz	0.01	0.6	0.8	µA
I_{stanby}	Supply current in Standby mode	CE=1, CLK = 12 MHz	0.001	0.4	1.2	mA
I_{stop}	Supply current in Stop mode	CE=1, CLK = 12 MHz	0.002	0.4	7.45	mA
I_{Pause}	Supply current in Pause mode	CE=1, CLK = 12 MHz	0.050	14.99	24.4	mA
I_{run}	Supply current in active streaming run mode	CE=1, CLK = 12 MHz streaming VGA @30 fps	8.3	32.6	41.0	mA

13.4 AC electrical characteristics

13.4.1 External clock

The VL6524/VS6524 requires an external clock. This clock is a CMOS digital input. The clock input is fail-safe in power down mode.

Table 36. External clock

CLK	Range			Unit
	Min.	Typ.	Max.	
DC coupled square wave		VDD		V
Clock frequency (normal operation)	6.50	6.50, 8.40, 9.60, 9.72, 12.00, 13.00, 16.80, 19.20, 19.44	26	MHz

13.4.2 Chip enable

CE is a CMOS digital input. The module is powered down when a logic 0 is applied to CE. See *Chapter 4* for power down and for power-up sequence.

13.4.3 I²C slave interface

VL6524/VS6524 contains an I²C-type interface using two signals: a bidirectional serial data line (SDA) and an input-only serial clock line (SCL). See *Chapter 10* for detailed description of protocol.

Table 37. Serial interface voltage levels(1)

Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
V_{HYS}	Hysteresis of Schmitt Trigger Inputs					
	V_{DD} > 2 V	N/A	N/A	0.05 V_{DD}	-	V
	V_{DD} < 2V	N/A	N/A	0.1 V_{DD}	-	V
	LOW level output voltage (open drain) at 3mA sink current					
V_{OL1}	V_{DD} > 2 V	0	0.4	0	0.4	V
V_{OL3}	V_{DD} < 2V	N/A	N/A	0	0.2 V_{DD}	V
V_{OH}	HIGH level output voltage	N/A	N/A	0.8 V_{DD}		V
t_{OF}	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance from 10 pF to 400 pF	-	250	20+0.1C_b(2)	250	ns
t_{SP}	Pulse width of spikes which must be suppressed by the input filter	N/A	N/A	0	50	ns

1. Maximum $V_{IH} = V_{DDmax}$ + 0.5 V
2. C_b = capacitance of one bus line in pF

Figure 32. Voltage level specification

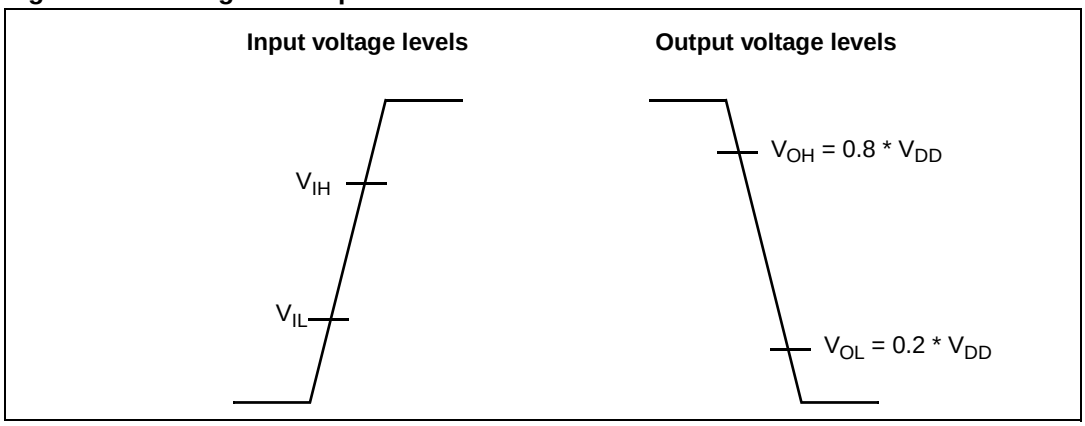


Table 38. Timing specification(1)

Symbol	Parameter	Standard mode		Fast mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;STA}$	Hold time for a repeated ***start***	4.0	-	0.6	-	µs
t_{LOW}	LOW period of SCL	4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of SCL	4.0	-	0.6	-	µs
$t_{SU;STA}$	Set-up time for a repeated ***start***	4.7	-	0.6	-	µs
$t_{HD;DAT}$	Data hold time (1)	300	-	300	-	ns
$t_{SU;DAT}$	Data Set-up time (1)	250	-	100	-	ns
t_r	Rise time of SCL, SDA	-	1000	$20+0.1C_b$(2)	300	ns
t_f	Fall time of SCL, SDA	-	300	$20+0.1C_b$(2)	300	ns
$t_{SU;STO}$	Set-up time for a ***stop***	4.0	-	0.6	-	µs
t_{BUF}	Bus free time between a ***stop*** and a ***start***	4.7	-	1.3	-	µs
C_b	Capacitive Load for each bus line	-	400	-	400	pF
V_{nL}	Noise Margin at the LOW level for each connected device (including hysteresis)	0.1 V_{DD}	-	0.1 V_{DD}	-	V
V_{nH}	Noise Margin at the HIGH level for each connected device (including hysteresis)	0.2 V_{DD}	-	0.2 V_{DD}	-	V

1. All values are referred to a V_{IHmin} = 0.9 V_{DD} and V_{ILmax} = 0.1 V_{DD}
2. C_b = capacitance of one bus line in pF

Figure 33. Timing specification

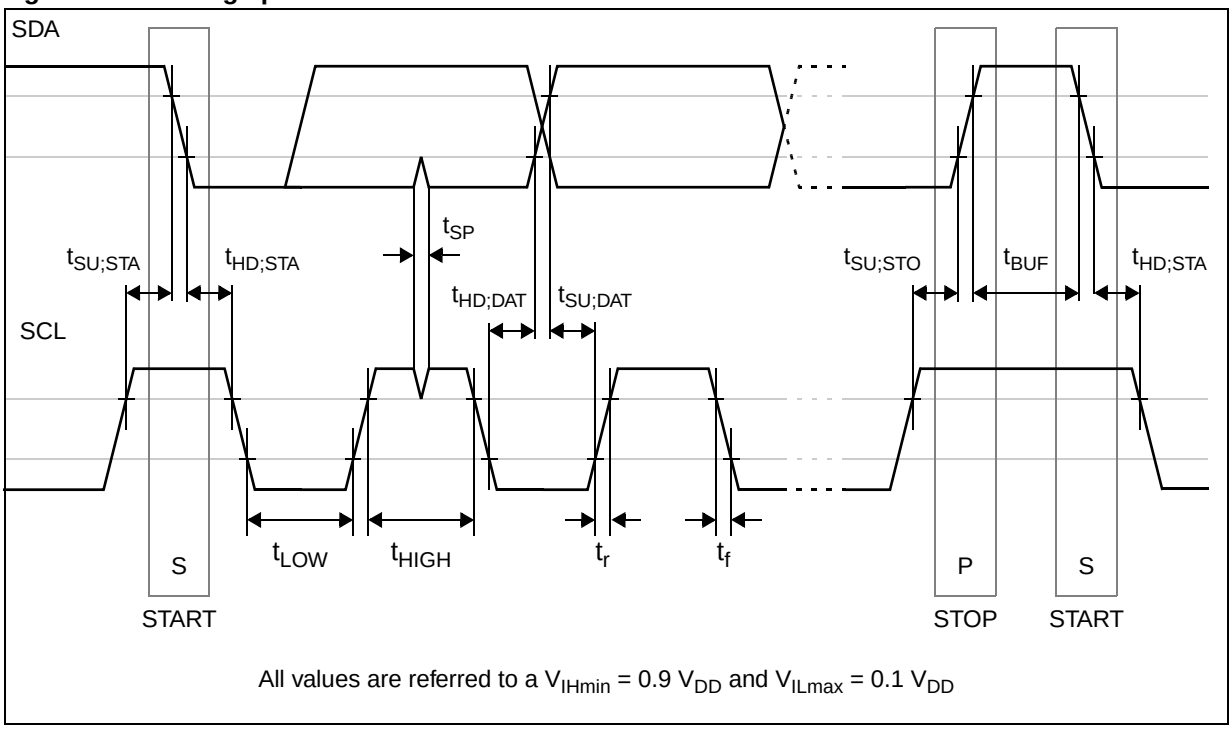
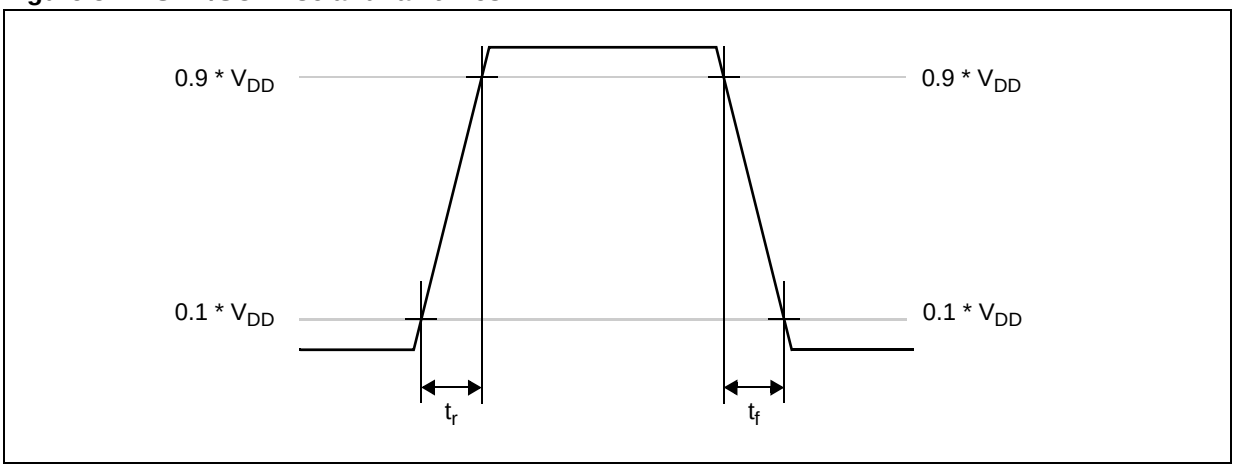


Figure 34. SDA/SCL rise and fall times



13.4.4 Parallel data interface timing

VL6524/VS6524 contains a parallel data output port (D[7:0]) and associated qualification signals (HSYNC, VSYNC, PCLK and FSO).

This port can be enabled and disabled (tri-stated) to facilitate multiple camera systems or bit-serial output configurations. The port is disabled (high impedance) upon reset.

Figure 35. Parallel data output video timing

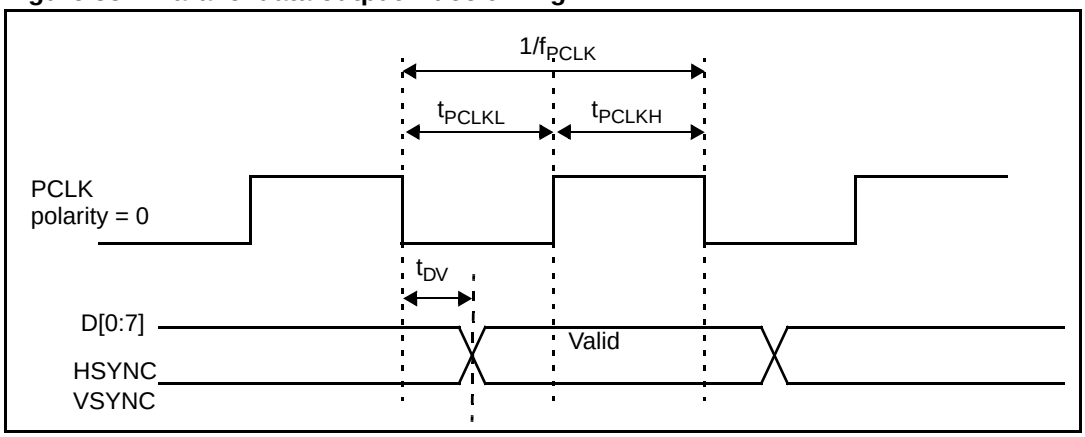


Table 39. Parallel data interface timings

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
f_{PCLK}	PCLK frequency				26	MHz
t_{PCLKL}	PCLK low width		10			ns
t_{PCLKH}	PCLK high width		10			ns
t_{DV}	PCLK to output valid		-5		5	ns

13.5 ESD handling characteristics

Table 40. ESD handling characteristics

Test	Criteria	Unit
ESD Machine Model	150	V
ESD Human body	2.0	kV

14 Package outline

14.1 SmOP

Figure 36. VS6524Q06J outline drawing

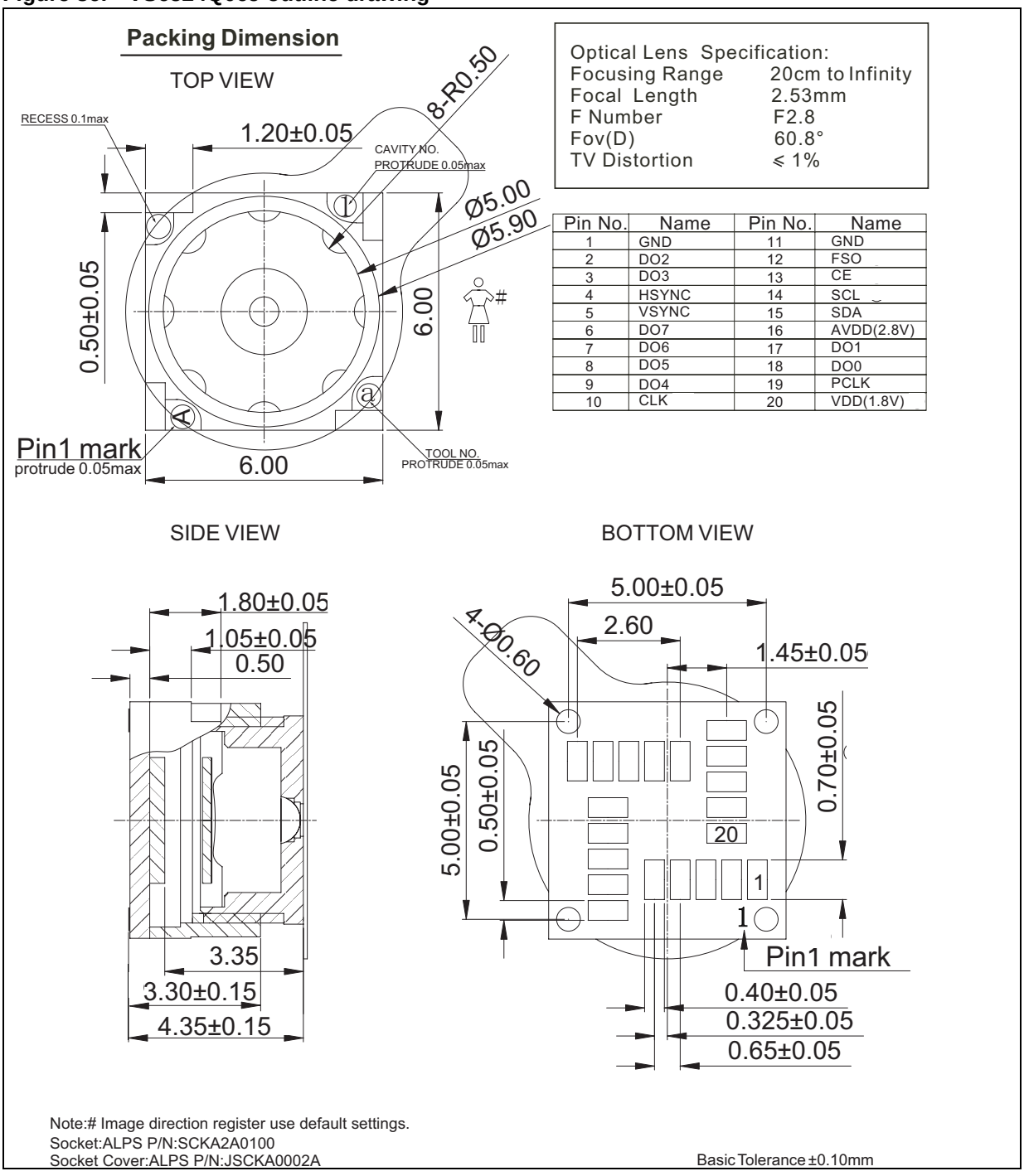
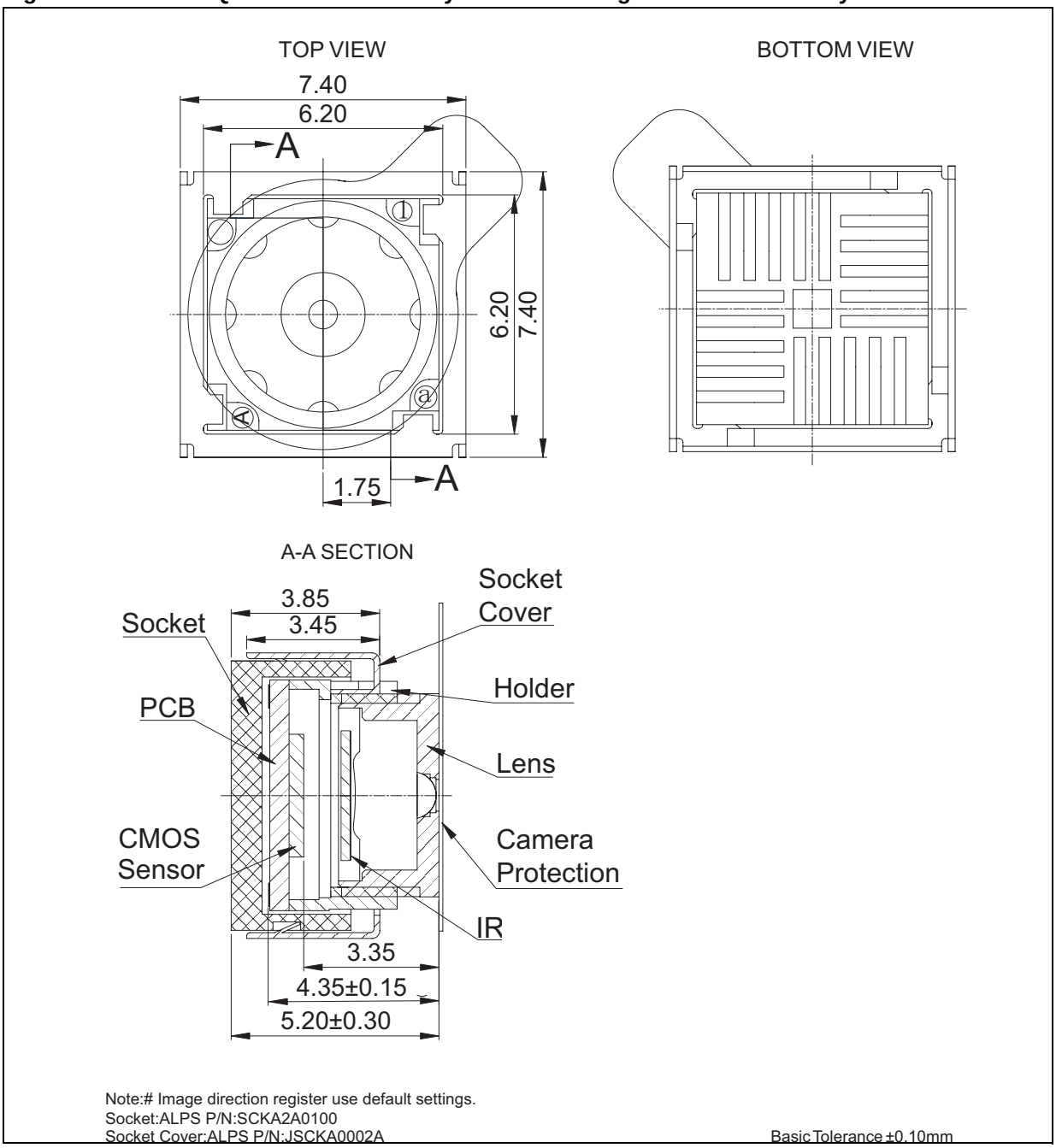


Figure 37. VS6524Q06J socket assembly outline drawing for information only



14.2 LGA

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 41. LGA package mechanical data

Data book (mm)			
Symbol	**Min.**	**Typ.**	**Max.**
A	1.80	1.90	2.00
A4	0.35	0.4	0.45
A5	0.7	0.8	0.9
B1		2.0	
B2		3.5	
B3		0.55	
b	0.25	0.30	0.35
D	9.90	10.00	10.10
D1	9.60	9.70	9.80
D2		5	
D4		5.4	
e		0.8	
E	9.90	10.00	10.10
E1	9.60	9.70	9.80
E2		5	
E4		4.5	
G	1.0	1.1	1.2
G1		1	
G2	0.3	0.4	0.5
G3	0.8	0.9	1.0
G4		0.8	
H	0.8	0.9	1.0
H1		0.8	
H2	0.3	0.4	0.5
I	3.95	4.05	4.15
J		4.1	
K		0.3	

Table 41. LGA package mechanical data (continued)

Data book (mm)			
Symbol	**Min.**	**Typ.**	**Max.**
PHI	4°	5°	6°
z		1.65	
L	0.7	0.8	0.9
bbb		0.01	
ccc		0.1	
ddd		0.08	
eee		0.08	
nD		9	
nE		9	
n		36	

Figure 38. VL6524QOMH outline drawing

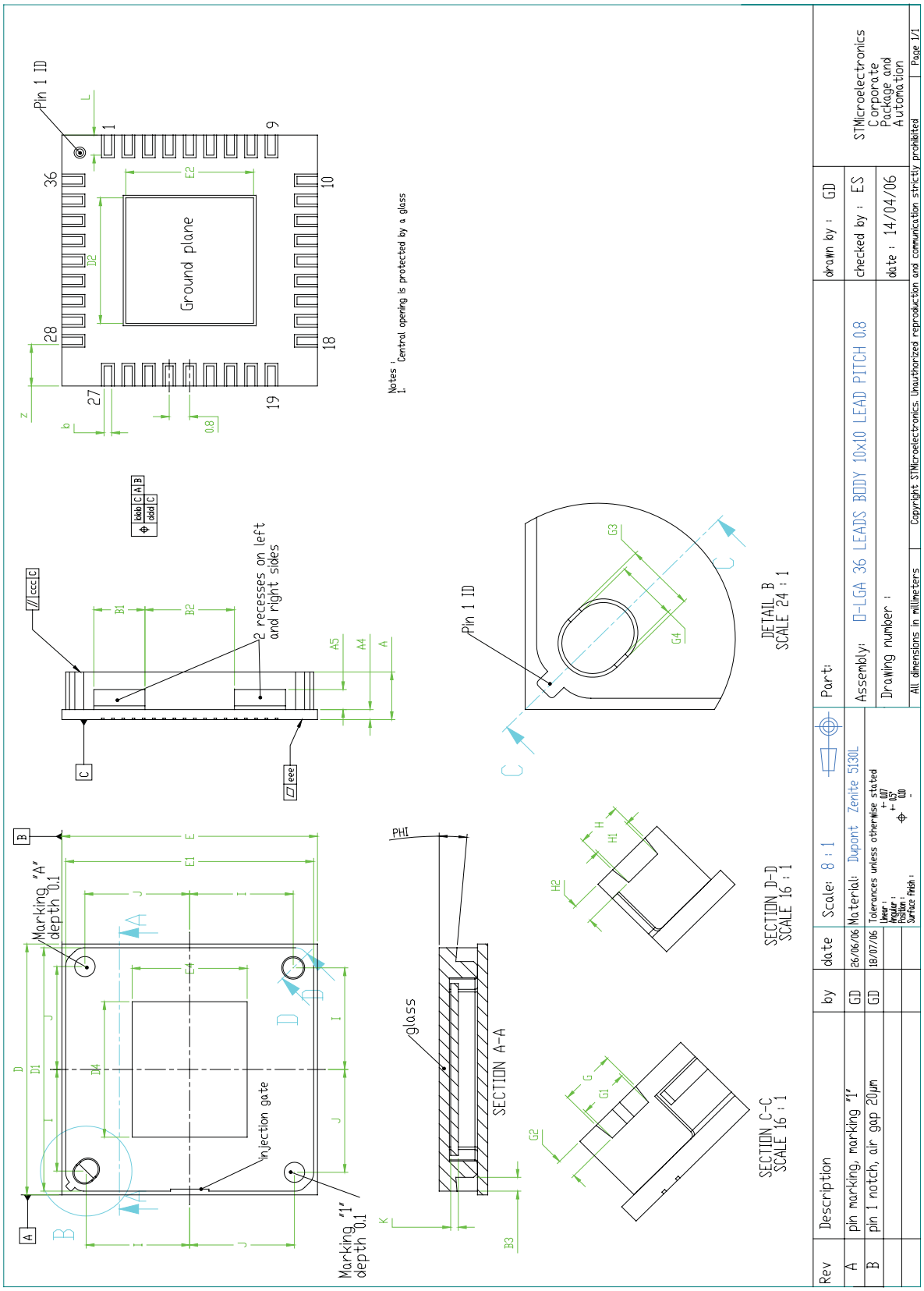


Table 42. VL6524 pin assignment

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	AVDD	10	GND	19	DIO7	28	GND
2	GND	11	NC	20	DIO6	29	PCLK
3	SDA	12	NC	21	DIO5	30	VDD
4	SCL	13	NC	22	DIO4	31	NC
5	CE	14	NC	23	VDD	32	NC
6	VDD	15	AVDD	24	DIO3	33	NC
7	CLK	16	HSYNC	25	DIO2	34	NC
8	GND	17	VSYNC	26	DIO1	35	NC
9	FSO	18	GND	27	DIO0	36	GND

15 Ordering information

Table 43. Order codes

Part number	Package
VS6524Q06J	SmOP 6x6x4.35 mm
VL6524QOMH	LGA 10x10x1.90 mm
IMG-524-E01	Baseboard with socket plug-in for X24 camera integration kit
IMG-524-P02	LGA package plug-in for X24 camera integration kit

16 Revision history

Table 44. Document revision history

Date	Revision	Changes
21-Mar-2006	1	Initial release.
29-Jun-2006	2	Updates in *Table 30: Optical specifications* and addition of *Section 12.1: Average sensitivity* and *Section 12.2: Spectral response*. Updates in *Table 34: DC electrical characteristics* Updates in *Table 40: ESD handling characteristics* Updates in *Figure 35: Parallel data output video timing*
06-Nov-2006	3	Addition of VL6524 reference and package outline drawing.
22-Dec-2007	4	Corrected number of interframe blanking lines (0x10/0x80) in *Figure 5*. Corrected default value for registers with index 0x2007 and 0x2008 in *Table 27*. Replaced IOL with IOH for VOH test conditions in *Table 34*. Corrected t4 value(>=200 µs) in *Figure 3*. Updated the 4 steps in *Section 9.1*.
09-Feb-2007	5	Corrected IOH value to < 2 mA in *Table 34*, . Corrected ESD human body criteria to 2.0 kV in *Table 40.*

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