Programmable Spread Spectrum Clock Generator for EMI Reduction

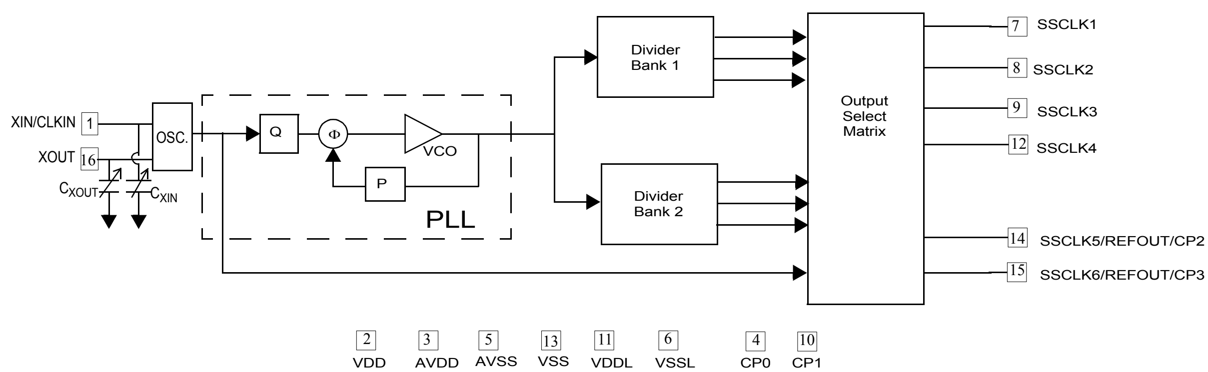
Features

- **Wide operating output (SSCLK) frequency range**
  - **3–200 MHz**
- **Programmable spread spectrum with nominal 31.5-kHz modulation frequency.**
- **Center spread: ±0.25% to ±2.5%**
- **Down spread: –0.5% to –5.0%**
- **Input frequency range:**
  - **External crystal: 8–30 MHz fundamental crystals**
  - **External reference: 8–166 MHz Clock**
- **Integrated phase-locked loop (PLL)**
- **Programmable crystal load capacitor tuning array**
- **Low cycle-to-cycle Jitter**
- **3.3V operation with 2.5V output clock drive option**
- **Spread spectrum On/Off function**
- **Power-down or Output Enable function**
- **Output frequency select option**

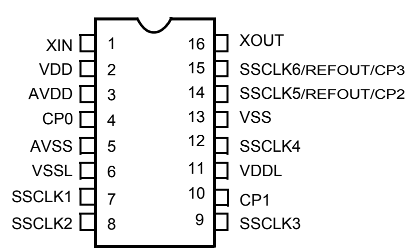
Benefits

- Suitable for most PC peripherals, networking, and consumer applications.
- Provides wide range of spread percentages for maximum EMI reduction, to meet regulatory agency Electro Magnetic Compliance (EMC) requirements. Reduces development and manufacturing costs and time-to-market.
- Eliminates the need for expensive and difficult to use higher order crystals.
- Internal PLL generates up to 200 MHz outputs, and can generate custom frequencies from an external crystal or a driven source.
- Enables fine-tuning of output clock frequency by adjusting C_{Load} of the crystal. Eliminates the need for external C_{Load} capacitors.
- Application compatibility in standard and low-power systems.
- Provides ability to enable or disable spread spectrum with an external pin.
- Enables low-power state or output clocks to High-Z state.

Logic Block Diagram



Pin Configuration



General Description

The CY25200 is a Spread Spectrum Clock Generator (SSCG) IC used for the purpose of reducing Electro Magnetic Interference (EMI) found in today's high-speed digital electronic systems.

The device uses a Cypress proprietary Phase-Locked Loop (PLL) and Spread Spectrum Clock (SSC) technology to synthesize and modulate the frequency of the input clock. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies are greatly reduced. This reduction in radiated energy can significantly reduce the cost of complying with regulatory agency requirements (EMC) and improve time to market without degrading system performance.

The CY25200 uses a factory-programmable configuration memory array to synthesize output frequency, spread %, crystal load capacitor, clock control pins, PD# and OE options.

The spread % is factory programmed to either center spread or down spread with various spread percentages. The range for center spread is from ±0.25% to ±2.50%. The range for down spread is from –0.5% to –5.0%. Contact the factory for smaller or larger spread % amounts if required.

The input to the CY25200 can be either a crystal or a clock signal. The input frequency range for crystals is 8–30 MHz, and for clock signals is 8–166 MHz.

The CY25200 has six clock outputs, SSCLK1 to SSCLK6. The frequency modulated SSCLK outputs can be programmed from 3–200 MHz.

The CY25200 products are available in a 16-pin TSSOP package with a commercial operating temperature range of 0 to 70°C.

CY25200 Pin Summary

Name	Pin Number	Description
XIN	1	**Crystal Input or Reference Clock Input**.
XOUT	16	**Crystal Output.** Leave this pin floating if external clock is used.
VDD	2	3.3V Power supply for digital logic and SSCLK5/6 clock drives.
AVDD	3	3.3V analog–PLL power supply
VSS	13	Ground
AVSS	5	Analog ground
VDDL	11	2.5V or 3.3V power supply for SSCLK1/2/3/4 clock drives
VSSL	6	VDDL power supply ground
SSCLK1	7	Programmable Spread Spectrum Clock Output at VDDL Level (2.5V or 3.3V)
SSCLK2	8	Programmable Spread Spectrum Clock Output at VDDL Level (2.5V or 3.3V)
SSCLK3	9	Programmable Spread Spectrum Clock Output at VDDL Level (2.5V or 3.3V)
SSCLK4	12	Programmable Spread Spectrum Clock Output at VDDL Level (2.5V or 3.3V)
SSCLK5/REFOUT/CP2	14	Programmable Spread Spectrum Clock or Buffered Reference Output at VDD Level (3.3V) or Control pin, CP2
SSCLK6/REFOUT/CP3	15	Programmable Spread Spectrum Clock or Buffered Reference Output at VDD Level (3.3V) or Control pin, CP3
CP0[1]	4	Control Pin 0
CP1[1]	10	Control Pin 1

Note:
1. Pins can be programmed to be any of the following control signals: OE: Output Enable, OE = 1 all the SSCLK outputs are enabled, PD#: Powerdown, PD# = 0, all the SSCLK outputs are three-stated and the part enters a low-power state, SSON: Spread Spectrum Control (SSON = 0, No Spread and SSON = 1, Spread Signal), CLKSEL: SSCLK Output Frequency Select. Please see page 3 for control pins programming option.

Table 1. Fixed Function Pins

Pin Function	Output Clock Functions and Frequency				Input Frequency	C_{XIN} and C_{XOUT}	Spread Percent	Frequency Modulation
Pin Name	SSCLK1	SSCLK2	SSCLK3	SSCLK4	XIN and XOUT	XIN and XOUT	SSCLK[1:6]	SSCLK[1:6]
Pin#	7	8	9	12	1 and 16	1 and 16	7,8,9,12,14,15	7,8,9,12,14,15
Units	MHz	MHz	MHz	MHz	MHz	pF	%	kHz
Program Value CLKSEL = 0	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**	**31.5**
Program Value CLKSEL = 1	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**				

Table 2. Multi-function Pins

Pin Function	Output Clock /REFOUT /OE/SSON/CLKSEL		OE/PD#/SSON/CLKSEL	
Pin Name	SSCLK5/REFOUT/CP2	SSCLK6/REFOUT/CP3	CP0	CP1
Pin#	14	15	4	10
Units	MHz	MHz	N/A	N/A
Program Value CLKSEL = 0	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**
Program Value CLKSEL = 1	**ENTER DATA**	**ENTER DATA**		

Programming Description

Customers planning to use the CY25200 need to provide the programming information described as “ENTER DATA” in *Table 1 and Table 2,* then should contact local Cypress Sales.

Additional information on the CY25200 can be obtained from the Cypress web site at www.cypress.com.

Product Functions

Control Pins (CP0, CP1, CP2 and CP3)

There are four control signals available through programming of pins 4, 10, 14 and 15.

CP0 (pin 4) and CP1 (pin10) are specifically designed to function as control pins. However pins 14 (SSCLK5/REFOUT/CP2) and 15 (SSCLK6/REFOUT/CP3) are multi-functional and can be programmed to be a control signal or an output clock (SSCLK or REFOUT). All of the control pins, CP0, CP1, CP2 and CP3 are programmable and can be programmed to have only one of the following functions:

- Output Enable (OE), if OE = 1, all the SSCLK or REFOUT outputs are enabled
- SSON, Spread spectrum control, 1 = spread on and 0 = spread off
- CLKSEL, SSCLK output frequency select
- PD#, Active Low, PD# = 0, all the outputs are three-stated and the part enters a low-power state
- The last control signal is the Power down (PD#) that can be implemented only through programming CP0 or CP1 (CP2 and CP3 can not be programmed as PD#). Here is an example with 3 control pins,
- CLKIN = 33MHz
- SSCLK1/2/3/4 = 100MHz with ±1% Spread
- SSCLK 5 = REFOUT(33MHz)
- CP0 (Pin 4) = PD#
- CP1 (Pin 10) = OE
- CP3 (pin 15) = SSON

The pinout for the above example is shown in *Figure 1*.

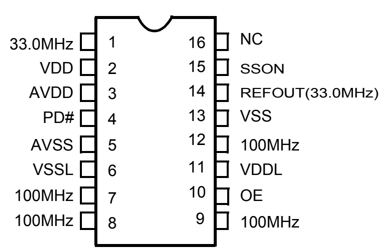


Figure 1.

The CLKSEL control pin enables the user to change the output frequency from one frequency (e.g., frequency A) to another frequency (e.g., frequency B). These must be related frequencies that can be derived off of a common VCO frequency, e.g., 33.333 MHz and 66.666 MHz can both be derived from a VCO = 400 MHz and dividing it down by 12 and 6 respectively. *Table 3* shows an example of how this can be implemented. The VCO frequency range is 100–400MHz. The CY25200 has two separate dividers, Divider 1 and Divider 2, these two can be loaded to have any number between 2 and 130 providing two different but related frequencies as explained above.

In the above example SSCLK5 (pin 14) and SSCLK6(pin 15) are used as output clocks, however they could have been used as control signals. See *Figure 2* for the pinout.

Input Frequency (XIN, pin 1 and XOUT, pin 16)

The input to the CY25200 can be a crystal or a clock. The input frequency range for crystals is 8 to 30 MHz, and for clock signal is 8 to 166 MHz.

C_{XIN} and C_{XOUT} (pin 1 and pin 16)

The load capacitors at pin 1 ($\mathbf{C_{XIN}}$) and pin 16 ($\mathbf{C_{XOUT}}$) can be programmed from 12 pF to 60 pF with 0.5-pF increments. The programmed value of these on-chip crystal load capacitors are the same (XIN = XOUT = 12 to 60 pF).

The required values of $\mathbf{C_{XIN}}$ and $\mathbf{C_{XOUT}}$ for matching crystal load (CL) can be calculated using the following formula:

$C_{XIN} = C_{XOUT} = 2C_L - C_P$

Where C_L is the crystal load capacitor as specified by the crystal manufacturer and C_P is the parasitic PCB capacitance.

For example, if a fundamental 16-MHz crystal with C_L of 16 pF is used and C_P is 2 pF, C_{XIN} and C_{XOUT} can be calculated as:

$C_{XIN} = C_{XOUT} = (2 \times 16) - 2 = 30$ pF.

If using a driven reference clock, set C_{XIN} and C_{XOUT} to the minimum value 12 pF.

Output Frequency (SSCLK1 through SSCLK6 Outputs)

All of the SSCLK outputs are produced by synthesizing the input reference frequency using a PLL and modulating the VCO frequency. SSCLK[1:4] can be programmed to be only output clocks (SSCLK). SSCLK5 and SSCLK6 can also be programmed to function the same as SSCLK[1:4] or a buffered copy of the input reference (REFOUT) or they can be programmed to be a control pin as discussed in the control pins section. To utilize the 2.5V output drive option on SSCLK[1:4], VDDL must be connected to a 2.5V power supply (SSCLK[1:4] outputs are powered by VDDL). When using the 2.5V output drive option, the maximum output frequency on SSCLK[1:4] is 166MHz.

Spread Percentage (SSCLK1 through SSCLK6 Outputs)

The SSCLK frequency can be programmed at any percentage value from ±0.25% to ±2.5% for Center Spread and from –0.5% to –5.0% Down Spread.

Frequency Modulation

The frequency modulation is programmed at 31.5 kHz for all SSCLK frequencies from 3 to 200 MHz. Contact the factory if a higher modulation frequency is required.

Table 3. Using Clock Select, CLKSEL Control Pin

Input Freq. (MHz)	CLKSEL (Pin 4)	SSCLK1 (Pin 7)	SSCLK2 (Pin 8)	SSCLK3 (Pin 9)	SSCLK4 (Pin 12)	REFOUT (Pin 14)	REFOUT (Pin 15)
14.318	CLKSEL = 0	33.33	33.33	33.33	33.33	14.318	14.318
	CLKSEL = 1	66.66	66.66	66.66	66.66	14.318	14.318

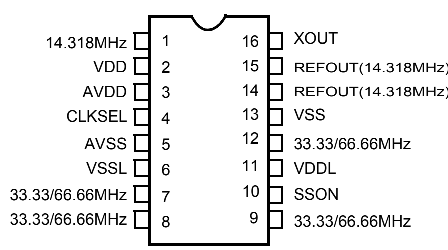
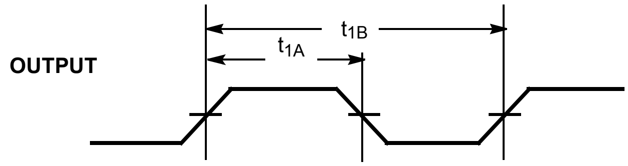


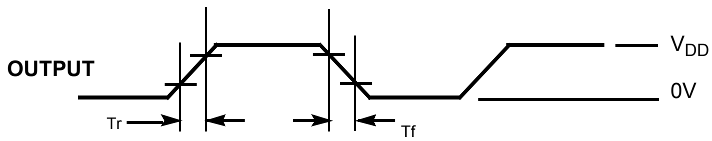
Figure 2. *Table 3* Configuration Pinout

Switching Waveforms

Duty Cycle Timing (DC = t_{1A}/t_{1B})

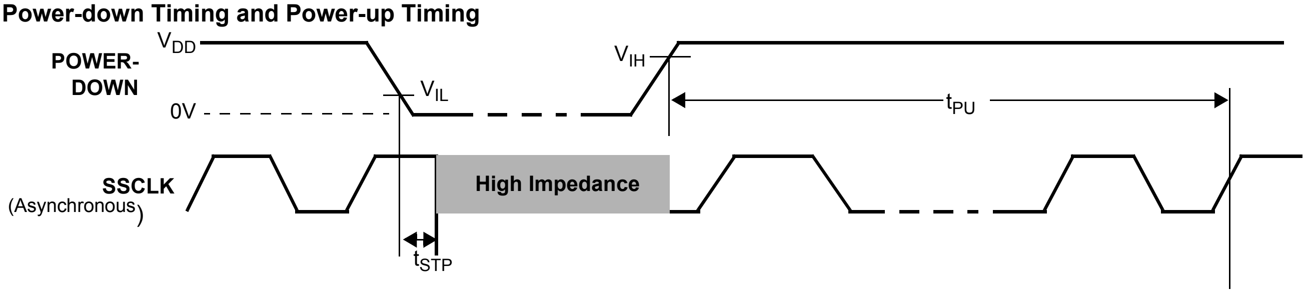


Output Rise/Fall Time (SSCLK and REFCLK)

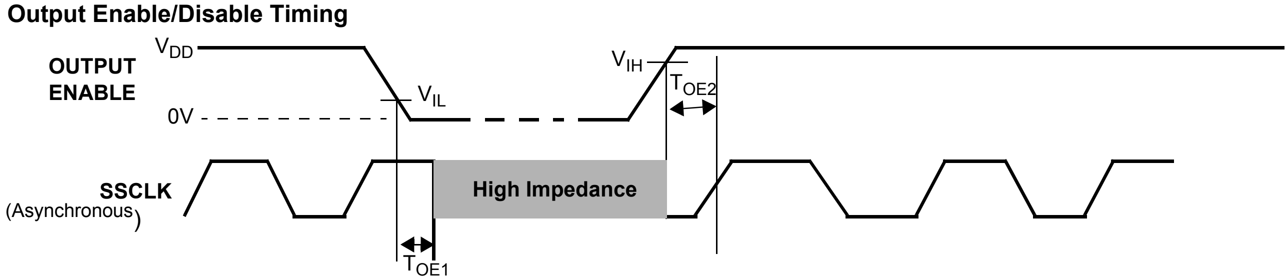


Output Rise time (Tr) = (0.6 x V_{DD})/SR1 (or SR3)
Output Fall time (Tf) = (0.6 x V_{DD})/SR2 (or SR4)
Refer to AC Electrical Characteristics table for SR (Slew Rate) values.

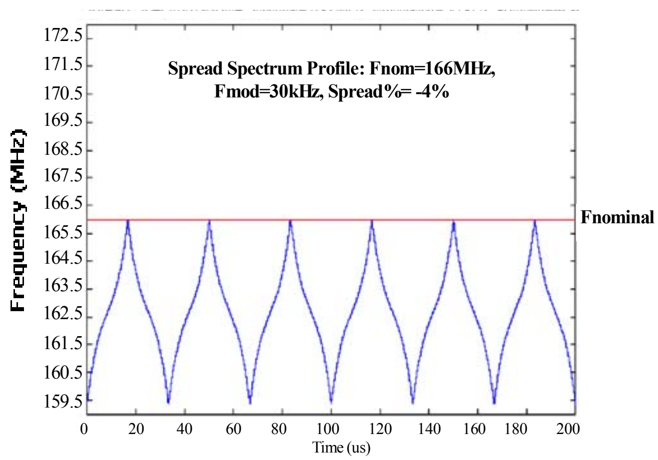
Power-down Timing and Power-up Timing

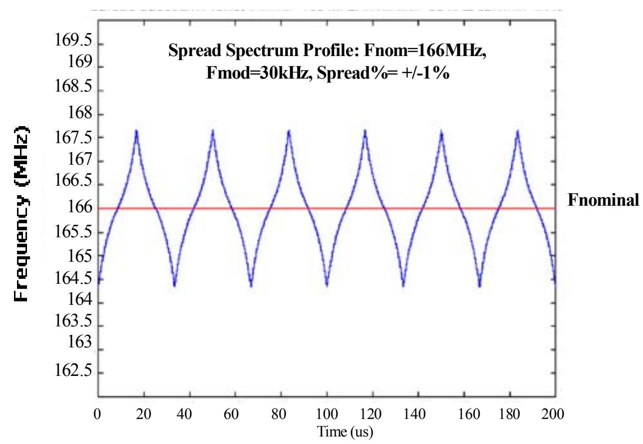


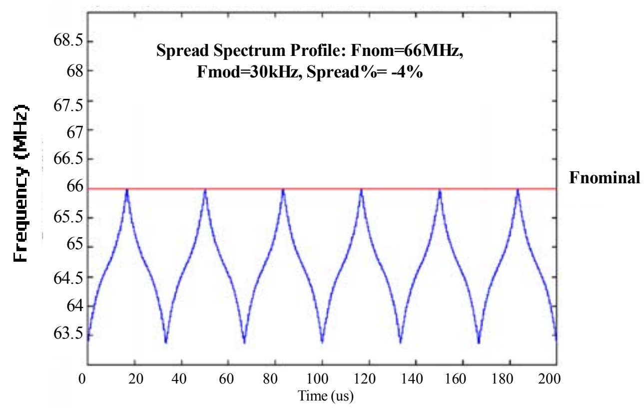
Output Enable/Disable Timing

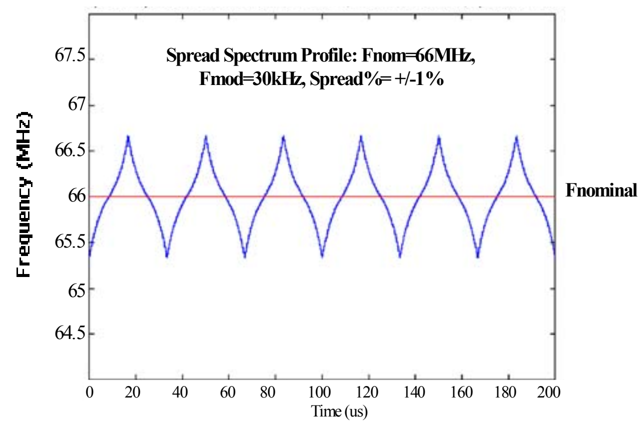


Informational Graphs [2]









Note:

2. The “Informational Graphs” are meant to convey the typical performance levels. No performance specifications is implied or guaranteed. Refer to the tables on pages 4 and 5 for device specifications.

Absolute Maximum Rating

Supply Voltage (VDD) ....–0.5 to +7.0V

DC Input Voltage .... –0.5V to V_{DD} + 0.5

Storage Temperature (Non-condensing).....–55°C to +125°C

Junction Temperature .... –40°C to +125°C

Data Retention @ Tj = 125°C.............................. > 10 Years

Package Power Dissipation..................................... 350 mW

Static Discharge Voltage... ≥ 2000V
(per MIL-STD-883, Method 3015)

Recommended Crystal Specifications

Parameter	Description	Comments	Min.	Typ.	Max.	Unit
F_{NOM}	Nominal Crystal Frequency	Parallel resonance, fundamental mode, AT cut	8		30	MHz
C_{LNOM}	Nominal Load Capacitance	Internal load caps	6		30	pF
R_1	Equivalent Series Resistance (ESR)	Fundamental mode			25	Ω
R_3/R_1	Ratio of Third Overtone Mode ESR to Fundamental Mode ESR	Ratio used because typical R_1 values are much less than the maximum spec	3			
DL	Crystal Drive Level	No external series resistor assumed		0.5	2	mW

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	3.135	3.3	3.465	V
V_{DDLHI}	Operating Voltage	3.135	3.3	3.465	V
V_{DDLLO}	Operating Voltage	2.375	2.5	2.625	V
T_{AC}	Ambient Commercial Temp	0	–	70	°C
C_{LOAD}	Max. Load Capacitance V_{DD}/V_{DDL} = 3.3V	–	–	15	pF
C_{LOAD}	Max. Load Capacitance V_{DDL} = 2.5V	–	–	15	pF
$F_{SSCLK\text{-}HighVoltage}$	SSCLK1/2/3/4/5/6 when V_{DD} = A_{VDD} = V_{DDL} = 3.3 V	3	–	200	MHz
$F_{SSCLK\text{-}LowVoltage}$	SSCLK5/6 when V_{DD} = 3.3.V and V_{DDL} = 2.5V	3	–	166	MHz
R_{EFOUT}	REFOUT when V_{DD} = A_{VDD} = 3.3.V and V_{DDL} = 3.3V or 2.5V	8	–	166	MHz
f_{REF1}	Clock Input	8	–	166	MHz
f_{REF2}	Crystal Input	8	–	30	MHz
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

DC Electrical Specifications

Parameter[4]	Name	Description	Min.	Typ.	Max.	Unit
$I_{OH3.3}$	Output High Current	V_{OH} = V_{DD} – 0.5V, V_{DD}/V_{DDL} = 3.3V	10	12	–	mA
$I_{OL3.3}$	Output Low Current	V_{OL} = 0.5V, V_{DD}/V_{DDL} = 3.3V	10	12	–	mA
$I_{OH2.5}$	Output High Current	V_{OH} = V_{DDL} – 0.5V, V_{DDL} = 2.5V	8	16	–	mA
$I_{OL2.5}$	Output Low Current	V_{OL} = 0.5V, V_{DDL} = 2.5V	8	16	–	mA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7	–	1.0	V_{DD}
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}	0	–	0.3	V_{DD}
I_{VDD}[5]	Supply Current	AV_{DD}/V_{DD} Current	–	–	33	mA
$I_{VDDL2.5}$[5]	Supply Current	V_{DDL} Current (V_{DDL} = 2.625V)	–	–	20	mA
$I_{VDDL3.3}$[5]	Supply Current	V_{DDL} Current (V_{DDL} = 3.465V)	–	–	26	mA
I_{DDS}	Power-Down Current	V_{DD} = V_{DDL} = AV_{DD} = 3.465V	–	–	50	uA
I_{OHZ} I_{OLZ}	Output Leakage	V_{DD} = V_{DDL} = AV_{DD} = 3.465V	–	–	10	uA

Notes:
3. Rated for 10 years.
4. Not 100% tested, guaranteed by design.
5. I_{VDD} currents specified for SSCLK1/2/3/4/5/6 = 33.33 MHz with CLKIN = 14.318 MHz and 15 pF on all the output clocks.

AC Electrical Specifications

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	SSCLK, Measured at $V_{DD}/2$	45	50	55	%
	Output Duty Cycle	REFCLK, Measured at $V_{DD}/2$ Duty Cycle of CLKIN = 50%.	40	50	60	%
SR1	Rising/Falling Edge Slew Rate	SSCLK1/2/3/4 < 100 MHz, $V_{DD} = V_{DDL}$ = 3.3V	0.6	–	2.0	V/ns
SR2	Rising/Falling Edge Slew Rate	SSCLK1/2/3/4 ≥ 100 MHz, $V_{DD} = V_{DDL}$ = 3.3V	0.8	–	3.5	V/ns
SR3	Rising/Falling Edge Slew Rate	SSCLK1/2/3/4 < 100 MHz, $V_{DD} = V_{DDL}$ = 2.5V	0.5	–	2.2	V/ns
SR4	Rising/Falling Edge Slew Rate	SSCLK1/2/3/4 ≥ 100 MHz, $V_{DD} = V_{DDL}$ = 2.5V	0.6	–	3.0	V/ns
SR5	Rising/Falling Edge Slew Rate	SSCLK5/6 < 100 MHz, $V_{DD} = V_{DDL}$ = 3.3V	0.6	–	1.9	V/ns
SR6	Rising/Falling Edge Slew Rate	SSCLK5/6 ≥ 100 MHz, $V_{DD} = V_{DDL}$ = 3.3V	1.0	–	2.9	V/ns
T_{CCJ1}	Cycle-to-Cycle Jitter SSCLK1/2/3/4	CLKIN = SSCLK1/2/3/4 = 166MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL}$ = 3.3V	–	–	110	ps
		CLKIN = SSCLK1/2/3/4 = 66.66 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL}$ = 3.3V	–	–	170	ps
		CLKIN = SSCLK1/2/3/4 = 33.33 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL}$ = 3.3V	–	–	140	ps
		CLKIN = SSCLK1/2/3/4 = 14.318MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL}$ = 3.3V	–	–	290	
T_{CCJ2}	Cycle-to-Cycle Jitter SSCLK5/6=REFOUT	CLKIN = SSCLK1/2/3/4 = 166 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL}$ = 3.3V	–	–	100	ps
		CLKIN = SSCLK1/2/3/4 = 66.66 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL}$ = 3.3V	–	–	120	ps
		CLKIN = SSCLK1/2/3/4 = 33.33 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL}$ = 3.3V	–	–	180	ps
		CLKIN = SSCLK1/2/3/4 = 14.318 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL}$ = 3.3V	–	–	180	
T_{CCJ3}	Cycle-to-Cycle Jitter SSCLK1/2/3/4	CLKIN = SSCLK1/2/3/4 = 166 MHz, ±2% spread and SSCLK5/6 = REFOUT, V_{DD} = 3.3V, V_{DDL} = 2.5V	–	–	110	ps
		CLKIN = SSCLK1/2/3/4 = 66.66MHz, ±2% spread and SSCLK5/6 = REFOUT, V_{DD} = 3.3V, V_{DDL} = 2.5V	–	–	170	ps
		CLKIN = SSCLK1/2/3/4 = 33.33 MHz, ±2% spread and SSCLK5/6 = REFOUT, V_{DD} = 3.3V, V_{DDL} = 2.5V	–	–	190	ps
		CLKIN = SSCLK1/2/3/4 = 14.318 MHz, ±2% spread and SSCLK5/6 = REFOUT, V_{DD} = 3.3V, V_{DDL} = 2.5V	–	–	330	
T_{CCJ4}	Cycle-to-Cycle Jitter SSCLK5/6=REFOUT	CLKIN = SSCLK1/2/3/4 = 166 MHz, ±2% spread and SSCLK5/6 = REFOUT, V_{DD} = 3.3V, V_{DDL} = 2.5V	–	–	90	ps
		CLKIN = SSCLK1/2/3/4 = 66.66 MHz, ±2% spread and SSCLK5/6 = REFOUT, V_{DD} = 3.3V, V_{DDL} = 2.5V	–	–	110	ps
		CLKIN = SSCLK1/2/3/4 = 33.33 MHz, ±2% spread and SSCLK5/6 = REFOUT, V_{DD} = 3.3V, V_{DDL} = 2.5V	–	–	160	ps
		CLKIN = SSCLK1/2/3/4 = 14.318MHz, ±2% spread and SSCLK5/6 = REFOUT, V_{DD} = 3.3V, V_{DDL} = 2.5V	–	–	150	
t_{STP}	Power-down Time (pin3 = PD#)	Time from falling edge on PD# to stopped outputs (Asynchronous)	–	150	300	ns
T_{OE1}	Output Disable Time (pin3 = OE)	Time from falling edge on OE to stopped outputs (Asynchronous)	–	150	300	ns
T_{OE2}	Output Enable Time (pin3 = OE)	Time from rising edge on OE to outputs at a valid frequency (Asynchronous)	–	150	300	ns
F_{MOD}	Spread Spectrum Modulation Frequency	SSCLK1/2/3/4/5/6	30.0	31.5	33.0	kHz

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
t_{PU1}	Power-up Time, Crystal is used	Time from rising edge on PD# to outputs at valid frequency (Asynchronous)	–	3	5	ms
t_{PU2}	Power-up Time, Reference clock is used	Time from rising edge on PD# to outputs at valid frequency (Asynchronous)	–	2	3	ms

Ordering Information

Ordering Code[6]	Package Type	Temperature Operating Range
CY25200ZXC_XXXW	16-lead TSSOP (Lead Free)	Commercial, 0 to 70°C
CY25200ZXC_XXXWT	16-lead TSSOP- Tape and Reel (Lead Free)	Commercial, 0 to 70°C

16-lead TSSOP Package Characteristics

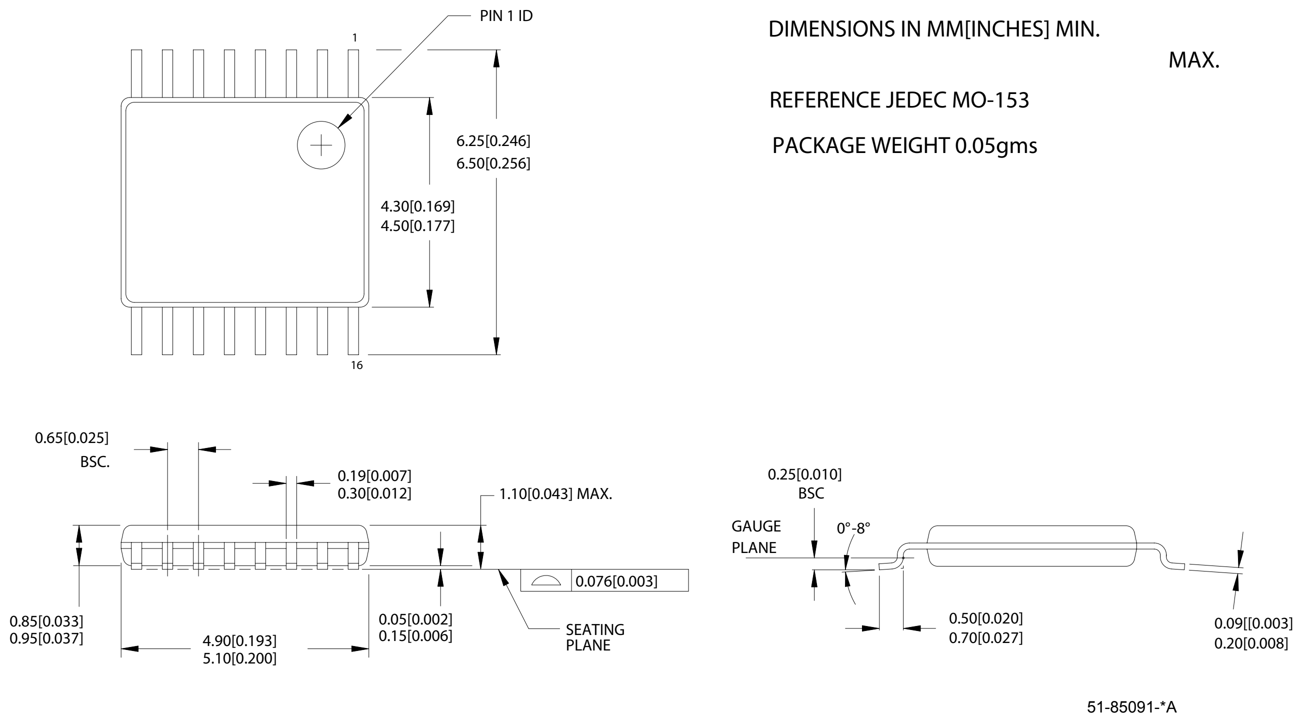
Parameter	Name	Value	Unit
θ_{JA}	theta JA	115	°C/W

Notes:

6. "XXX" denotes the assigned product dash number. "W" denotes the different revisions of the product.

Package Drawing and Dimension

16-lead TSSOP 4.40 MM Body Z16.173



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Document History Page

Document Title: CY25200 Programmable Spread Spectrum Clock Generator for EMI Reduction Document Number: 38-07633				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	204243	See ECN	RGL	New Data Sheet
*A	220043	See ECN	RGL	Minor Change: Corrected letter assignment in the ordering info for Lead Free.