



3.3V CMOS 16-BIT BUS TRANSCIVER AND REGISTER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH16646

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP,
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, Normal Range
- $V_{CC} = 2.7\text{V}$ to 3.6V , Extended Range
- $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$
- CMOS power levels ($0.4\mu\text{W}$ typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCH16646:

- High Output Drivers: $\pm 24\text{mA}$
- Suitable for heavy loads

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

DESCRIPTION:

This 16-bit bus transceiver is built using advanced dual metal CMOS technology. The ALVCH16646 can be used as two 8-bit transceivers or

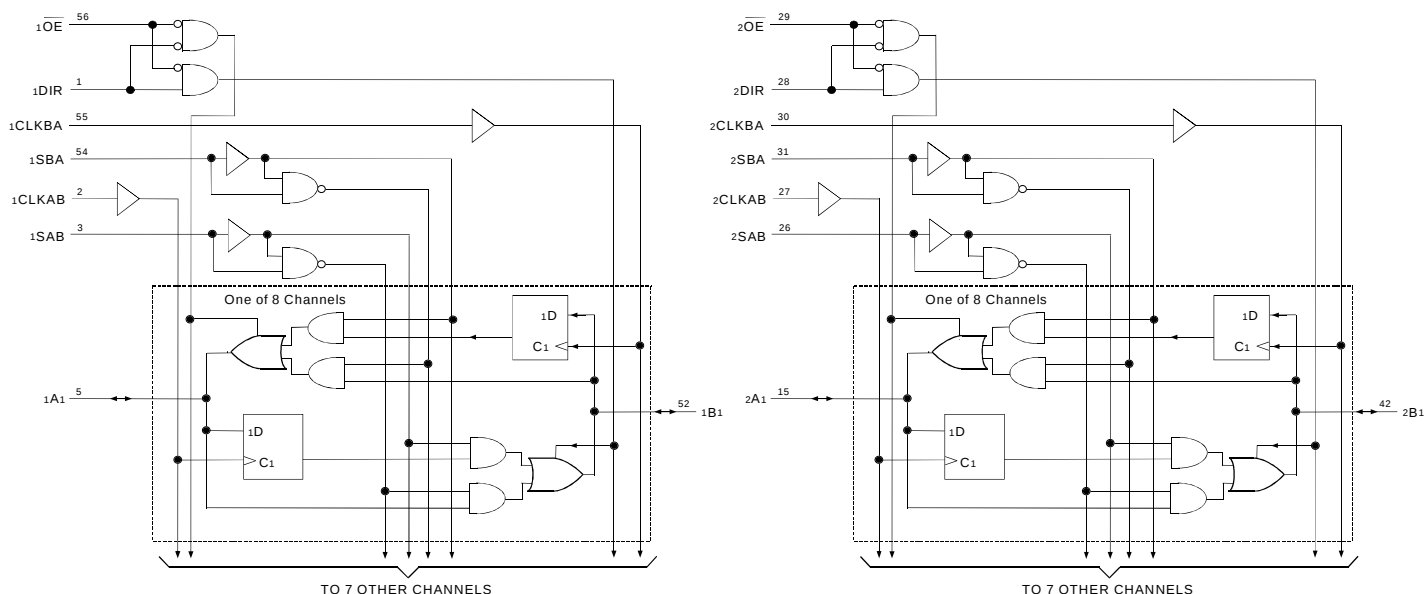
one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input.

Output-enable ($\overline{\text{OE}}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or both. The select control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when $\overline{\text{OE}}$ is low. In the isolation mode ($\overline{\text{OE}}$ high), A data may be stored in one register and/or B data may be stored in the other register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

The ALVCH16646 has been designed with a $\pm 24\text{mA}$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16646 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

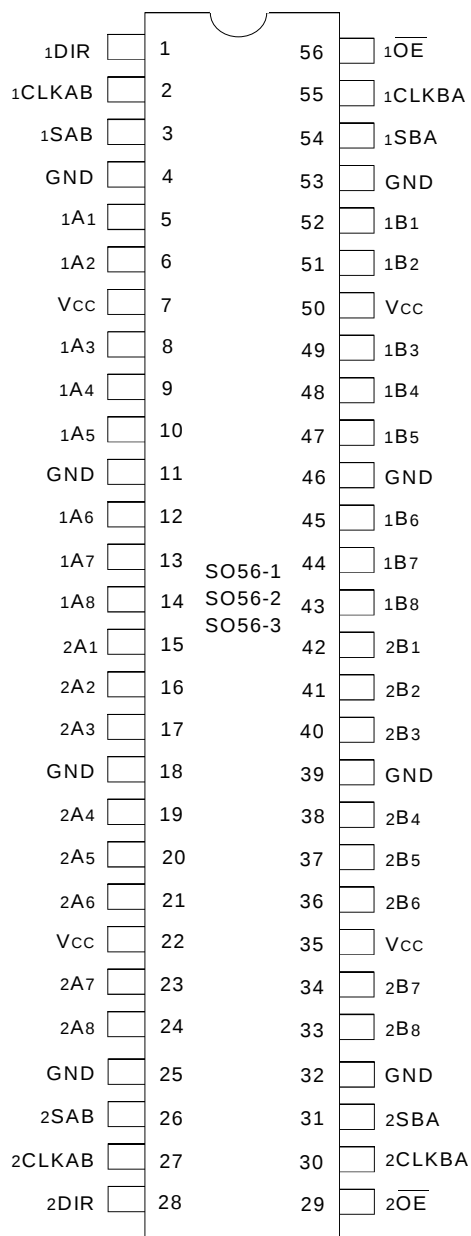
Functional Block Diagram



EXTENDED COMMERCIAL TEMPERATURE RANGE

APRIL 1999

PIN CONFIGURATION



SSOP/TSSOP/TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	– 0.5 to + 4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	– 0.5 to Vcc + 0.5	V
TSTG	Storage Temperature	– 65 to + 150	°C
IOUT	DC Output Current	– 50 to + 50	mA
IIK	Continuous Clamp Current, VI < 0 or VI > Vcc	± 50	mA
IOK	Continuous Clamp Current, Vo < 0	– 50	mA
ICC	Continuous Current through each Vcc or GND	±100	mA

NEW16link

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Vcc terminals.
- All terminals except Vcc.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	5	7	pF
COUT	Output Capacitance	VOUT = 0V	7	9	pF
CIO	I/O Port Capacitance	VIN = 0V	7	9	pF

NEW16link

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
xAx	Data Register A Inputs ⁽¹⁾ Data Register B Outputs
xBx	Data Register B Inputs ⁽¹⁾ Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xOE	Output Enable Inputs
xDIR	Direction-control Inputs

NOTE:

- These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE (1)

Inputs						Data I/O		Operation or Function
x $\overline{OE}$	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
X	X	↑	X	X	X	Input	Unspecified ⁽²⁾	Store A, B unspecified ⁽²⁾
X	X	X	↑	X	X	Unspecified ⁽²⁾	Input	Store B, A unspecified ⁽²⁾
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition
- The data output functions may be enabled or disabled by various signals at the x $\overline{OE}$ or xDIR inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = – 40°C to +85°C

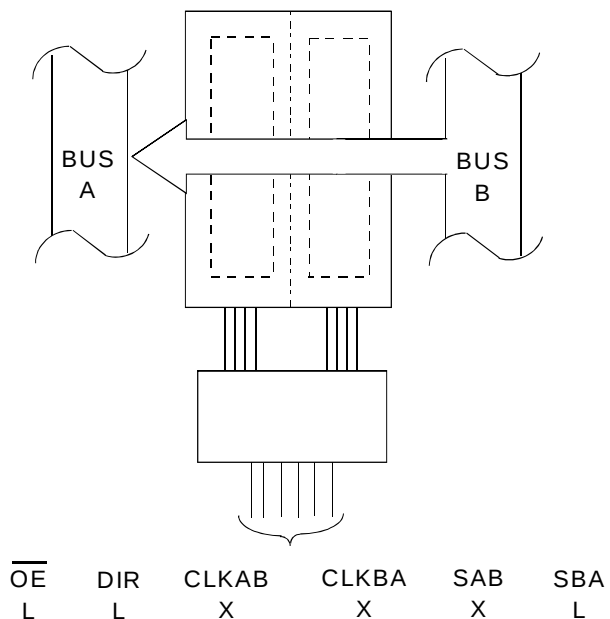
Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
VIH	Input HIGH Voltage Level	VCC = 2.3V to 2.7V		1.7	—	—	V
		VCC = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	VCC = 2.3V to 2.7V		—	—	0.7	V
		VCC = 2.7V to 3.6V		—	—	0.8	
IiH	Input HIGH Current	VCC = 3.6V	Vi = VCC	—	—	± 5	μA
IiL	Input LOW Current	VCC = 3.6V	Vi = GND	—	—	± 5	
IoZH IoZL	High Impedance Output Current (3-State Output pins)	VCC = 3.6V	Vo = VCC	—	—	± 10	μA
			Vo = GND	—	—	± 10	μA
VIK	Clamp Diode Voltage	VCC = 2.3V, IIN = – 18mA		—	– 0.7	– 1.2	V
VH	Input Hysteresis	VCC = 3.3V		—	100	—	mV
ICCL ICCH IC CZ	Quiescent Power Supply Current	VCC = 3.6V VIN = GND or VCC		—	0.1	40	μA
ΔICC	Quiescent Power Supply Current Variation	One input at VCC – 0.6V, other inputs at VCC or GND		—	—	750	μA

NOTE:

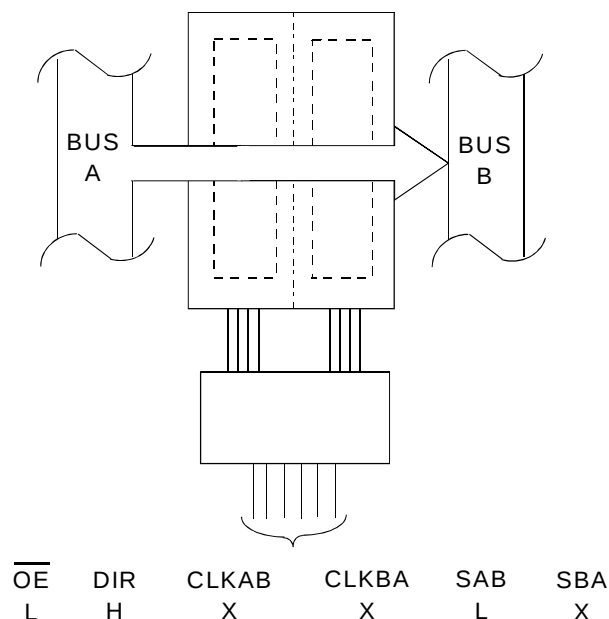
- Typical values are at VCC = 3.3V, +25°C ambient.

NEW16link

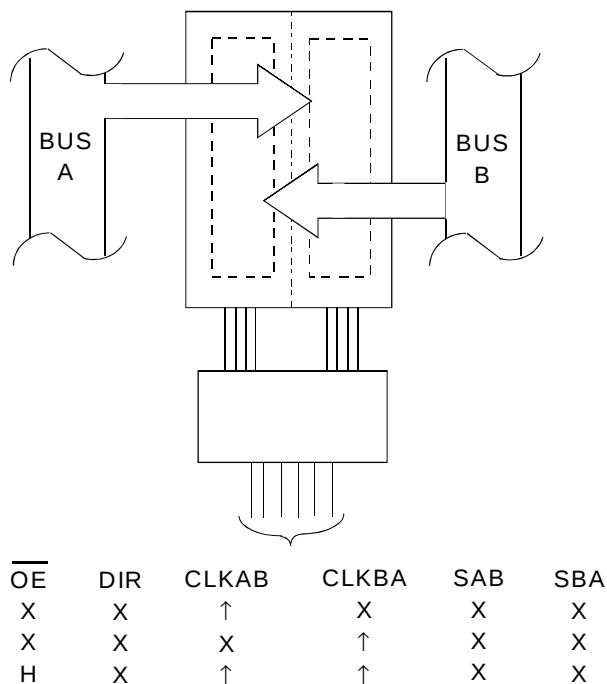
BUS MANAGEMENT FUNCTIONS



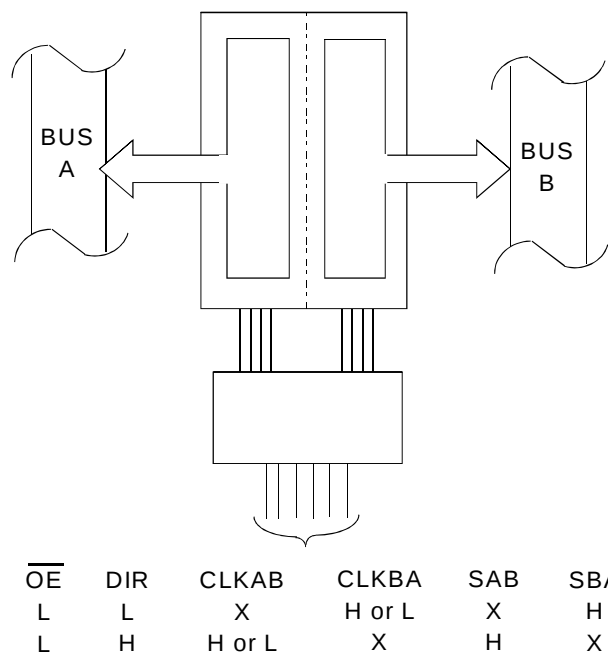
REAL-TIME TRANSFER BUS B TO BUS A



REAL-TIME TRANSFER BUS A TO BUS B



STORAGE FROM A, B, OR A AND B



TRANSFER STORED DATA TO A AND/OR B

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
IBHH IBHL	Bus-Hold Input Sustain Current	V _{CC} = 3.0V	V _I = 2.0V	– 75	—	—	μA
			V _I = 0.8V	75	—	—	
IBHH IBHL	Bus-Hold Input Sustain Current	V _{CC} = 2.3V	V _I = 1.7V	– 45	—	—	μA
			V _I = 0.7V	45	—	—	
IBHHO IBHLO	Bus-Hold Input Overdrive Current	V _{CC} = 3.6V	V _I = 0 to 3.6V	—	—	± 500	μA

NEW16link

NOTES:

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = – 0.1mA	V _{CC} – 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = – 6mA	2	—	
		V _{CC} = 2.3V	I _{OH} = – 12mA	1.7	—	
		V _{CC} = 2.7V		2.2	—	
		V _{CC} = 3.0V		2.4	—	
		V _{CC} = 3.0V	I _{OH} = – 24mA	2	—	
VOL	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		V _{CC} = 2.7V	I _{OL} = 12mA	—	0.4	
		V _{CC} = 3.0V	I _{OL} = 24mA	—	0.55	

NEW16link

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	V _{CC} = 2.5V ± 0.2V	V _{CC} = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	C _L = 0pF, f = 10MHz	39	43	pF
CPD	Power Dissipation Capacitance Outputs disabled		10	12	pF

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}		150	—	150	—	150	—	MHz
t _{PLH} t _{PHL}	Propagation Delay xAx to xBx or xBx to xAx	1	4.8	—	4.5	1	3.9	ns
t _{PLH} t _{PHL}	Propagation Delay xCLKAB to xBx or xCLKBA to xAx	1	5.6	—	5.2	1	4.5	ns
t _{PLH} t _{PHL}	Propagation Delay xSBA or xAx or xSAB to xBx	1	6.8	—	6.4	1	5.3	ns
t _{PZH} t _{PZL}	Output Enable Time xOE to xAx or xBx	1	6.5	—	6.2	1	5.1	ns
t _{PZH} t _{PZL}	Output Enable Time xDIR to xAx or xBx	1	7.8	—	6.2	1	5.1	ns
t _{PHZ} t _{PLZ}	Output Disable Time xOE to xAx or xBx	1.6	5.7	—	5	1.4	4.7	ns
t _{PHZ} t _{PLZ}	Output Disable Time xDIR to xAx or xBx	1.5	6.5	—	6	1.1	5.3	ns
t _{SU}	Setup Time, xAx before xCLKAB↑ or xBx before xCLKBA↑	1.6	—	1.7	—	1.4	—	ns
t _H	Hold Time, xAx after xCLKAB↑ or xBx after xCLKBA↑	0.6	—	0.4	—	0.7	—	ns
t _w	Pulse Width, xCLKAB or xCLKBA HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
t _{SK(0)}	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

NOTES:

1. See test circuits and waveforms. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

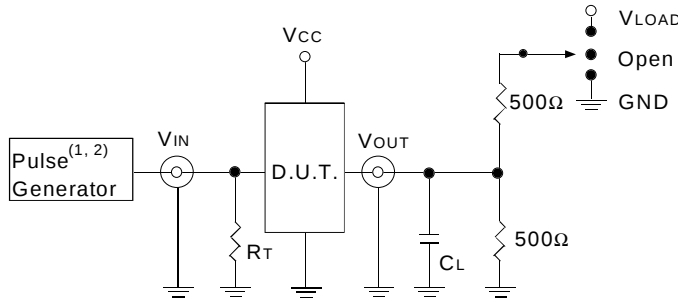
TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	V _{CC} (1)= 3.3V±0.3V	V _{CC} (1)= 2.7V	V _{CC} (2)= 2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

NEW16link

TEST CIRCUITS FOR ALL OUTPUTS



ALVC Link

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

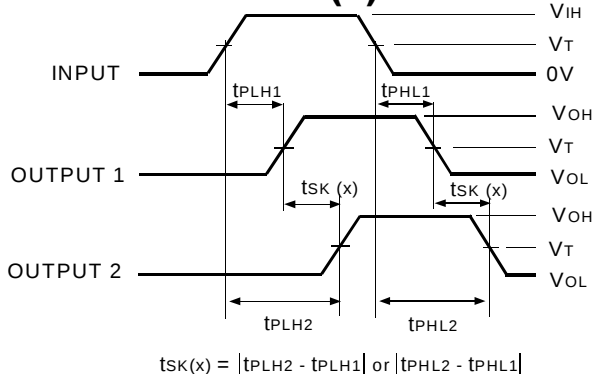
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

NEW16link

OUTPUT SKEW - t_{SK} (x)

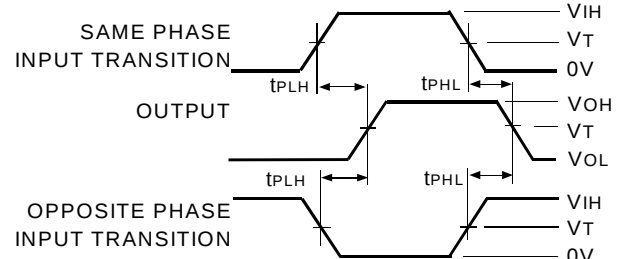


ALVC Link

NOTES:

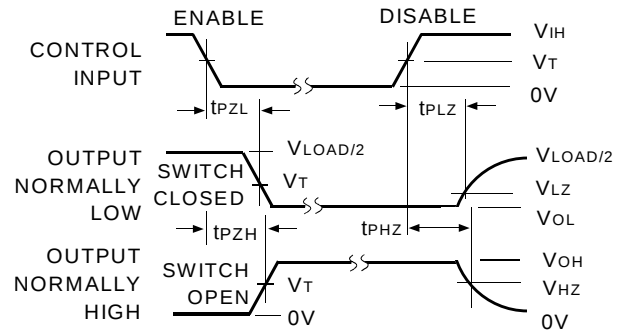
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



ALVC Link

ENABLE AND DISABLE TIMES

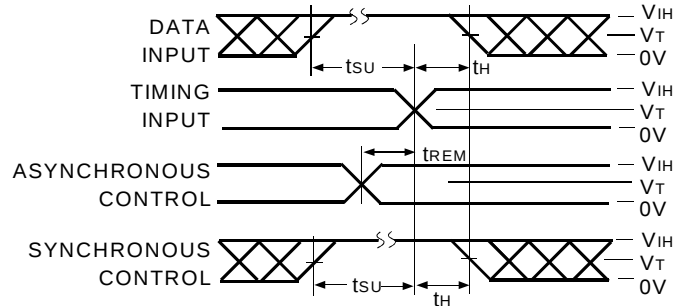


ALVC Link

NOTE:

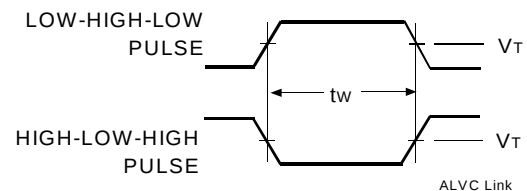
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



ALVC Link

PULSE WIDTH



ALVC Link

ORDERING INFORMATION

IDT	XX	ALVC	X	XX	XXX	XX	
Temp. Range	Bus-Hold	Family	Device Type	Package			
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
				646			16-Bit Bus Transceiver and Register with 3-State Outputs
			16				Double-Density with Resistors, $\pm 24\text{mA}$
		H					Bus-Hold
				74			-40°C to $+85^{\circ}\text{C}$



CORPORATE HEADQUARTERS
 2975 Stender Way
 Santa Clara, CA 95054

for SALES:
 800-345-7015 or 408-727-6116
 fax: 408-492-8674
www.idt.com*

*To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.
 The IDT logo is a registered trademark of Integrated Device Technology, Inc.