

3 V, SUPER MINIMOLD MEDIUM POWER SI MMIC AMPLIFIER

FEATURES

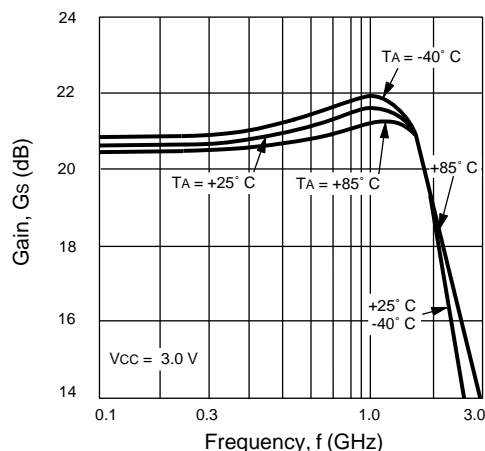
- **HIGH GAIN:** 21 dB at 900 to 1500 MHz Typical
- **HIGH OUTPUT POWER:** $P_{SAT} = +12.5$ dBm at 900 MHz
+11 dBm at 1500 MHz
- **LOW BIAS VOLTAGE:** 3.0 V Typical, 2.7 V Minimum
- **SUPER SMALL PACKAGE:** SOT-363
- **TAPE AND REEL PACKAGING OPTION AVAILABLE**

DESCRIPTION

The UPC2771TB is a Silicon Monolithic integrated circuit which is manufactured using the NESAT™ III process. The NESAT III process produces transistors with f_T approaching 20 GHz. The UPC2771TB is pin compatible and has comparable performance as the larger UPC2771T, so it is suitable for use as a replacement to help reduce system size. The IC is housed in a 6 pin super minimold or SOT-363 package. Operating on a 3 volt supply, this IC is ideally suited for hand-held, portable designs.

NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.

GAIN vs. FREQUENCY AND TEMPERATURE



ELECTRICAL CHARACTERISTICS (TA = 25°C, ZL = ZS = 50 Ω, VCC = 3.0 V)

PART NUMBER PACKAGE OUTLINE			UPC2771TB S06		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
I _{CC}	Circuit Current (no signal)	mA		36	45
G _s	Small Signal Gain, f = 900 MHz f = 1500 MHz	dB dB	19 18	21 21	24 24
f _U	Upper Limit Operating Frequency (The gain at f _U is 3 dB down from the gain at 100 MHz)	GHz	1.8	2.2	
P _{1dB}	1 dB Compressed Output Power, f = 900 MHz f = 1500 MHz	dBm dBm	+9 +7	+11.5 +9.5	
P _{SAT}	Saturated Output Power, f = 900 MHz f = 1500 MHz	dBm dBm		+12.5 +11	
NF	Noise Figure, f = 900 MHz f = 1500 MHz	dB dB		6 6	7.5 7.5
RL _{IN}	Input Return Loss, f = 900 MHz f = 1500 MHz	dB dB	10 10	14 14	
RL _{OUT}	Output Return Loss, f = 900 MHz f = 1500 MHz	dB dB	6.5 5.5	9.0 8.5	
ISOL	Isolation, f = 900 MHz f = 1500 MHz	dB dB	25 25	30 30	
OIP3	SSB Output Third Order Intercept Point f = 900, 902 MHz, P _{OUT} = +4 dBm f = 1500, 1502 MHz, P _{OUT} = +4 dBm	dBm dBm		+13 +10	
P _{ADJ1}	Adjacent Channel Power 1, f = 900 mHz, π/4 QPSK wave ¹ , P _{OUT} = +7 dBm Δf = ± 50 kHz Δf = ± 100 kHz	dBc dBc		-61 -72	
P _{ADJ2}	Adjacent Channel Power 2, f = 1.5 GHz, π/4 QPSK wave ¹ , P _{OUT} = +7 dBm Δf = ± 50 kHz Δf = ± 100 kHz	dBc dBc		-59 -71	

Note:

1. π/4 QPSK modulated wave input, data rate 42 kbps, Filter roll off α = 0.5

ABSOLUTE MAXIMUM RATINGS¹ ($T_A = 25^\circ\text{C}$)

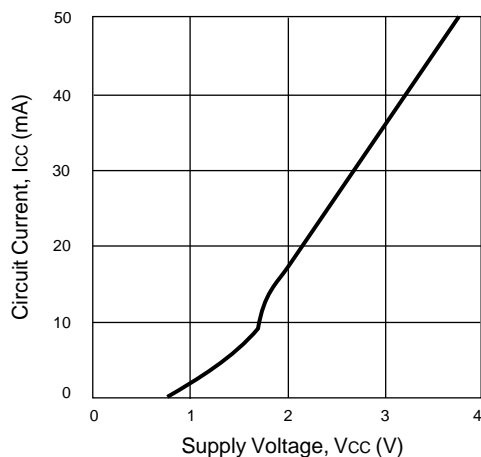
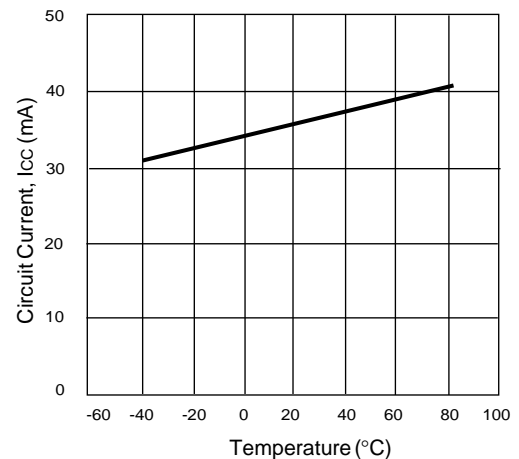
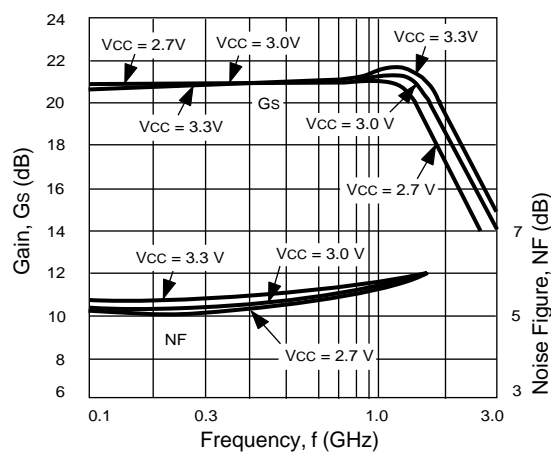
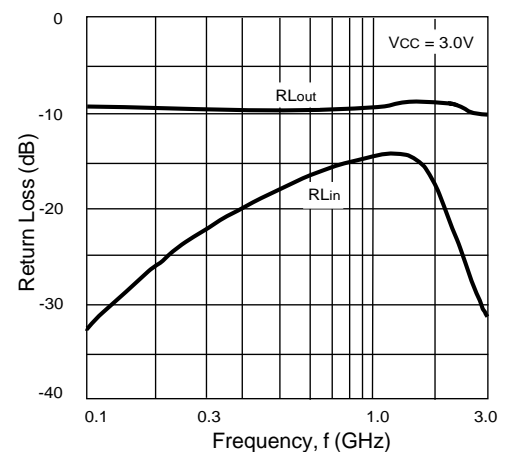
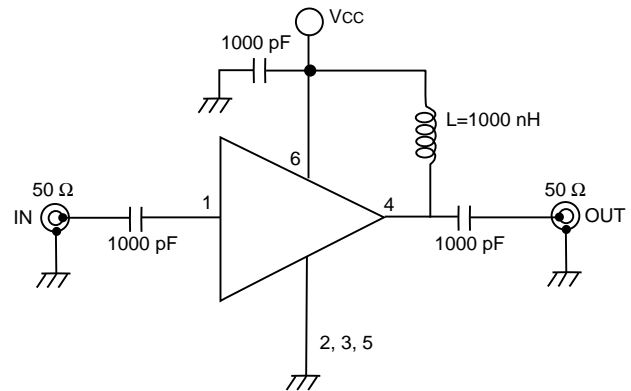
SYMBOLS	PARAMETERS	UNITS	RATINGS
V _{CC}	Supply Voltage	V	3.6
I _{CC}	Total Supply Current	mA	77.7
P _{IN}	Input Power	dBm	+13
P _T	Total Power Dissipation ²	mW	270
T _{OP}	Operating Temperature	°C	-40 to +85
T _{STG}	Storage Temperature	°C	-55 to +150

Notes:

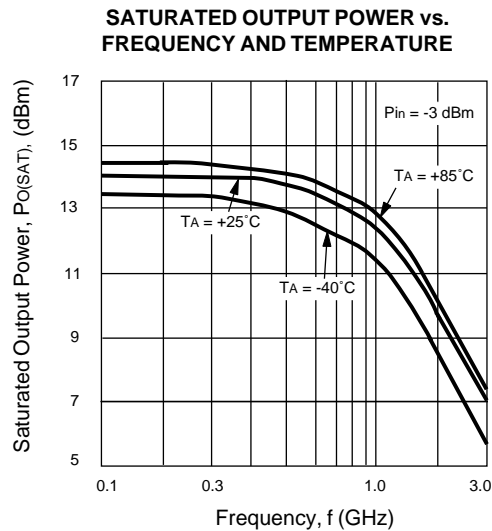
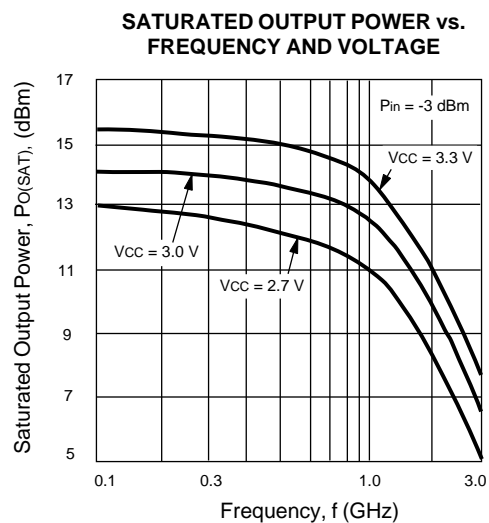
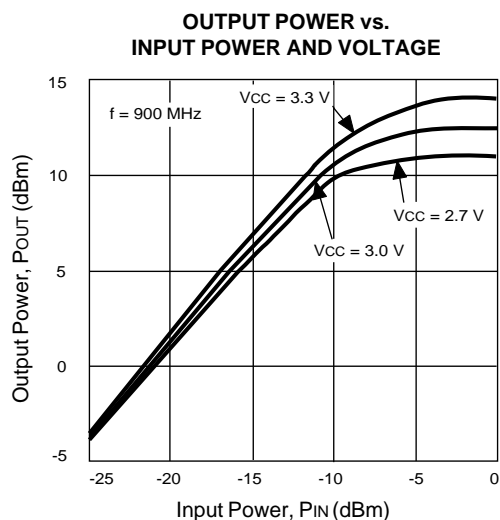
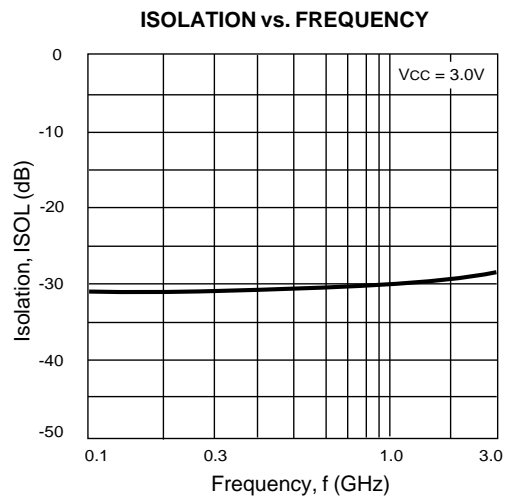
- Operation in excess of any one of these parameters may result in permanent damage.
- Mounted on a 50 X 50 X 1.6 mm epoxy glass PWB ($T_A = 85^\circ\text{C}$).

**RECOMMENDED
OPERATING CONDITIONS**

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
V _{CC}	Supply Voltage	V	2.7	3	3.3
T _{OP}	Operating Temperature	°C	-40	+25	+85

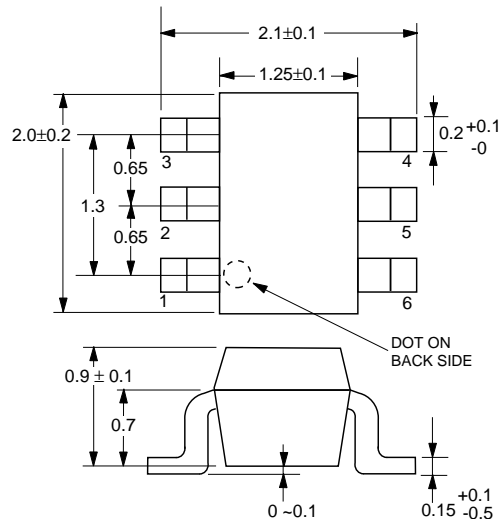
TYPICAL PERFORMANCE CURVES ($T_A = 25^\circ\text{C}$)**CIRCUIT CURRENT vs. VOLTAGE****CIRCUIT CURRENT vs. TEMPERATURE****GAIN AND NOISE FIGURE
vs. FREQUENCY AND VOLTAGE****INPUT RETURN LOSS AND
OUTPUT RETURN LOSS vs. FREQUENCY****TEST CIRCUIT**

TYPICAL PERFORMANCE CURVES (T_A = 25°C)

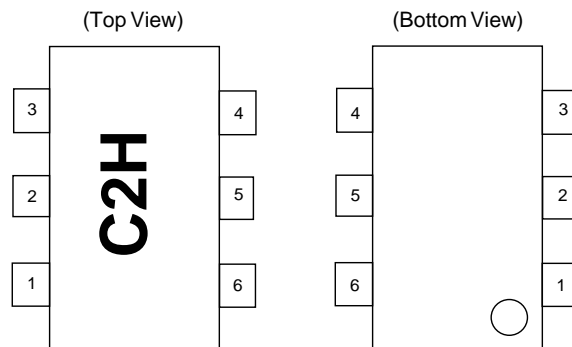


OUTLINE DIMENSIONS (Units in mm)

UPC2771TB
PACKAGE OUTLINE S06



LEAD CONNECTIONS



1. INPUT
2. GND
3. GND
4. OUTPUT
5. GND
6. Vcc

PIN DESCRIPTION

Pin No.	Pin Name (V)	Applied Voltage	Description	Internal Equivalent Circuit
1	Input	—	Signal input pin. An internal matching circuit, configured with resistors, enables 50 Ω connection over a wide bandwidth. A multi-feedback circuit is designed to cancel the deviations of h_{FE} and resistance. This pin must be coupled to the signal source with a blocking capacitor.	
4	Output	2.7 to 3.3	Signal output pin. Connect an inductor between this pin and VCC to supply current to the internal output transistors.	
6	VCC		Power supply pin. This pin should be externally equipped with a bypass capacitor to minimize ground impedance.	
2	GND	0	Ground pins. These pins should be connected to system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. All the ground pins must be connected together with wide ground pattern to minimize impedance difference.	

ORDERING INFORMATION

PART NUMBER	QTY
UPC2771TB-E3-A	3K/Reel

Note: Embossed Tape, 8 mm wide. Pins 1, 2 and 3 face perforated side of tape.

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