TPS6505xEVM-195

This user's guide describes the characteristics, operation, and use of the TPS65050EVM-195, TPS65051EVM-195, TPS65052EVM-195, TPS65054EVM-195 and TPS65056EVM-195 evaluation module (EVM). This EVM demonstrates the Texas Instruments TPS6505x power management IC (PMIC). This document includes setup instructions, a schematic diagram, a bill of materials (BOM), and PCB layout drawings for the evaluation module.

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1 Introduction

The Texas Instruments TPS6505xEVM-195 evaluation module (EVM) helps designers evaluate the operation and performance of the TPS65050, TPS65051, TPS65052, TPS65054 and TPS65056 PMICs for applications that are powered with one Li ion or Li polymer cell and require multiple power rails. The TPS6505x contains two highly efficient step-down switching converters, four low dropout linear regulators (LDO), and additional status I/O pins.

1.1 Related Documentation From Texas Instruments

TPS6505x data sheet (SLVS710)

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS6505xEVM-195.

2.1 Input/Output Connector Descriptions

2.1.1 J1 —VIN

This is the positive input voltage connection to the converter. The EVM operates from any supply voltage between 2.5 V and 6 V. The leads to the input supply should be twisted and kept as short as possible to minimize EMI transmission and input voltage droop.

2.1.2 J2—GND

This is the input return connection for the input power supply.

2.1.3 J3—VDCDC1

This is the positive output for VDCDC1 step-down converter. This output is externally adjustable for the TPS65050, TPS65051, and TPS65054. The output for the TPS65052 and TPS65056 is fixed. The EVM preset output voltages are found in Table 1. VDCDC1 is capable of sourcing up to 600 mA for the TPS65050 and TPS65054 and up to 1 A for the TPS65051, TPS65052 and TPS65056.

2.1.4 J4—GND

This is the return connection for the VDCDC1 output rail.

2.1.5 J5 —VDCDC2

This is the positive output for VDCDC2 step-down converter. This output is externally adjustable for the TPS65050 and TPS65051. The output for the TPS65052, TPS65054 and TPS65056 is programmed by the DEFDCDC2 input to two factory-programmed voltages. The EVM preset output voltages are found in Table 1. VDCDC2 is capable of sourcing up to 600 mA for all versions.

2.1.6 J6—GND

This is the return connection for the VDCDC2 output rail.

2.1.7 J7—VLDO1

This is the positive output for the VLDO1 LDO linear regulator. This output is input programmable for the TPS65050 and TPS65052 and externally adjustable for the TPS65051, TPS65054 and TPS65056. The VLDO1 output is capable of supplying up to 400 mA. The EVM preset output voltages are found in Table 1.

2.1.8 J8—GND

This is the return connection for the VLDO1 output rail.

2.1.9 J9—VLDO2

This is the positive output for the VLDO2 LDO linear regulator. This output is input programmable for the TPS65050 and TPS65052 and externally adjustable for the TPS65051, TPS65054 and TPS65056. The VLDO2 output is capable of supplying up to 400 mA. The EVM preset output voltages are found in Table 1.

2.1.10 J10—GND

This is the return connection for the VLDO2 output rail.

2.1.11 J11—VLDO3

This is the positive output for the VLDO3 LDO linear regulator. This output is input programmable for the TPS65050 and TPS65052 and externally adjustable for the TPS65051, TPS65054 and TPS65056. The VLDO3 output is capable of supplying up to 200 mA. The EVM preset output voltages are found in Table 1.

2.1.12 J12 —GND

This is the return connection for the VLDO3 output rail.

2.1.13 J13 —VLDO4

This is the positive output for the VLDO4 LDO linear regulator. This output is input programmable for the TPS65050 and TPS65052 and externally adjustable for the TPS65051, TPS65054 and TPS65056. The VLDO4 output is capable of supplying up to 200 mA. The EVM preset output voltages are found in Table 1.

2.1.14 J14—GND

This is the return connection for the VLDO4 output rail.

2.1.15 J15 —PB_OUT or $\overline{\text{RESET}}$

Pin 1 of this output allows the user to measure the PB_OUT (TPS65050) or $\overline{\text{RESET}}$ (TPS65051/ TPS65052/ TPS65054/ TPS65056) output. The PB_OUT output is toggled using the SW1 pushbutton switch. The $\overline{\text{RESET}}$ output goes high 100 ms after the THRESHOLD input exceeds 1 V. $\overline{\text{RESET}}$ goes low when the HYSTERESIS input falls below 1 V. On the EVM, the $\overline{\text{RESET}}$ circuitry monitors the input voltage. The rising threshold is set to a 3.4-V input and the falling threshold is set to 3.3 V.

2.1.16 JP1 —EN VDCDC1

JP1 is used to enable the VDCDC1 output. Place a shorting bar in the ON position to turn on the VDCDC1 step-down converter. Place a shorting bar in the OFF position to turn off the VDCDC1 converter.

2.1.17 JP2 —MODE

JP2 is used to select between the forced PWM and Power Save mode operation for the switching converters. Place a shorting bar in the PSM position to select the Power Save mode. In this mode, PFM is used for light loads, and PWM is used for heavier loads. Place a shorting bar in the PWM position to force PWM operation at all loads.

2.1.18 JP3 —DEFLDO1

JP3–JP6 are used to program the LDO regulation voltages for the TPS65050 and TPS65052. Place a shorting bar in the HI position to connect DEFLDO1 to the input voltage. Place a shorting bar in the LO position to connect DEFLDO1 to GND. This jumper is not installed on the TPS65051, TPS65054 and TPS65056 EVMs.

2.1.19 JP4—DEFLDO2

JP3 - JP6 are used to program the LDO regulation voltages for the TPS65050 and TPS65052. Place a shorting bar in the HI position to connect DEFLDO2 to the input voltage. Place a shorting bar in the LO position to connect DEFLDO2 to GND. This jumper is not installed on the TPS65051, TPS65054 and TPS65056 EVMs.

2.1.20 JP5—DEFLDO3

JP3–JP6 are used to program the LDO regulation voltages for the TPS65050 and TPS65052. Place a shorting bar in the HI position to connect DEFLDO3 to the input voltage. Place a shorting bar in the LO position to connect DEFLDO3 to GND. This jumper is not installed on the TPS65051, TPS65054 and TPS65056 EVMs.

2.1.21 JP6—DEFLDO4

JP3–JP6 are used to program the LDO regulation voltages for the TPS65050 and TPS65052. Place a shorting bar in the HI position to connect DEFLDO4 to the input voltage. Place a shorting bar in the LO position to connect DEFLDO4 to GND. This jumper is not installed on the TPS65051, TPS65054 and TPS65056 EVMs.

2.1.22 JP7—EN VDCDC2

JP7 is used to enable the VDCDC2 output. Place a shorting bar in the ON position to turn on the VDCDC2 step-down converter. Place a shorting bar in the OFF position to turn off the VDCDC2 converter.

2.1.23 JP8 —DEFDCDC2

JP8 is used to select the VDCDC2 output voltage for the TPS65052 and TPS65054. Place a shorting bar in the HI position to regulate the VDCDC2 output to 1.3 V (TPS65052/TPS65056) or 1.05 V (TPS65054). Place a shorting bar in the LO position to regulate the VDCDC2 output to 1 V (TPS65052/TPS65056) or 1.3 V (TPS65054).

2.1.24 JP9 —EN LDO1

JP9 is used to enable the VLDO1 output. Remove the shorting bar to turn off the VLDO1 LDO converter. Place a shorting bar in the ON position to turn on the VLDO1 LDO converter. For the TPS65050, place the shunt in the PB position to connect EN_LDO1 to the PB_OUT output. This allows the user to control the enable using the installed pushbutton switch (SW1). The PB position should not be used for the TPS65051/ TPS65052/ TPS65054/ TPS65056 EVMs.

2.1.25 JP10 —EN LDO2

JP10 is used to enable the VLDO2 output. Remove the shorting bar to turn off the VLDO2 LDO converter. Place a shorting bar in the ON position to turn on the VLDO2 LDO converter. For the TPS65050, place the shunt in the PB position to connect EN_LDO2 to the PB_OUT output. This allows the user to control the enable using the installed pushbutton switch (SW1). The PB position should not be used for the TPS65051/ TPS65052/ TPS65054/ TPS65056 EVMs.

2.1.26 JP11—EN LDO3

JP11 is used to enable the VLDO3 output. Remove the shorting bar to turn off the VLDO3 LDO converter. Place a shorting bar in the ON position to turn on the VLDO3 LDO converter. For the TPS65050, place the shunt in the PB position to connect EN_LDO3 to the PB_OUT output. This allows the user to control the enable using the installed pushbutton switch (SW1). The PB position should not be used for the TPS65051/ TPS65052/ TPS65054/ TPS65056 EVMs.

2.1.27 JP12—EN LDO4

JP12 is used to enable the VLDO4 output. Remove the shorting bar to turn off the VLDO4 LDO converter. Place a shorting bar in the ON position to turn on the VLDO4 LDO converter. For the TPS65050, place the shunt in the PB position to connect EN_LDO4 to the PB_OUT output. This allows the user to control the enable using the installed pushbutton switch (SW1). The PB position should not be used for the TPS65051/ TPS65052/ TPS65054/ TPS65056 EVMs.

2.2 Setup

2.2.1 EVM Family Configuration

The EVM is configured to provide the following nominal operating conditions:

Input voltage: 2.5 V to 6 V

Output voltage: See Table 1

Maximum load current: See Table 2

Table 1. EVM Preset Output Voltage

Output	TPS65050EVM	TPS65051EVM	TPS65052EVM	TPS65054EVM	TPS65056EVM
VDCDC1	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
VDCDC2	1.6 V	1.6 V	1 V	1.3 V	1 V
VLDO1	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
VLDO2	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
VLDO3	1.85 V	1.2 V	1.85 V	1.85 V	1.85 V
VLDO4	1.85 V	1.2 V	1.85 V	1.85 V	1.3 V

Table 2. Maximum Load Current

Output	TPS65050EVM	TPS65051EVM	TPS65052EVM	TPS65054EVM	TPS65056EVM
VDCDC1	600 mA	1 A	1 A	600 mA	1 A
VDCDC2	600 mA	600 mA	600 mA	600 mA	600 mA
VLDO1	400 mA	400 mA	400 mA	400 mA	400 mA
VLDO2	400 mA	400 mA	400 mA	400 mA	400 mA
VLDO3	200 mA	200 mA	200 mA	200 mA	200 mA
VLDO4	200 mA	200 mA	200 mA	200 mA	200 mA

2.2.2 Operation

1. Configure all EVM jumpers to factory settings shown in Table 3.
2. Connect the input voltage return to J2.
3. Connect the positive input voltage to J1.
4. Connect all loads to the outputs.
5. Turn on input voltage.

Table 3. Factory EVM Jumper Settings

Jumper	Shunt Location				
	TPS65050EVM	**TPS65051EVM**	**TPS65052EVM**	**TPS65054EVM**	**TPS65056EVM**
JP1	Between ON and ENDCDC1	Between ON and ENDCDC1	Between ON and ENDCDC1	Between ON and ENDCDC1	Between ON and ENDCDC1
JP2	Between PWM and MODE	Between PWM and MODE	Between PWM and MODE	Between PWM and MODE	Between PWM and MODE
JP3	Between LOW and DEFLDO1	Not Installed	Between LOW and DEFLDO1	Not Installed	Not Installed
JP4	Between LOW and DEFLDO2	Not Installed	Between LOW and DEFLDO2	Not Installed	Not Installed
JP5	Between LOW and DEFLDO3	Not Installed	Between LOW and DEFLDO3	Not Installed	Not Installed
JP6	Between LOW and DEFLDO4	Not Installed	Between LOW and DEFLDO4	Not Installed	Not Installed
JP7	Between OFF and ENDCDC2	Between OFF and ENDCDC2	Between OFF and ENDCDC2	Between OFF and ENDCDC2	Between OFF and ENDCDC2
JP8	Not Installed	Not Installed	Between LOW and DEFDCDC2	Between LOW and DEFDCDC2	Between LOW and DEFDCDC2
JP9	Between ON and ENLDO1	Between ON and ENLDO1	Between ON and ENLDO1	Between ON and ENLDO1	Between ON and ENLDO1
JP10	Between ON and ENLDO2	Between ON and ENLDO2	Between ON and ENLDO2	Between ON and ENLDO1	Between ON and ENLDO1
JP11	Between ON and ENLDO3	Between ON and ENLDO3	Between ON and ENLDO3	Between ON and ENLDO1	Between ON and ENLDO1
JP12	Between ON and ENLDO4	Between ON and ENLDO4	Between ON and ENLDO4	Between ON and ENLDO1	Between ON and ENLDO1

3 Board Layout

This section provides the TPS6505xEVM-195 board layout and illustrations.

3.1 Layout

Figure 1 through Figure 5 show the board layout for the TPS6505xEVM-195 PCB.

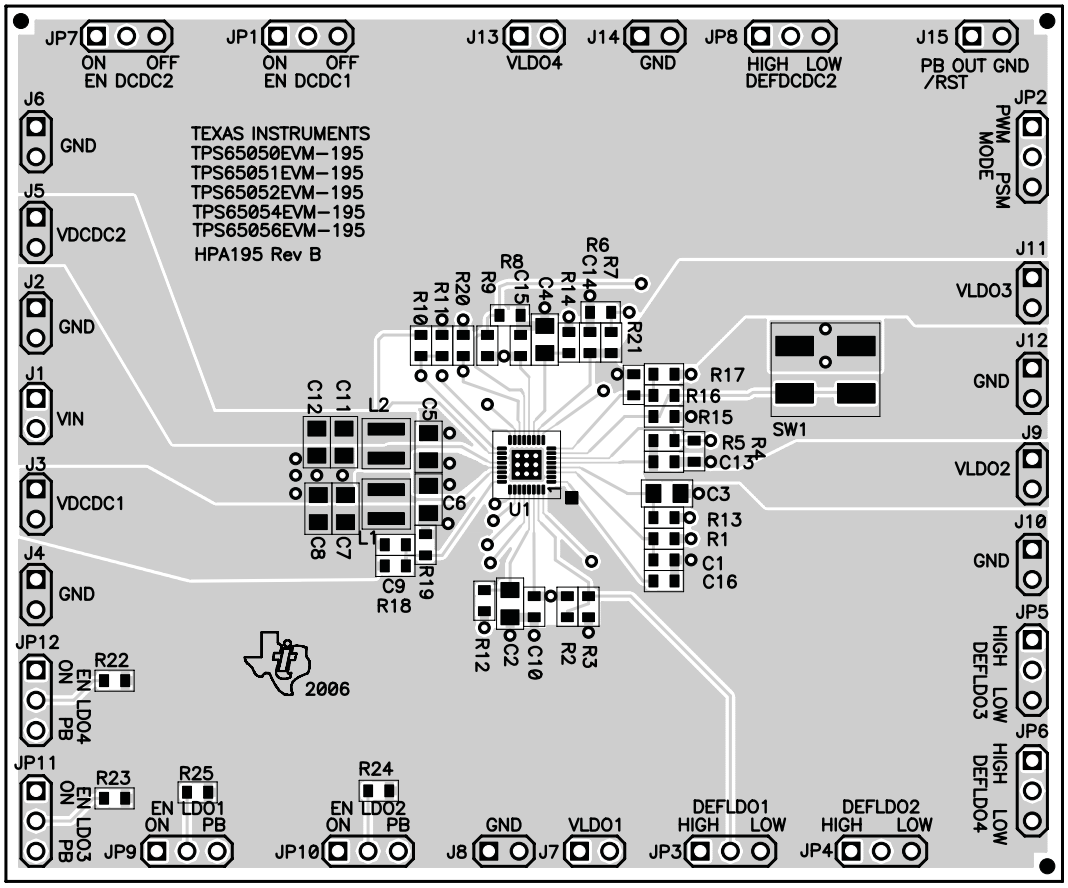

Figure 1. Assembly Layer

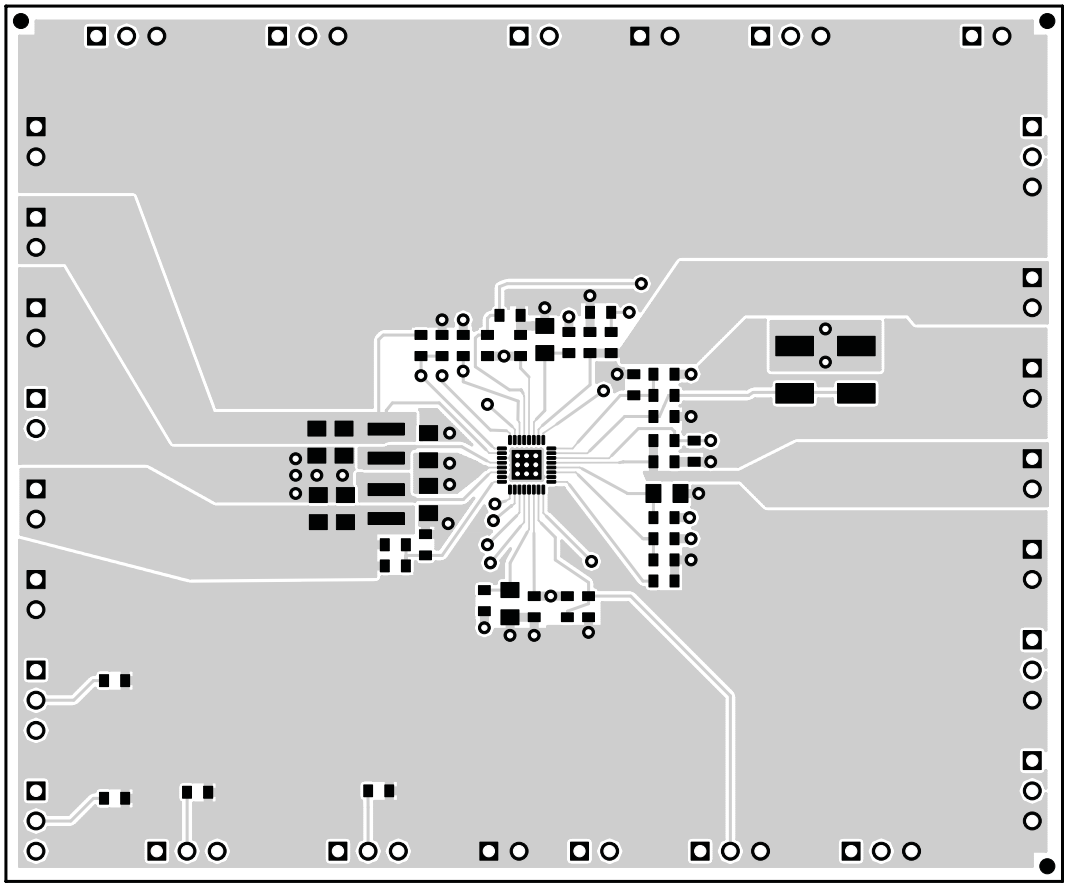

Figure 2. Top Layer Routing

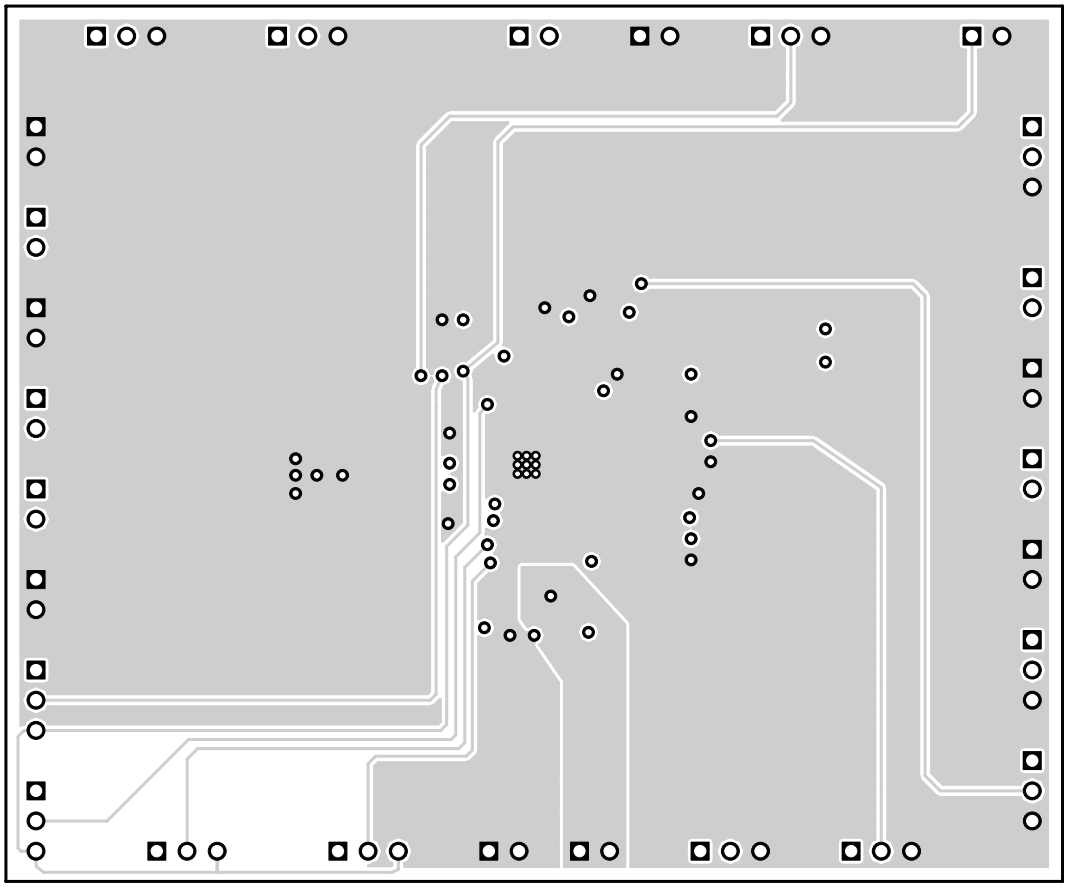

Figure 3. Inner Layer 2 Routing

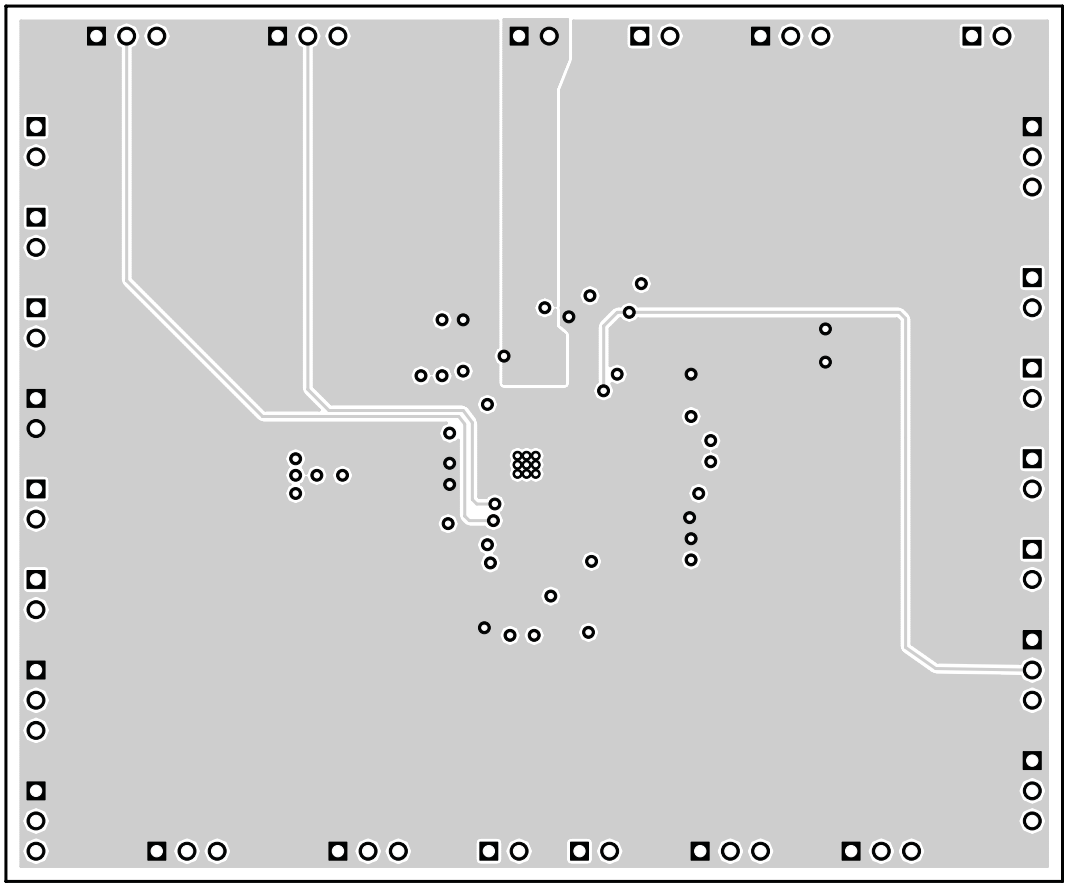

Figure 4. Inner Layer 3 Top Layer Routing

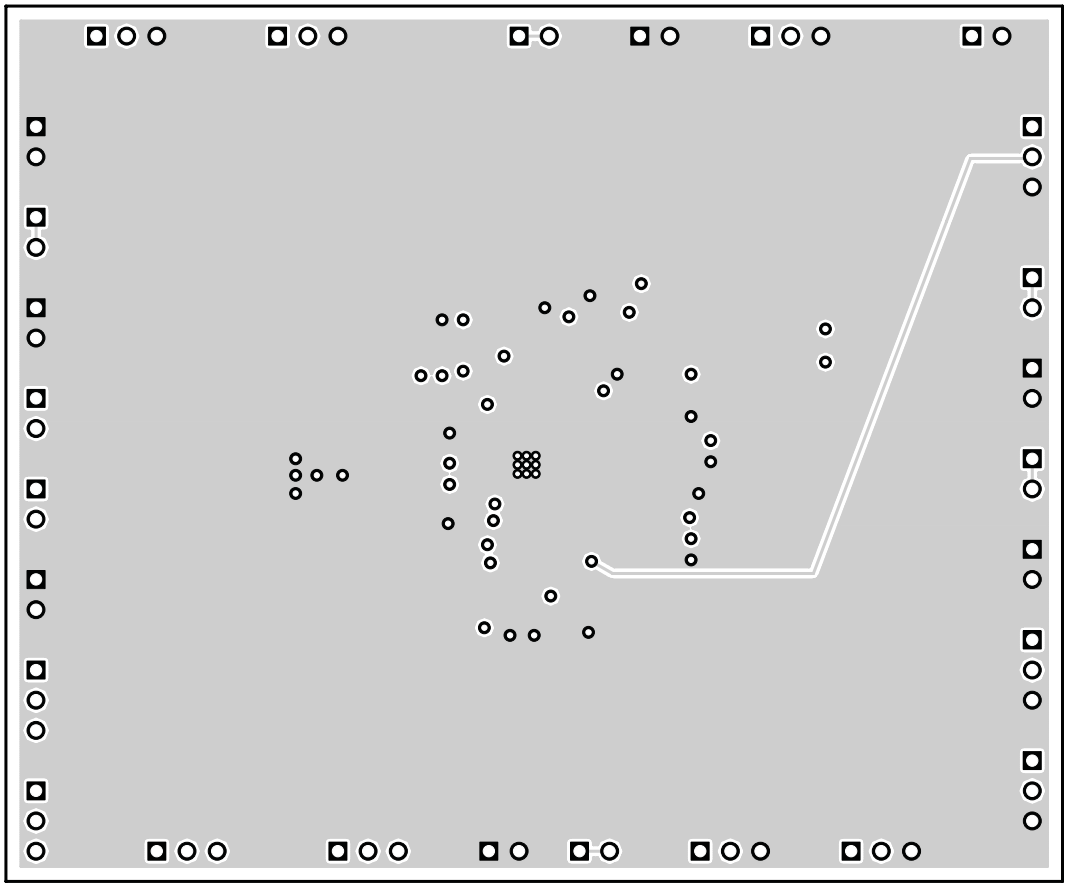

Figure 5. Bottom Layer Routing

4 Schematic and Bill of Materials

This section provides the TPS6505xEVM-195 schematic and bill of materials.

4.1 Schematic

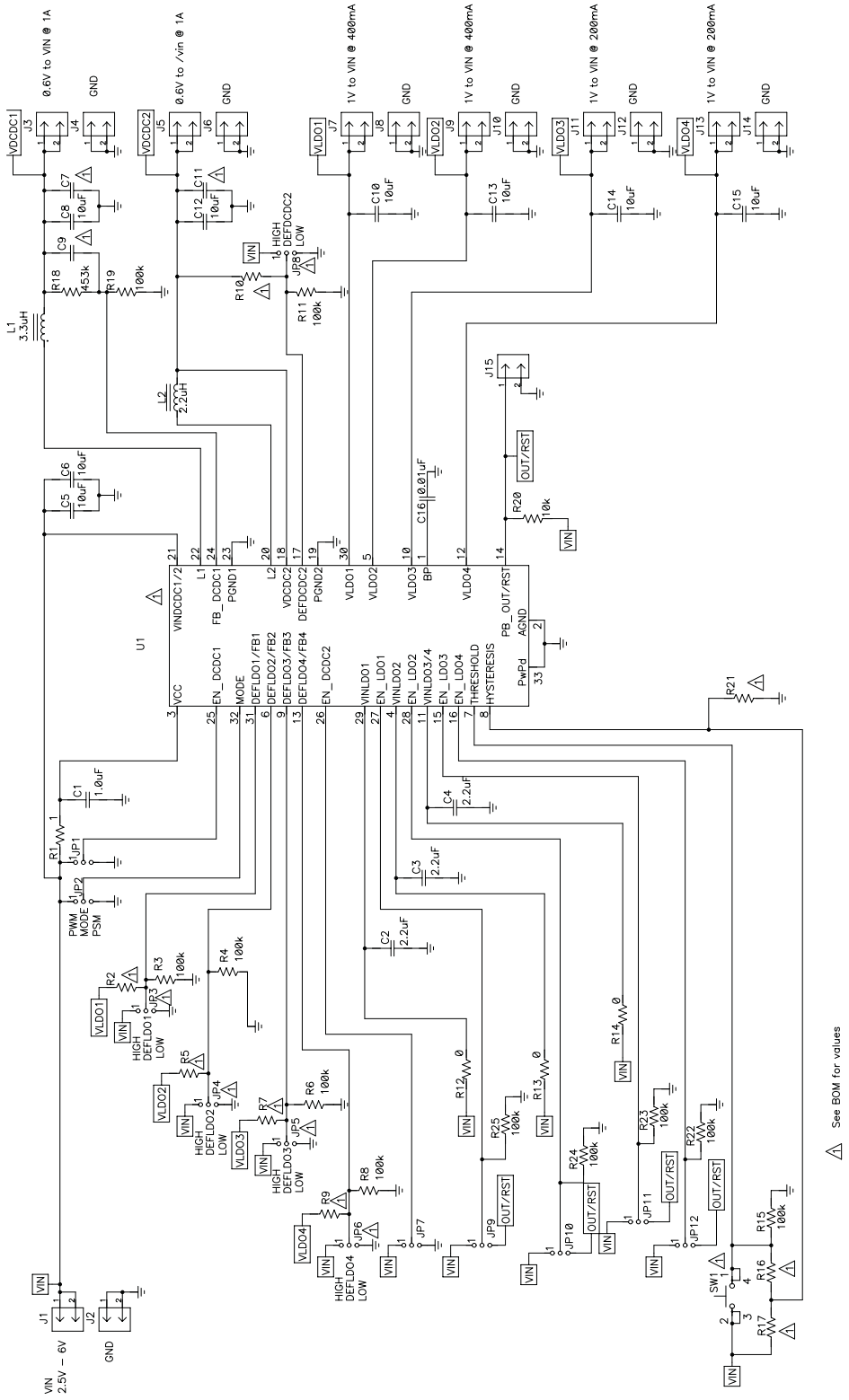

Figure 6. TPS6505xEVM-195 Schematic

4.2 Bill of Materials

Table 4. TPS6505xEVM-195 Bill of Materials

COUNT					RefDes	Value	Description	Size	Part Number	MFR
-001	-002	-003	-004	-005						
1	1	1	1	1	C1	1.0 µF	Capacitor, Ceramic, 25V, X5R, 10%	0603	GRM188R61E105KA12D	Murata
0	0	0	1	1	C10	4.7 µF	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	GRM188R60J475KE19D	Murata
1	1	1	0	0		10 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	GRM188R60J106ME47D	Murata
0	0	0	1	1	C13	4.7 µF	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	GRM188R60J475KE19D	Murata
1	1	1	0	0		10 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	GRM188R60J106ME47D	Murata
1	1	1	0	0	C14	10 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	GRM188R60J106ME47D	Murata
0	0	0	1	1		2.2 µF	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	GRM188R60J225KE01D	Murata
0	0	0	1	1	C15	2.2 µF	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	GRM188R60J225KE01D	Murata
1	1	1	0	0		10 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	GRM188R60J106ME47D	Murata
1	1	1	1	1	C16	0.01 µF	Capacitor, Ceramic, 50V, X7R, 10%	0603	C1608X7R1H103K	TDK
3	3	3	3	3	C2–C3	2.2 µF	Capacitor, Ceramic, 10V, X5R, 10%	0805	GRM216R61A225KE24D	Murata
4	4	4	4	4	C5, C6, C8, C12	10 µF	Capacitor, Ceramic, 10V, X5R, 10%	0805	GRM21BR61A106KE19L	Murata
0	0	0	0	0	C7, C11	Open	Capacitor, Ceramic, vvV	0805		
1	1	0	1	1	C9	47pF	Capacitor, Ceramic, 50V, COG, 5%	0603	C1608C0G1H470J	TDK
15	15	15	15	15	J1–J15		Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 × 2	PTC36SAAN	Sullins
7	7	7	7	7	JP1, JP2, JP7, JP9–JP12		Header, 3 pin, 100mil spacing, (36-pin strip)	0.100 × 3	PTC36SAAN	Sullins
4	0	4	4	4	JP3–JP6		Header, 3 pin, 100mil spacing, (36-pin strip)	0.100 × 3	PTC36SAAN	Sullins
0	0	1	0	0	JP8		Header, 3 pin, 100mil spacing, (36-pin strip)	0.100 × 3	PTC36SAAN	Sullins
1	1	1	1	1	L1	3.3 µH	Inductor, SMT, 1.3A, 130mΩ	0.118 × 0.118	LPS3015-332MLC	Coilcraft
1	1	1	1	1	L2	2.2 µH	Inductor, SMT, 1.4A, 220mΩ	0.118 × 0.118	LPS3010-222MLC	Coilcraft
1	1	1	0	0	R1	1	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	0	0	1	1		100	Resistor, Chip, 1/16W, 1%	0603	Std	Std
3	3	3	3	3	R12–R14	0	Resistor, Chip, 1/16W, 5%	0603	Std	Std
0	2	0	2	2	R2, R5	232k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	1	0	0	0	R7	20k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	0	0	1	1		30k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	1	0	0	0	R9	20k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	0	0	1	1		30k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	0	0	0	R10	169k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	1	1	0	0	R16	3.01k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	0	0	1	1		3.32k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	1	1	1	1	R17	237k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	0	0	0	R18	453k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	0	1	0	1		0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	0	0	1	0		200k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	0	1	0	R19	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	1	1	1	R20	10k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	0	0	0	0	R21	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
11	11	11	11	11	R3, R4, R6, R8, R11, R15, R22–R25	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	0	0	0	0	SW1		Switch, SPST, PB momentary, sealed washable	0.245 × 0.251	KT11P2JM	C & K

Table 4. TPS6505xEVM-195 Bill of Materials (continued)

COUNT					RefDes	Value	Description	Size	Part Number	MFR
-001	-002	-003	-004	-005						
1	0	0	0	0	U1		IC, Dual step-down converter with 4 fixed LDOs	QFN-32	TPS65050RSM	TI
0	1	0	0	0			IC, Dual step-down converter with 4 adjustable LDOs	QFN-32	TPS65051RSM	TI
0	0	1	0	0			IC, Dual fixed step-down converter with 4 fixed LDOs	QFN-32	TPS65052RSM	TI
0	0	0	1	0			IC, Dual step-down converter with 4 fixed LDOs	QFN-32	TPS65054RSM	TI
0	0	0	0	1			IC, Dual step-down converter with 4 fixed LDOs	QFN-32	TPS65056RSM	TI
1	1	1	1	1	—		PCB, 3.5 In × 2.9 In × 0.062 In		HPA195	Any
11	7	12	11	11	—		Shunt, 100 mil, Black	0.100	929950-00	3M

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.5 V to 6 V and the output voltage range of 1 V to VIN.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 100°C. The EVM is designed to operate properly with certain components above 100°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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