5-V Dual TTL-to-Differential PECL Translator

FEATURES

- **1.1-ns (max) Propagation Delay**
- **Operating Range: V_{CC} = 4.2V to 5.7V with GND = 0 V**
- **< 50-ps (typ) Output-to-Output Skew**
- **Built-In Temperature Compensation**
- **Drop-In Compatible to the MC10ELT22, MC100ELT22**

APPLICATIONS

- **Data and Clock Transmission Over Backplane**
- **Signaling Level Conversion for Clock or Data**

DESCRIPTION

The SN65ELT22 is a dual TTL-to-differential PECL translator. It operates on +5-V supply and ground only. The output is undetermined when the inputs are left floating. The low output skew makes the device an ideal solution for clock or data signal translation.

The SN65ELT22 is housed in an industry standard SOIC-8 package and is also available in an optional TSSOP-8 package.

PIN ASSIGNMENT

D or DGK PACKAGE
(TOP VIEW)

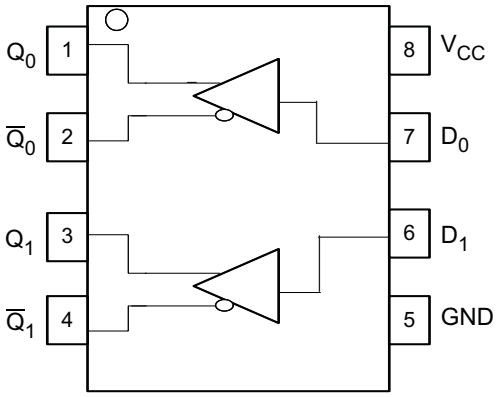


Table 1. Pin Descriptions

PIN	FUNCTION
D_0, D_1	TTL inputs
Q_0, $\overline{Q}_0$, Q_1, $\overline{Q}_1$	PECL outputs
V_{CC}	Positive supply
GND	Ground

ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE	LEAD FINISH
SN65ELT22D	SN65ELT22	SOIC	NiPdAu
SN65ELT22DGK	SN65ELT22	SOIC-TSSOP	NiPdAu

(1) Leaded device options are not initially available; contact a sales representative for further details

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

PARAMETER	CONDITIONS	VALUE	UNIT
Absolute PECL mode supply voltage, V_{CC}	GND = 0 V	6	V
Input voltage, V_{IN}	GND = 0 V	GND + 0.025 < V_{IN} < V_{CC} – 0.025	V
Output current	Continuous	50	mA
	Surge	100	
Operating temperature range		–40 to 85	°C
Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	POWER RATING T_A < 25°C (mW)	THERMAL RESISTANCE, JUNCTION-TO-AMBIENT NO AIRFLOW	DERATING FACTOR T_A > 25°C (mW/°C)	POWER RATING T_A = 85°C (mW)
SOIC	Low-K	719	139	7	288
	High-K	840	119	8	336
SOIC-TSSOP	Low-K	469	213	5	188
	High-K	527	189	5	211

THERMAL CHARACTERISTICS

PARAMETER			MIN	TYP	MAX	UNIT
θ_{JB}	Junction-to-board thermal resistance	SOIC		79		°C/W
		SOIC-TSSOP		120		
θ_{JC}	Junction-to-case thermal resistance	SOIC		98		°C/W
		SOIC-TSSOP		74		

KEY ATTRIBUTES

CHARACTERISTICS		VALUE
Moisture sensitivity level		Level 1
Flammability rating (oxygen index: 28 to 34)		UL 94 V-0 at 0.125 in
Electrostatic discharge	Human body model	4 kV
	Charge device model	2 kV
	Machine model	200 V
Meets or exceeds JEDEC Spec EIA/JESD78 latchup test		

PECL DC CHARACTERISTICS

At V_{CC} = 5.0 V, GND = 0.0 V (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	T_A = –40°C			T_A = 25°C			T_A = 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Power supply current			17.3	20		18.2	20		19.4	22	mA
V_{OH}	High-level output voltage	See (3)	3915	3954	4120	3915	3958	4120	3915	3961	4120	mV
V_{OL}	Low-level output voltage	See (3)	3170	3236	3380	3170	3231	3380	3170	3229	3380	mV

(1) The device meets the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) Input and output parameters vary 1:1 with V_{CC}. V_{CC} can vary +0.7 V /–0.8 V.
(3) Outputs are terminated through a 50-Ω resistor to V_{CC} – 2.0 V.

TTL DC CHARACTERISTICS

At V_{CC} = 4.2 V to 5.7 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	V_{IN} = 2.7 V, V_{IN} = (V_{CC} – 0.025) V			20	µA
I_{IHH}	High-level input current	V_{IN} = V_{CC}			20	µA
I_{IL}	Low-level input current	V_{IN} = 0.5 V, V_{IN} = (GND + 0.025) V			–200	µA
V_{IK}	Input clamp diode voltage	I_{IN} = –18 mA			–1.2	V
V_{IH}	High-level input voltage		2.0		Vcc– 0.025	V
V_{IL}	Low-level input voltage		GND + 0.025		0.8	V

(1) The device meets the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously

AC CHARACTERISTICS

At V_{CC} = 4.2 V to 5.7 V, GND = 0.0 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	T_A = –40°C			T_A = 25°C			T_A = 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Max switching frequency(2), see Figure 5			500			490			470		MHz
t_{PLH}	Propagation delay time	1.5 V to 50%	0.6	0.83	1.1	0.6	0.84	1.1	0.6	0.85	1.1	ns
t_{PHL}			0.5		0.9	0.5		0.9	0.5		0.9	
t_{SKEW}	Within device skew	See(3)		25	90		25	90		25	90	ps
	Device-to-device skew	See (4)		25	100		25	100		25	100	
t_{JITTER}	Random clock jitter (RMS)				0.5			0.5			0.5	ps
t_r/t_f	Output rise/fall times	Q (20%–80%)	0.7		1.1	0.7		1.1	0.7		1.1	ns

(1) The device meets the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) Maximum switching frequency measured at output amplitude of 300 mV_{pp}.
(3) Measured between outputs under the identical transitions and conditions on any one device.
(4) Device-to-device skew for identical transitions at identical V_{CC} levels.

Typical Termination for Output Driver

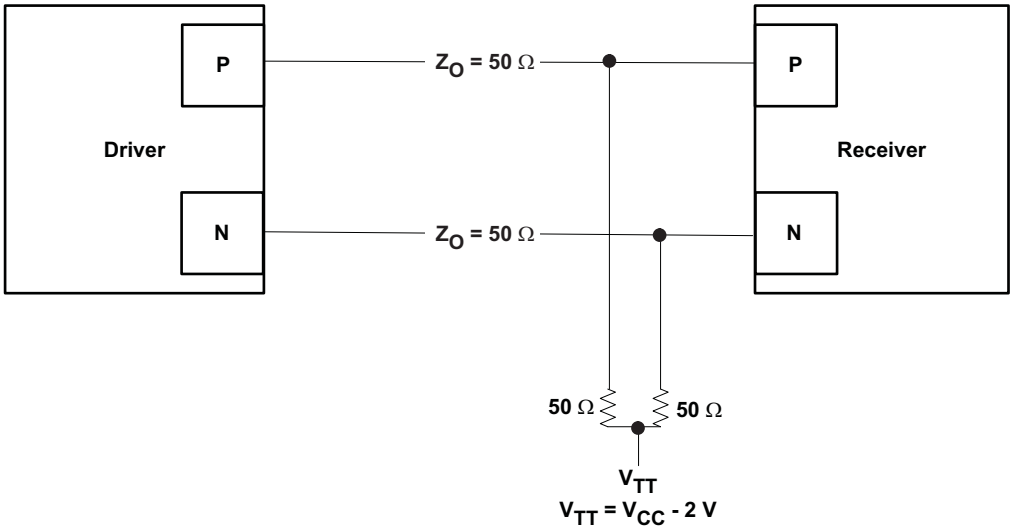


Figure 1. Typical Termination for Driver

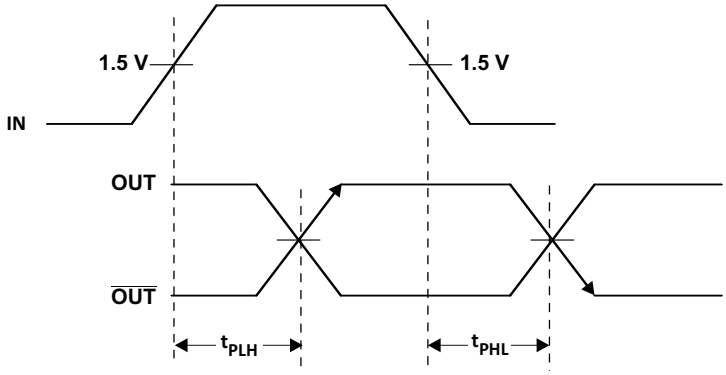


Figure 2. Output Propagation Delay

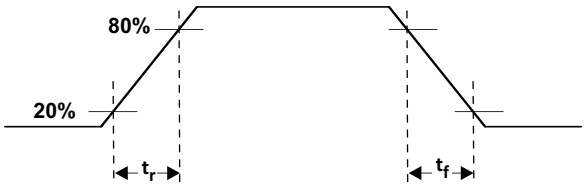


Figure 3. Output Rise and Fall Times

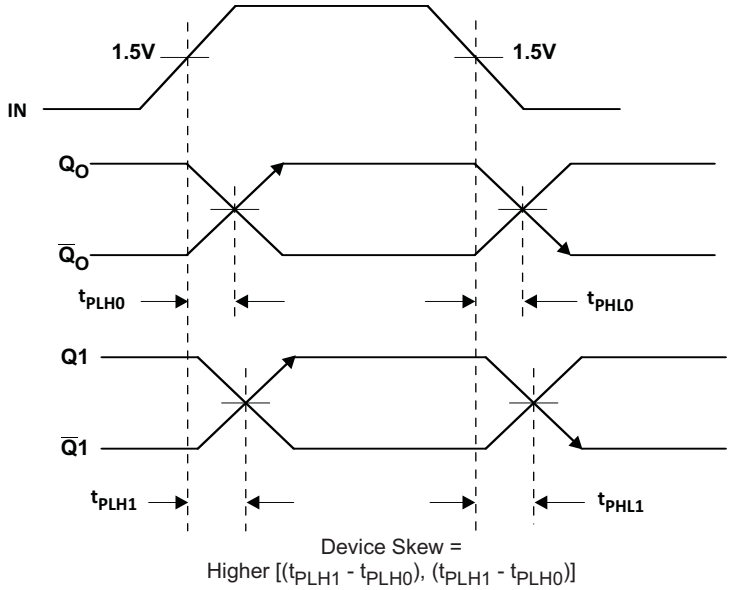


Figure 4. Device Skew

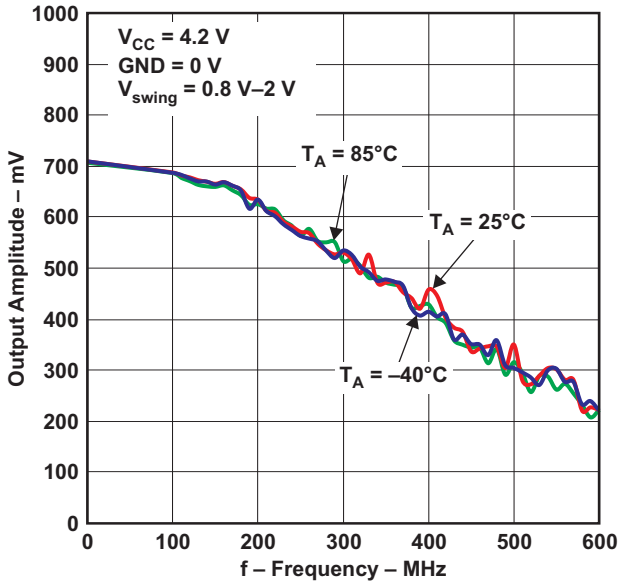


Figure 5. Output Amplitude vs. Frequency

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65ELT22D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ELT22
SN65ELT22D.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ELT22
SN65ELT22DGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIPI
SN65ELT22DGK.B	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIPI
SN65ELT22DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIPI
SN65ELT22DGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIPI
SN65ELT22DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ELT22
SN65ELT22DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ELT22

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

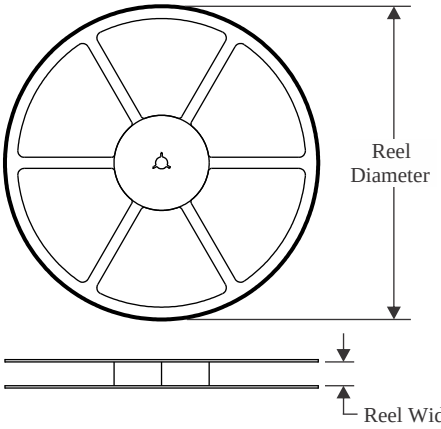
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

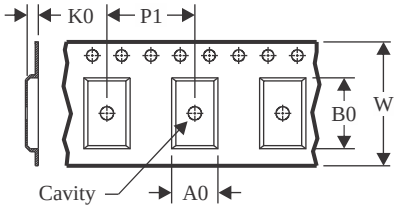
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

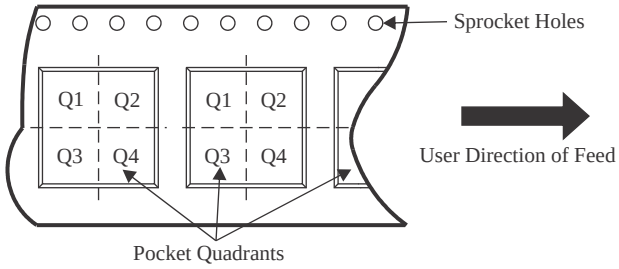


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

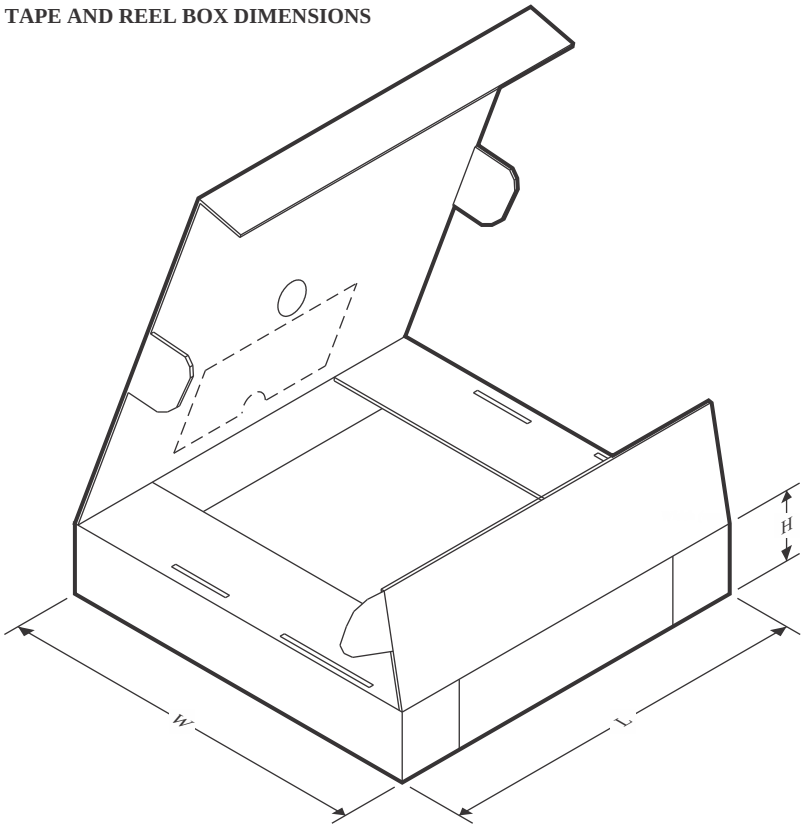
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65ELT22DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65ELT22DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

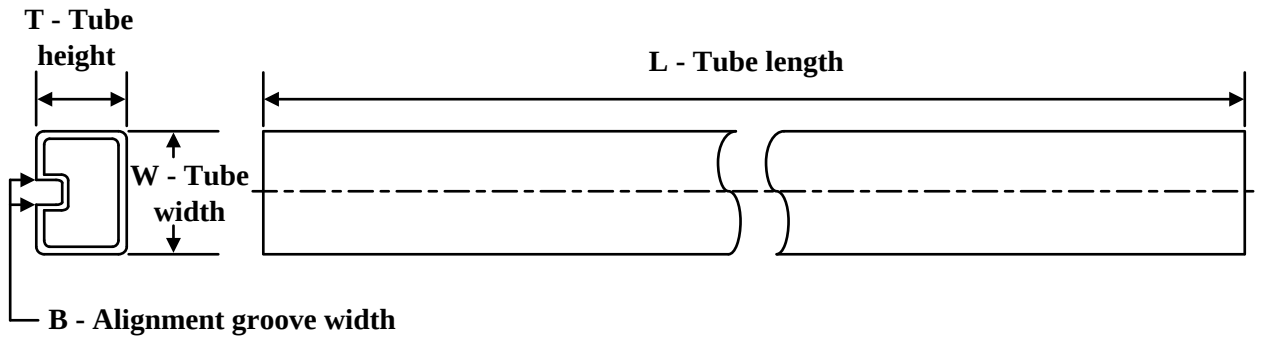
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65ELT22DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
SN65ELT22DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

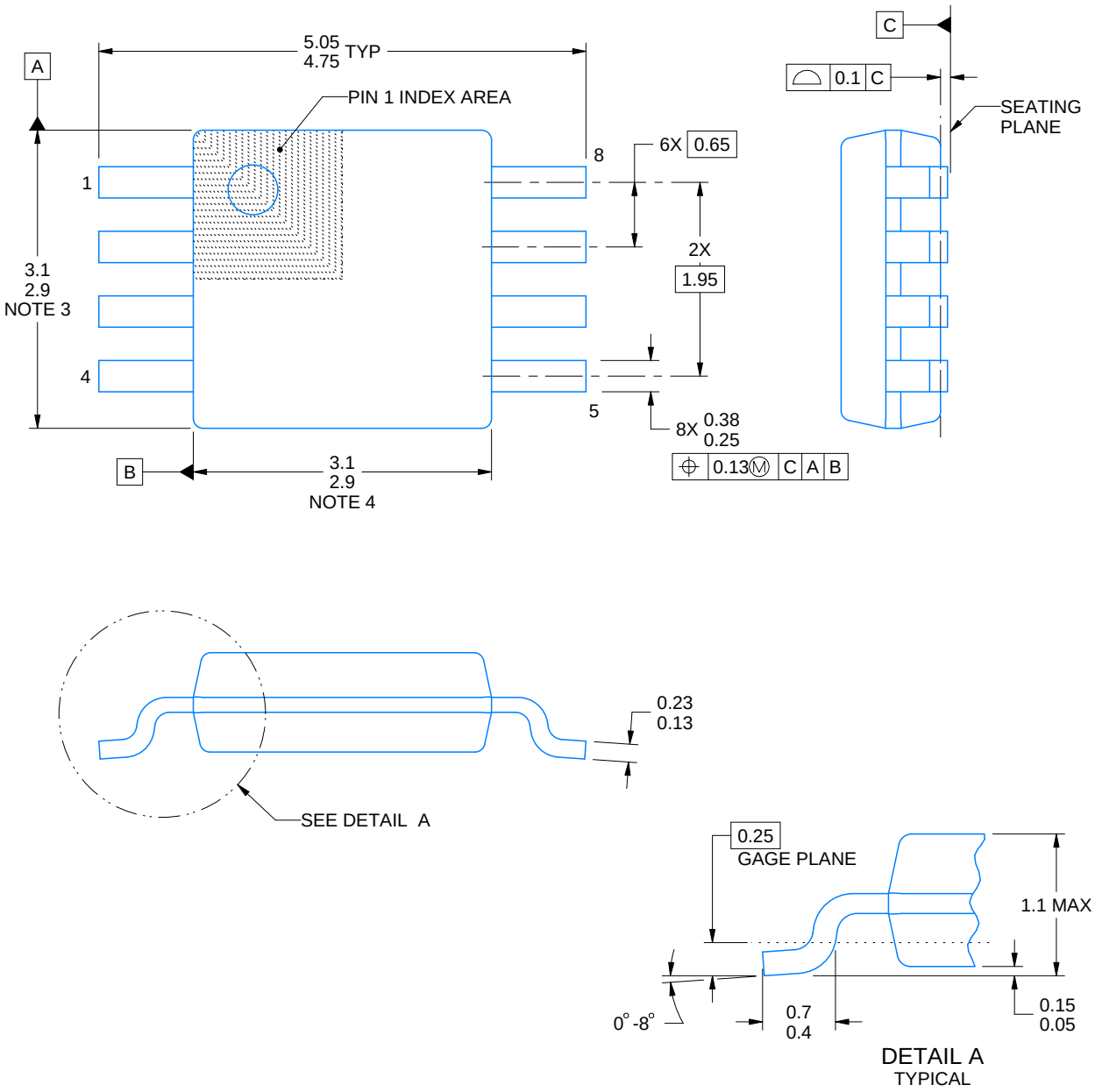
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65ELT22D	D	SOIC	8	75	506.6	8	3940	4.32
SN65ELT22D.B	D	SOIC	8	75	506.6	8	3940	4.32
SN65ELT22DGK	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
SN65ELT22DGK.B	DGK	VSSOP	8	80	330.2	6.6	3005	1.88

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

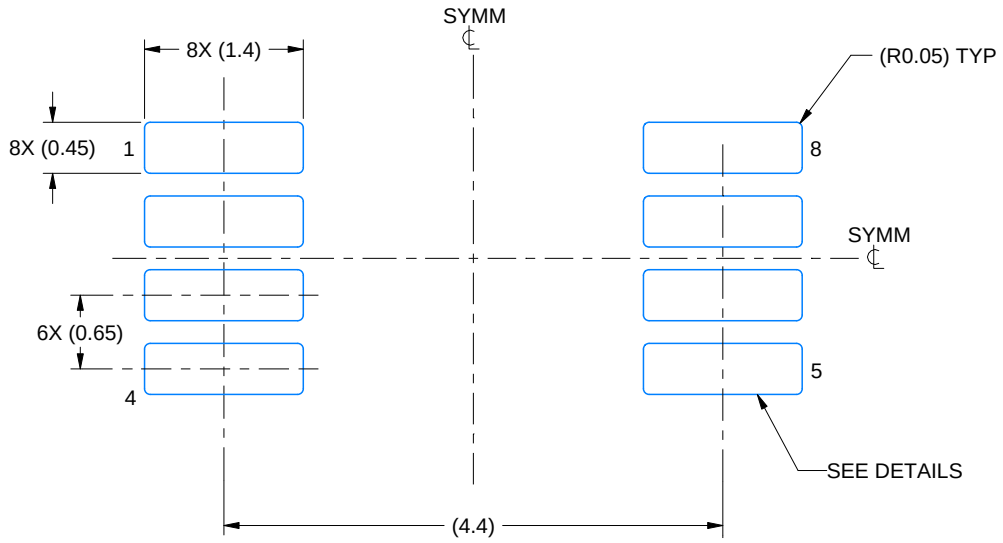
SMALL OUTLINE PACKAGE



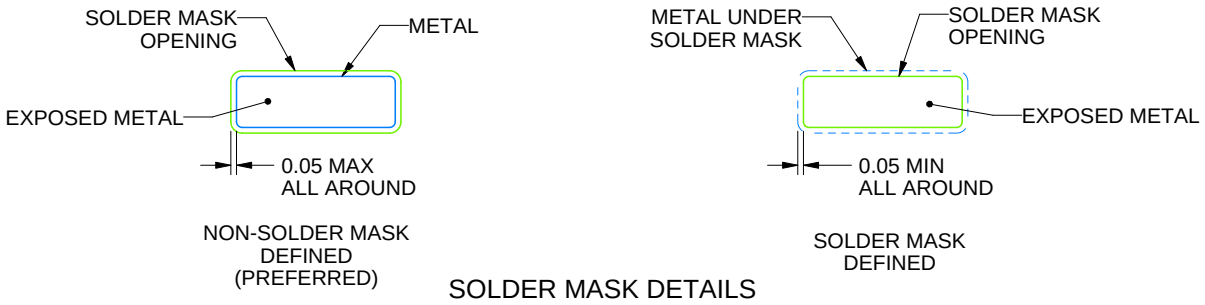
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

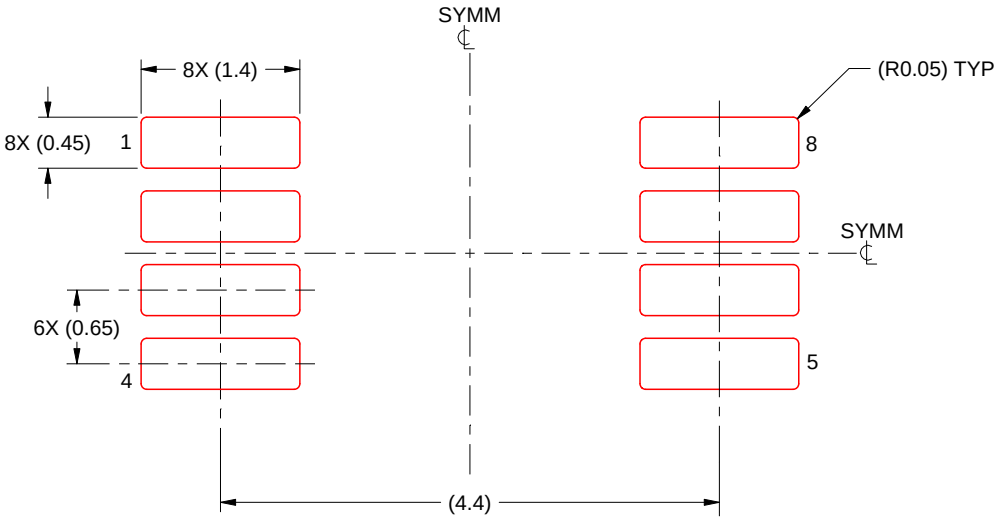


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

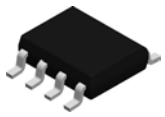


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

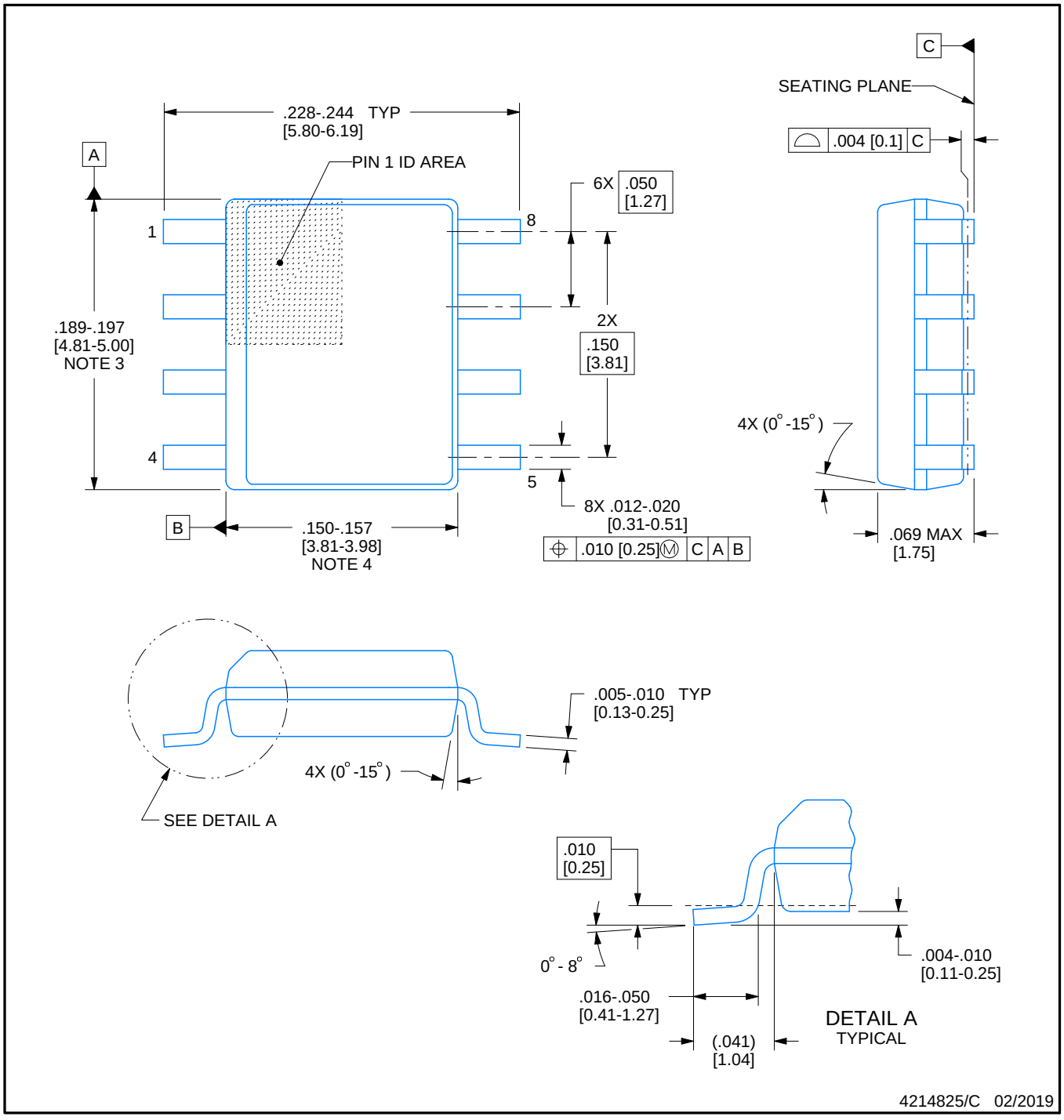


PACKAGE OUTLINE

D0008A

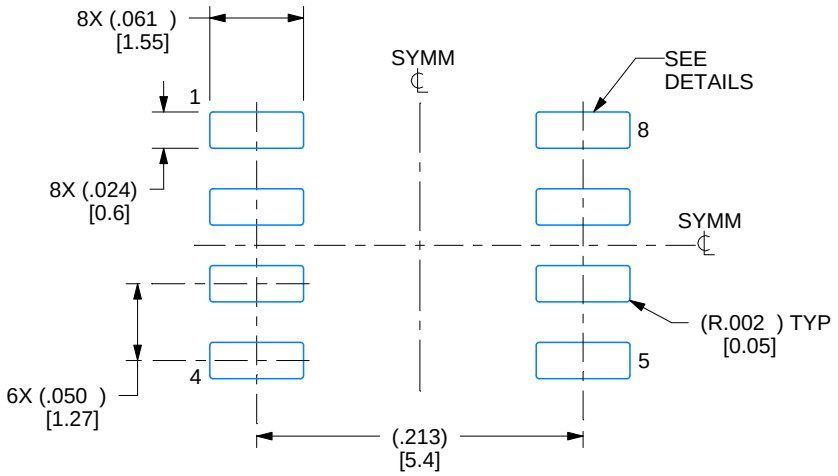
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

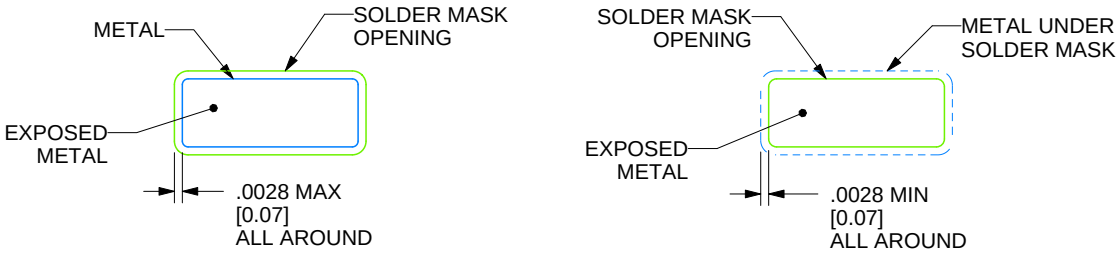


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

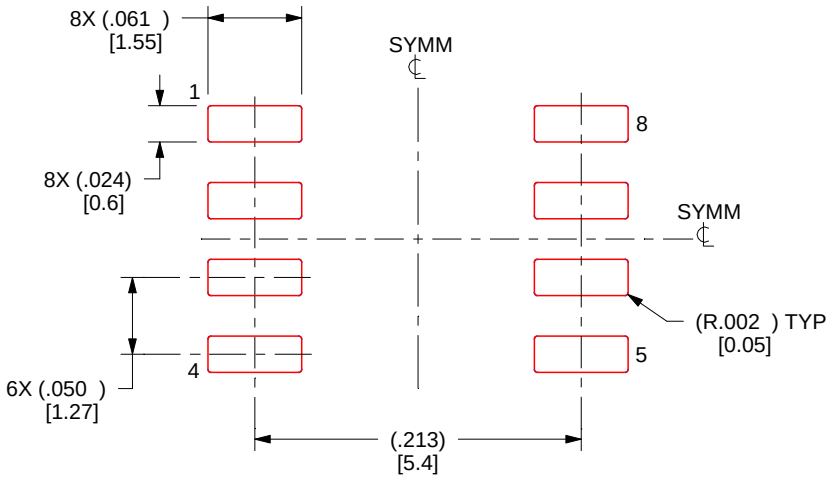
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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