

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- True Logic Outputs
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (N) 300-mil DIPs

description

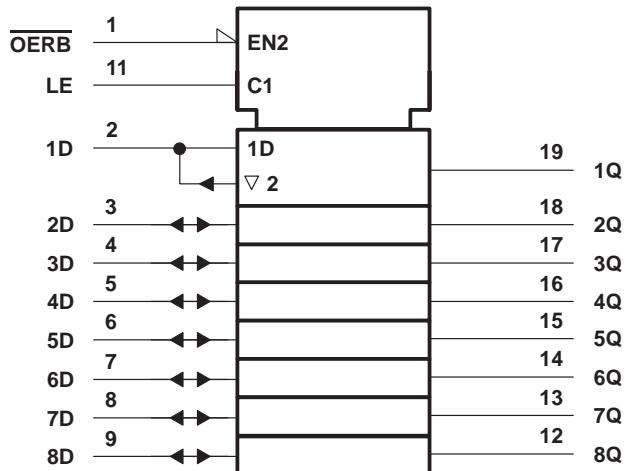
This 8-bit latch is designed specifically for storing the contents of the input data bus and providing the capability of reading back the stored data onto the input data bus.

The eight latches are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs.

Read back is provided through the output-enable (\overline{OERB}) input. When \overline{OERB} is taken low, the data present at the output of the data latches is allowed to pass back onto the input data bus. When \overline{OERB} is taken high, the output of the data latches is isolated from the D inputs. \overline{OERB} does not affect the internal operation of the latches; however, precautions should be taken not to create a bus conflict.

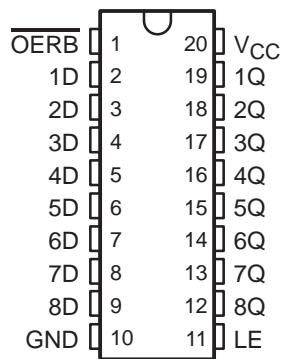
The SN74ALS990 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

DW OR N PACKAGE (TOP VIEW)

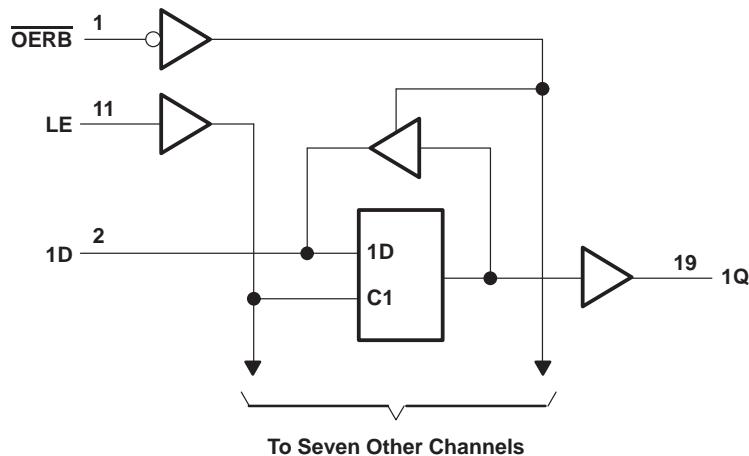


SN74ALS990

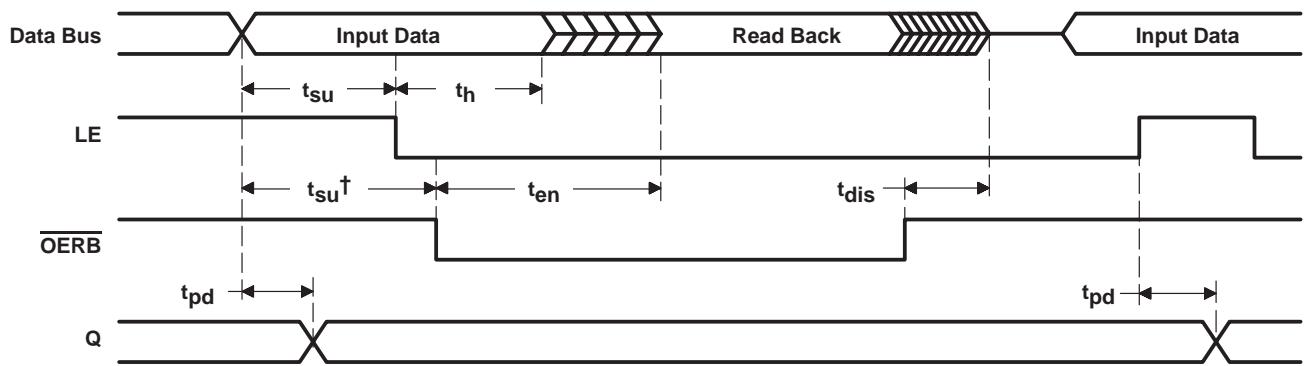
8-BIT D-TYPE TRANSPARENT READ-BACK LATCH

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logic diagram (positive logic)



timing diagram



† This setup time ensures that the read-back circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	7 V
Input voltage, V_I (OERB and LE)	7 V
Voltage applied to D inputs	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage		0.8		V
I_{OH}	High-level output current	Q		-2.6	mA
		D		-0.4	
I_{OL}	Low-level output current	Q		24	mA
		D		8	
t_W	Pulse duration, LE high		10		ns
t_{SU}	Setup time	Data before $LE \downarrow$	10		ns
		Data before $\overline{OERB} \downarrow$	10		
t_h	Hold time, data after $LE \downarrow$		5		ns
T_A	Operating free-air temperature	0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA				-1.2	V
V_{OH}	All outputs	$V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -0.4$ mA		$V_{CC} - 2$		V
	Q	$V_{CC} = 4.5$ V, $I_{OH} = -2.6$ mA	2.4	3.2		
V_{OL}	D	$V_{CC} = 4.5$ V	$I_{OL} = 4$ mA	0.25	0.4	V
			$I_{OL} = 8$ mA	0.35	0.5	
	Q	$V_{CC} = 4.5$ V	$I_{OL} = 12$ mA	0.25	0.4	
			$I_{OL} = 24$ mA	0.35	0.5	
I_I	OERB, LE	$V_{CC} = 5.5$ V	$V_I = 5.5$ V		0.1	mA
	D inputs		$V_I = 7$ V		0.1	
I_{IH}	OERB, LE	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20	μ A
	D inputs‡				20	
I_{IL}	OERB, LE	$V_{CC} = 5.5$ V, $V_I = 0.4$ V			-0.1	mA
	D inputs‡				-0.1	
I_O §	$V_{CC} = 5.5$ V, $V_O = 2.25$ V		-30	-112		mA
I_{CC}	$V_{CC} = 5.5$ V, OERB high	Outputs high		27	50	mA
		Outputs low		40	70	

† All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

‡ For I/O ports (Q_A thru Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

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switching characteristics (see Figure 1)

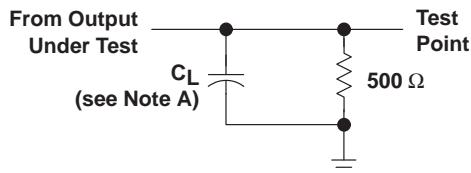
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V},$ $C_L = 50\text{ pF},$ $T_A = \text{MIN to MAX}^\dagger$		UNIT
			MIN	MAX	
t_{PLH}	D	Q	4	17	ns
t_{PHL}			5	24	
t_{PLH}	LE	Q	6	26	ns
t_{PHL}			8	26	
t_{en}^\ddagger	\overline{OERB}	D	4	21	ns
$t_{dis}^\$$	\overline{OERB}	D	4	19	ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

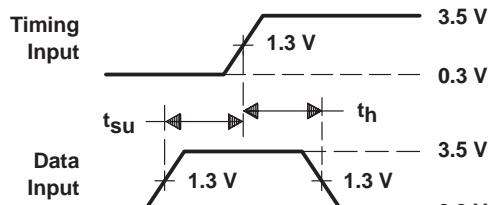
[‡] $t_{en} = t_{PZH}$ or t_{PZL}

[§] $t_{dis} = t_{PHZ}$ or t_{PLZ}

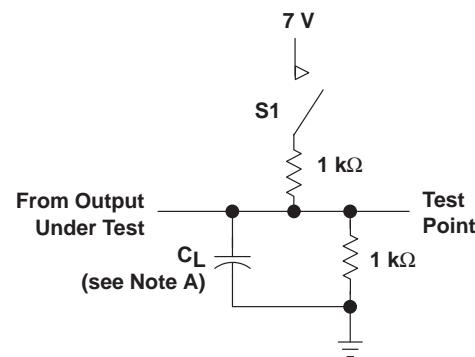
PARAMETER MEASUREMENT INFORMATION



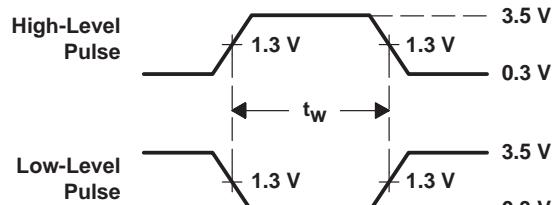
LOAD CIRCUIT FOR Q OUTPUTS



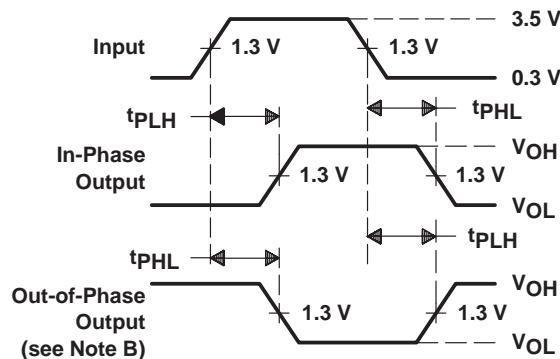
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



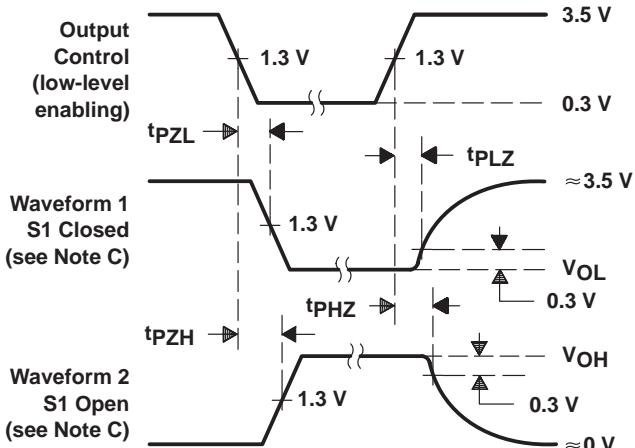
LOAD CIRCUIT FOR D OUTPUTS



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES:

- C_L includes probe and jig capacitance.
- When measuring propagation delay times of 3-state outputs, switch S1 is open.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALS990DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS990	Samples
SN74ALS990DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS990	Samples
SN74ALS990DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS990	Samples
SN74ALS990N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS990N	Samples
SN74ALS990N3	OBsolete	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74ALS990NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS990N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

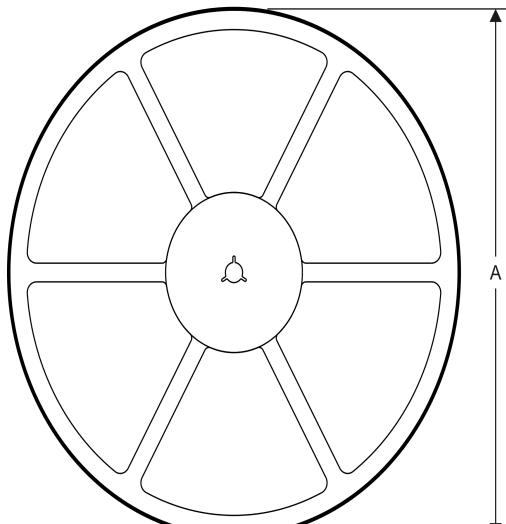
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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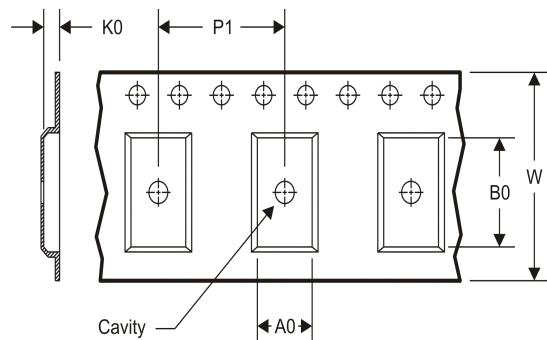
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TAPE AND REEL INFORMATION

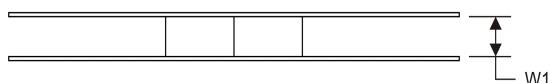
REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS990DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

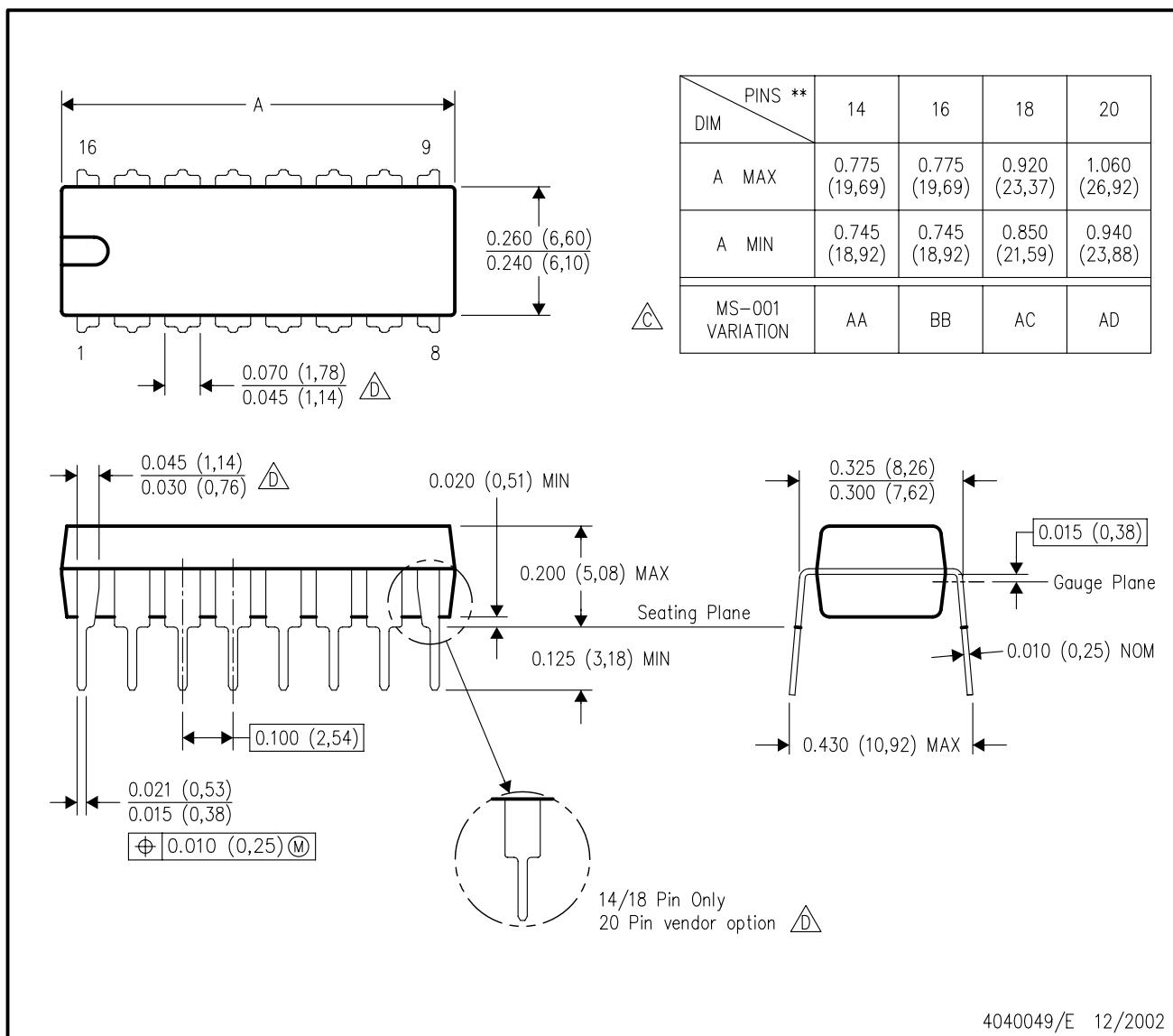
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS990DWR	SOIC	DW	20	2000	367.0	367.0	45.0

N (R-PDIP-T**)

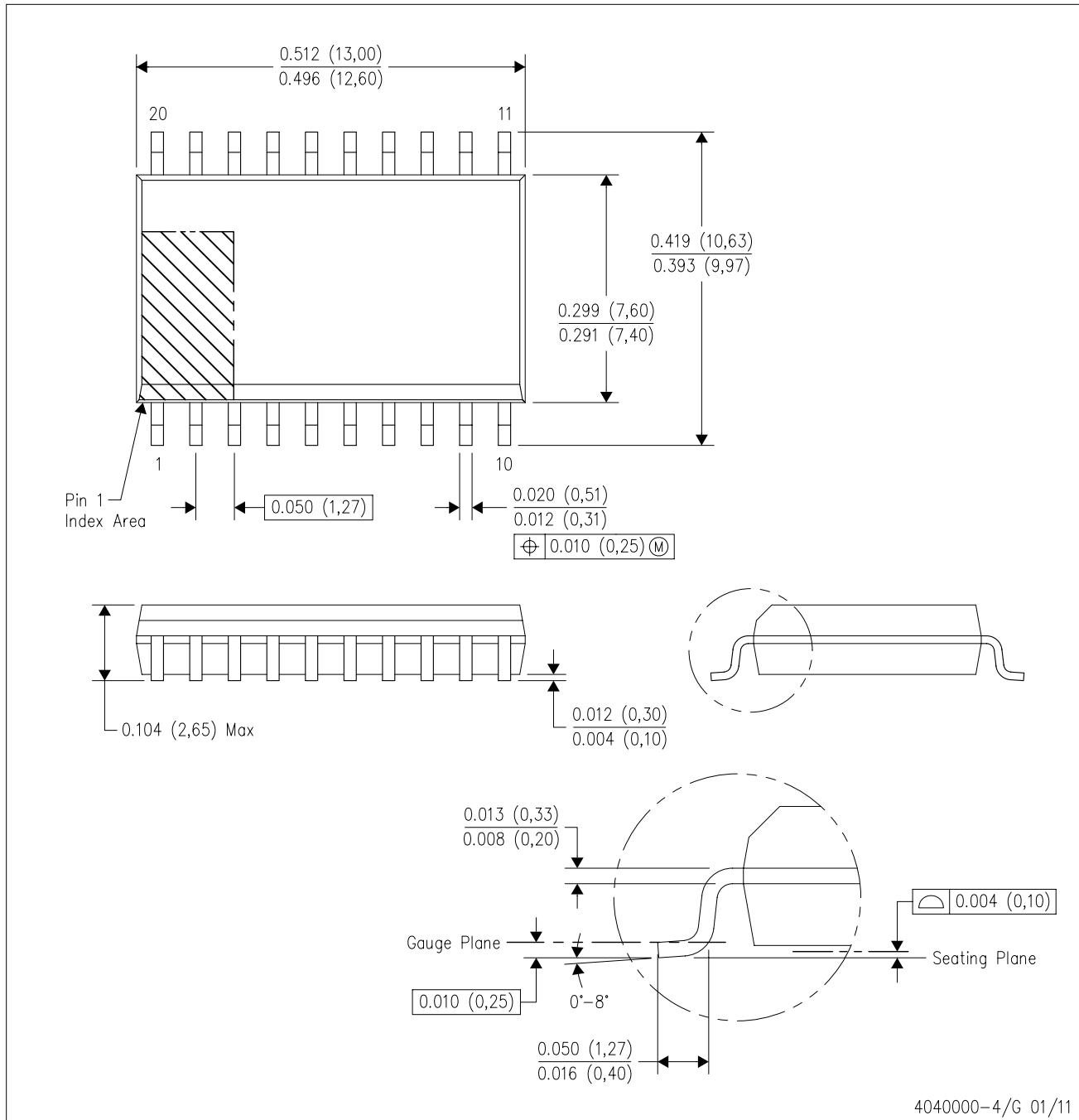
16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

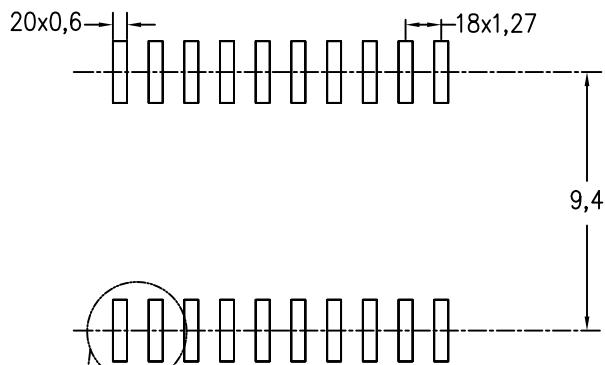
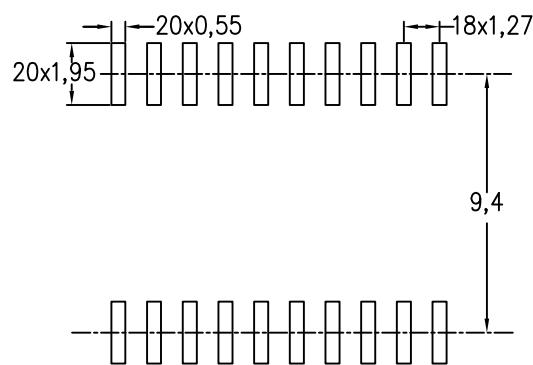


NOTES:

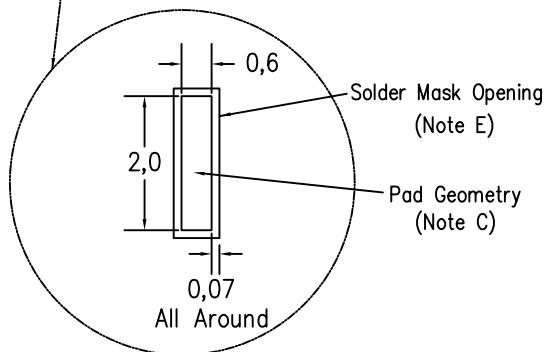
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)

Non Solder Mask Define Pad



4209202-4/F 08/13

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Refer to IPC7351 for alternate board design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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