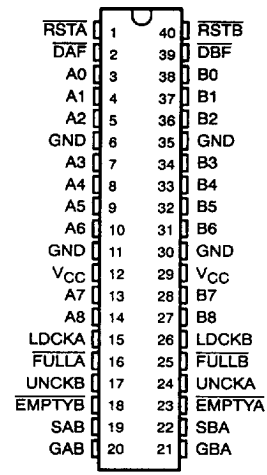
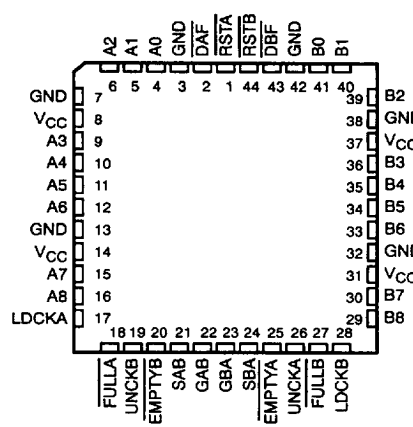
- **Independent Asychronous Inputs and Outputs**
- **Bidirectional**
- **32 Words by 9 Bits Each**
- **Programmable Depth**
- **Data Rates from 0 to 40 MHz**
- **Fall-Through Time . . . 22 ns Typ**
- **3-State Outputs**

**N PACKAGE**
**(TOP VIEW)**




**FN PACKAGE**
**(TOP VIEW)**




## description

This 576-bit memory uses Advanced Low-Power Schottky IMPACT-X™ technology and features high speed and fast fall-through times. It consists of two FIFOs organized as 32 words by 9 bits each.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

The 'ALS2238 consists of bus transceiver circuits, two 32 X 9 FIFOs, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal FIFO memories. Enable GAB and GBA are provided to control the transceiver functions. The SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low level selects real-time data and a high selects stored data. Eight fundamental bus-management functions can be performed as shown on the Operating Modes page.

Data on the A or B data bus, or both, is written into the FIFOs on a low-to-high transition at the load clock input (LDCKA or LDCKB) and is read out on a low-to-high transition at the unload clock input (UNCKA or UNCKB). The memory is full when the number of words clocked in exceeds, by the defined depth, the number of words clocked out.

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TEXAS INSTRUMENTS

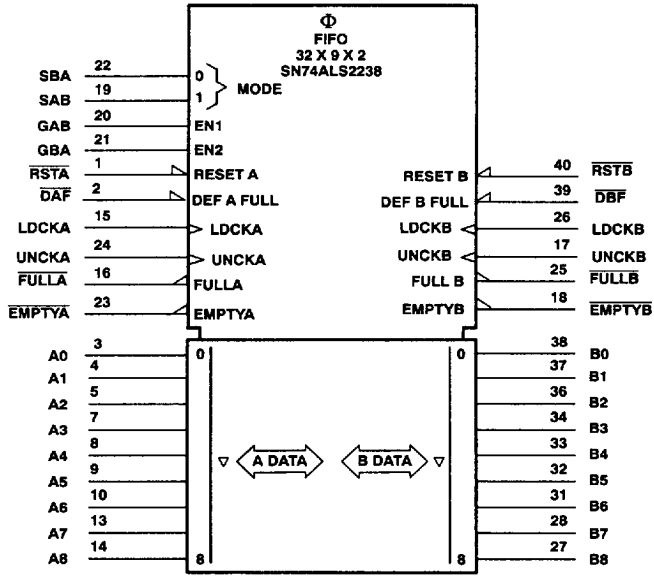
When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memories is monitored by the $\overline{\text{FULLA}}$, $\overline{\text{FULLB}}$, $\overline{\text{EMPTYA}}$, and $\overline{\text{EMPTYB}}$ output flags. The $\overline{\text{FULLA}}$ and $\overline{\text{FULLB}}$ are definable full flags. A high-to-low transition on $\overline{\text{DAF}}$ stores the binary value of A0 through A4 into a register for use as the value of X. A high-to-low transition on $\overline{\text{DBF}}$ stores the binary value of B0 through B4 into a register for use as the value of Y. In this way, the depth of either FIFO can be defined to be one to thirty-two words deep. The value of X and Y must be defined after power-up or the stored value of X and Y will be ambiguous. The $\overline{\text{FULLA}}$ and $\overline{\text{FULLB}}$ outputs will be low when their corresponding memories are full and high when the memories are not full.

The $\overline{\text{EMPTYA}}$ and $\overline{\text{EMPTYB}}$ outputs will be low when their corresponding memories are empty and high when they are not empty. The status flag outputs are always active.

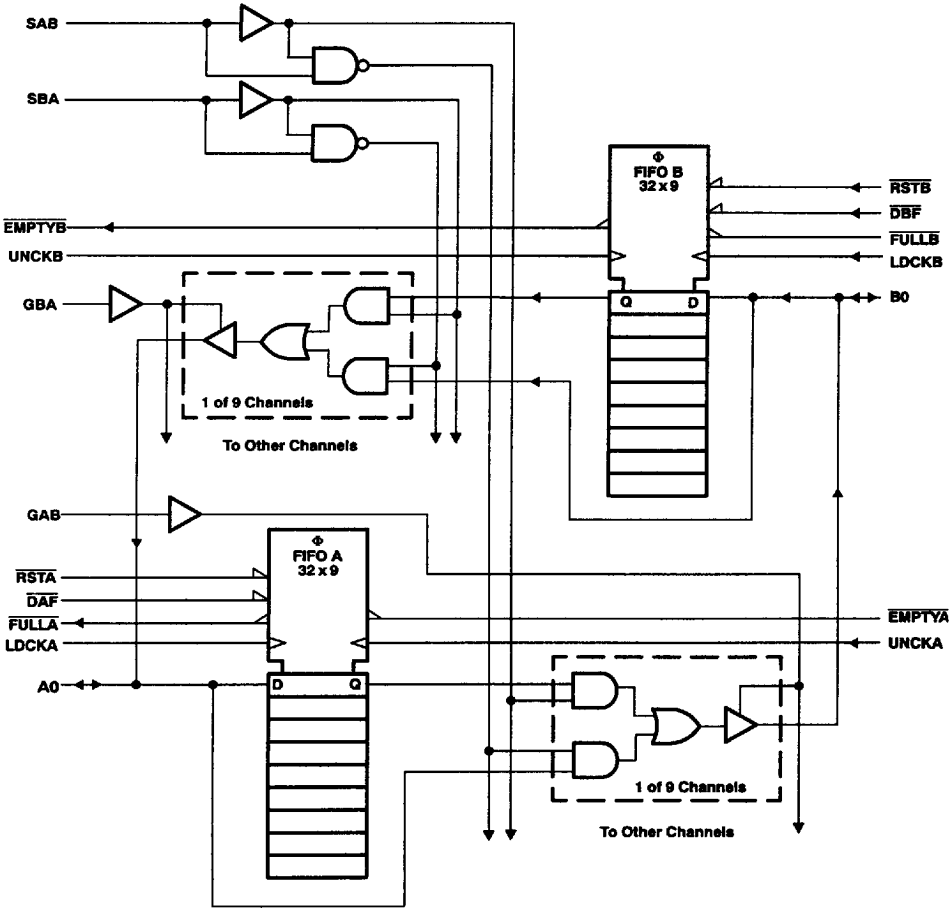
A low-level pulse on the $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$ inputs resets the control pointers on FIFO A or FIFO B and also sets $\overline{\text{EMPTYA}}$ low and $\overline{\text{FULLA}}$ high, or $\overline{\text{EMPTYB}}$ low and $\overline{\text{FULLB}}$ high. The outputs are not reset to any specific logic levels. With $\overline{\text{DAF}}$ at a low level, a low-level pulse on $\overline{\text{RSTA}}$ sets FIFO A to a depth of 32 minus X, where X is the value stored above. With $\overline{\text{DAF}}$ at a high level, a low level pulse on $\overline{\text{RSTA}}$ sets FIFO A to a depth of 32 words. The depth of FIFO B is set in a similar manner. The first low-to-high transition on LDCKA or LDCKB, either after a reset pulse or from an empty condition, will cause $\overline{\text{EMPTYA}}$ or $\overline{\text{EMPTYB}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

**logic symbol†**




† This symbol is in accordance with ANSI/IEEE Std 91-1984.
Pin numbers shown are for the N package.

**logic diagram (positive logic)**

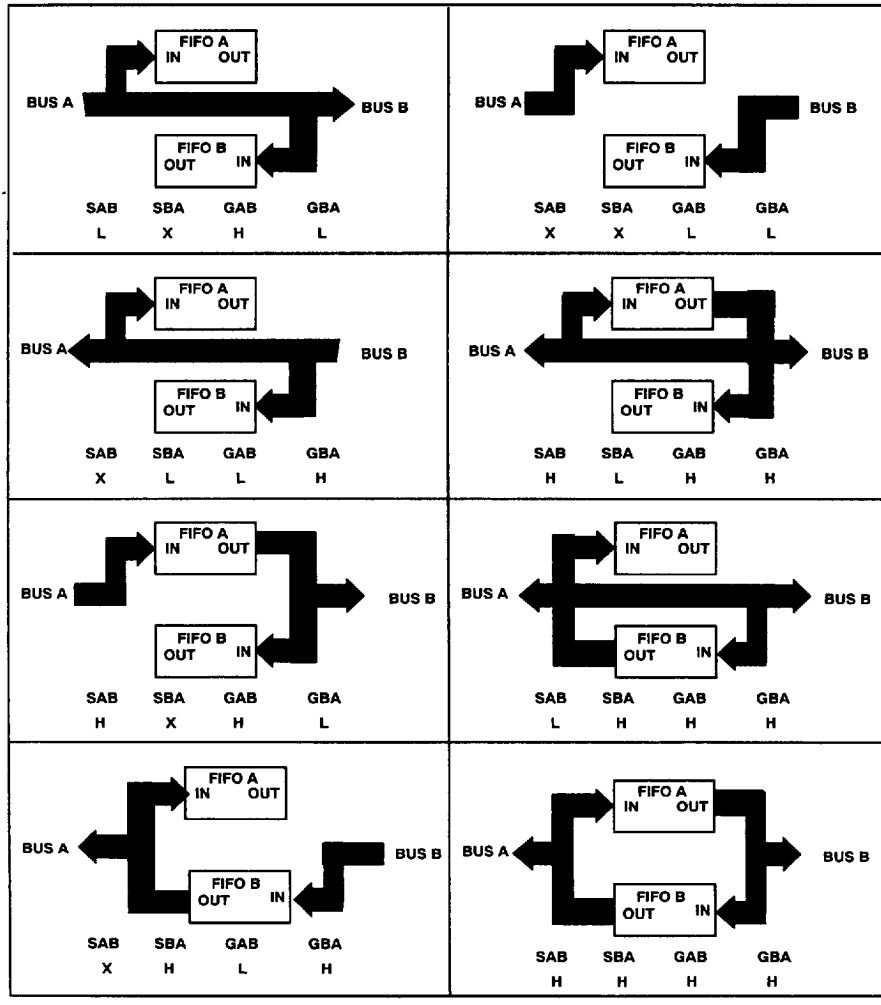




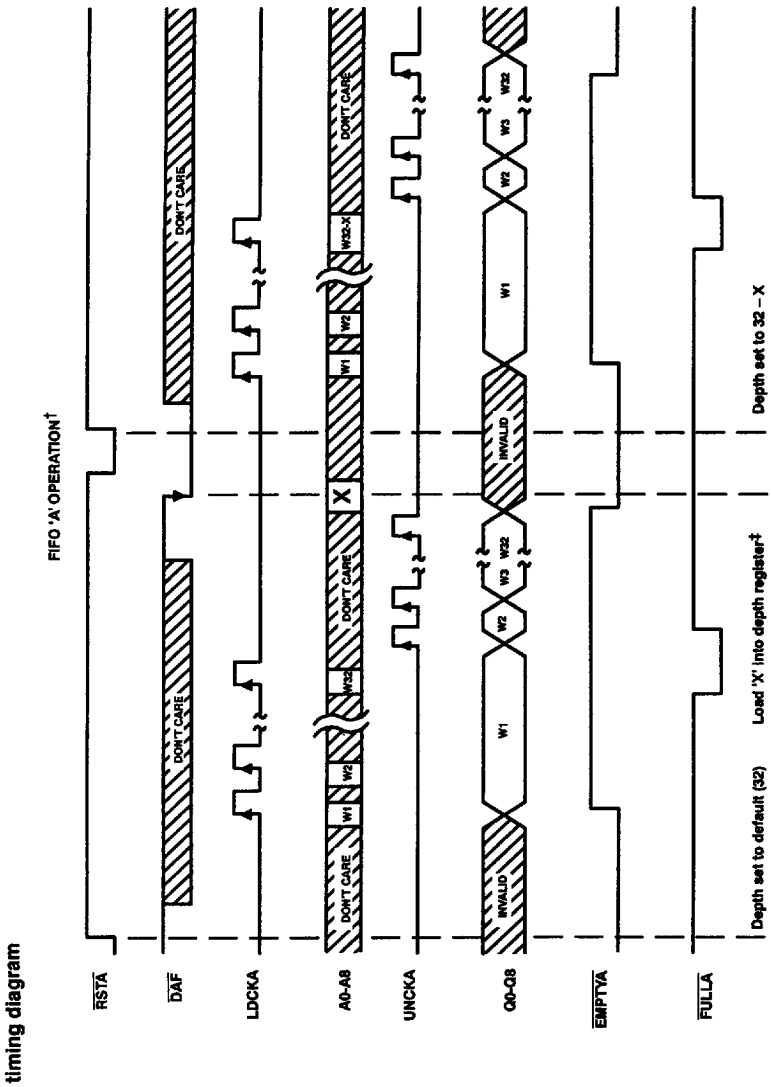

TEXAS INSTRUMENTS

8961723 0099330 678

## operating modes



## timing diagram




† Operation of FIFO 'B' is the same as shown above.
‡ 'X' includes A0 through A4 only. A5 through A8 are ignored.

## FUNCTION TABLES

**SELECT MODE CONTROL TABLE**

| CONTROL | | OPERATION | |
|---|---|---|---|
| SBA | SAB | A Bus | B Bus |
| L | L | Real Time B to A Bus | Real Time A to B Bus |
| H | L | FIFO B to A Bus | Real Time A to B Bus |
| L | H | Real Time B to A Bus | FIFO A to B Bus |
| H | H | FIFO B to A Bus | FIFO A to B Bus |

**OUTPUT ENABLE CONTROL TABLE**

| CONTROL | | OPERATION | |
|---|---|---|---|
| GBA | GAB | A Bus | B Bus |
| H | H | A Bus Enabled | B Bus Enabled |
| H | L | A Bus Enabled | Isolation/Input to B Bus |
| L | H | Isolation/Input to A Bus | B Bus Enabled |
| L | L | Isolation/Input to A Bus | Isolation/Input to B Bus |

### programming procedure for depth of FIFO A†

PROGRAM:

Step 1. With $\overline{\text{RSTA}}$ at a high level, take $\overline{\text{DAF}}$ from a high level to a low level. The high-to-low transition on $\overline{\text{DAF}}$ stores the binary value of A0-A4 for use as the value of 'X' in defining the depth of FIFO A.

Step 2. With $\overline{\text{DAF}}$ held low, pulse the $\overline{\text{RSTA}}$ signal low. On the low-to-high transition of $\overline{\text{RSTA}}$, FIFO A is set to a depth of 32 minus 'X', where X is the value of A0-A4 stored above.

Step 3. To redefine the depth of FIFO A to 32 words, hold $\overline{\text{DAF}}$ at a high level and pulse the $\overline{\text{RSTA}}$ signal low.

† The programming procedures used to define the depth of FIFO B are the same as the procedure above.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$ ..... – 0.5 V to 7 V
Input voltage: Control inputs ..... 7 V
I/O ports ..... 5.5 V
Voltage applied to a diabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Maximum junction temperature ..... 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions (see Note 1)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | A or B Ports | | | −15 | mA |
| | | Status flags | | | −0.4 | |
| $I_{OL}$ | Low-level output current | A or B Ports | | | 24 | mA |
| | | Status flags | | | 8 | |
| $f_{clock}$ | Clock frequency | LDCKA or LDCKB | 0 | | 40 | MHz |
| | | UNCKA or UNCKB | 0 | | 40 | |
| $t_w$ | Pulse duration | $\overline{RSTA}$ or $\overline{RSTB}$ low | 17 | | | ns |
| | | LDCKA or LDCKB low | 12.5 | | | |
| | | LDCKA or LDCKB high | 10 | | | |
| | | UNCKA or UNCKB low | 12.5 | | | |
| | | UNCKA or UNCKB high | 10 | | | |
| | | $\overline{DAF}$ or $\overline{DBF}$ high | 10 | | | |
| $t_{su}$ | Setup time | Data before LDCKA or LDCKB↑ | 7 | | | ns |
| | | Define Depth: D4-D0 before $\overline{DAF}$ or $\overline{DBF}$↓ | 6 | | | |
| | | Define Depth: $\overline{DAF}$ or $\overline{DBF}$↓ before $\overline{RSTA}$ or $\overline{RSTB}$↑ | 45 | | | |
| | | Define Depth (32): $\overline{DAF}$ or $\overline{DBF}$ high before $\overline{RSTA}$ or $\overline{RSTB}$↑ | 32 | | | |
| | | LDCKA or LDCKB (inactive) before $\overline{RSTA}$ or $\overline{RSTB}$↑ | 5 | | | |
| $t_h$ | Hold time | Data after LDCKA or LDCKB↑ | 3 | | | ns |
| | | Define Depth: D4-D0 after $\overline{DAF}$ or $\overline{DBF}$↓ | 4 | | | |
| | | Define Depth: $\overline{DAF}$ or $\overline{DBF}$ low after $\overline{RSTA}$ or $\overline{RSTB}$↑ | 0 | | | |
| | | Define Depth (32): $\overline{DAF}$ or $\overline{DBF}$ high after $\overline{RSTA}$ or $\overline{RSTB}$↑ | 0 | | | |
| | | LDCKA or LDCKB (inactive) after $\overline{RSTA}$ or $\overline{RSTB}$↑ | 5 | | | |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

NOTE 1: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCKA or LDCKB and UNCKA or UNCKB clock inputs. Any excessive noise or glitching on the clock inputs (which violates the $V_{IL}$, $V_{IH}$, or minimum pulse duration limits) can cause a false clock or improper operation of the internal read and write pointers.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | Status flags | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = −0.4 mA | $V_{CC}$−2 | | | V |
| | A or B ports | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −2 mA | $V_{CC}$−2 | | | |
| | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −3 mA | 2.4 | 3.2 | | |
| | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −15 mA | 2 | | | |
| $V_{OL}$ | A or B ports | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 24 mA | | 0.35 | 0.5 | |
| | Status flags | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | |
| | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | 0.35 | 0.5 | |
| $I_I$ | $\overline{DAF}$, $\overline{DBF}$, $\overline{RSTA}$, $\overline{RSTB}$, GAB, GBA, SAB, SBA, LDCKA, LDCKB, UNCKA, UNCKB | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| | A or B ports | | | | | 0.2 | |
| $I_{IH}$ | $\overline{DAF}$, $\overline{DBF}$, $\overline{RSTA}$, $\overline{RSTB}$, GAB, GBA, SAB, SBA, LDCKA, LDCKB, UNCKA, UNCKB | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | μA |
| | A or B ports‡ | | | | | 40 | |
| $I_{IL}$ | $\overline{DAF}$, $\overline{DBF}$, $\overline{RSTA}$, $\overline{RSTB}$, GAB, GBA, SAB, SBA, LCKA, LDCKB, UNCKA, UNCKB | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | −0.2 | mA |
| | A or B ports‡ | | | | | −0.4 | |
| $I_O$§ | A or B ports‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | −20 | | −130 | mA |
| | Status flags | | | −15 | | −100 | |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V | | | 190 | 350 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ For I/O ports, the parameters $I_{IH}$ and $I_{IL}$ include the offstate output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output ccurrent, $I_{OS}$.

**switching characteristics (see Note 2)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | |
| $f_{max}$ | LDCK | | 40 | | | MHz |
| | UNCK | | 40 | | | |
| $t_{pd}$ | LDCKA↑, LDCKB↑ | B/A | 7 | 22 | 33 | ns |
| $t_{pd}$ | UNCKA↑, UNCKB↑ | B/A | 7 | 20 | 29 | ns |
| $t_{PLH}$ | LDCKA↑, LDCKB↑ | $\overline{EMPTYA}$, $\overline{EMPTYB}$ | 5 | 12 | 22 | ns |
| $t_{PHL}$ | UNCKA↑, UNCKB↑ | $\overline{EMPTYA}$, $\overline{EMPTYB}$ | 5 | 12 | 22 | ns |
| $t_{PHL}$ | $\overline{RSTA}$↓, $\overline{RSTB}$↓ | $\overline{EMPTYA}$, $\overline{EMPTYB}$ | 5 | 12 | 22 | ns |
| $t_{PHL}$ | LDCKA↑, LDCKB↑ | $\overline{FULLA}$, $\overline{FULLB}$ | 5 | 12 | 22 | ns |
| $t_{PLH}$ | UNCKA↑, UNCKB↑ | $\overline{FULLA}$, $\overline{FULLB}$ | 5 | 12 | 23 | ns |
| $t_{LH}$ | $\overline{RSTA}$↓, $\overline{RSTB}$↓ | $\overline{FULLA}$, $\overline{FULLB}$ | 6 | 15 | 28 | ns |
| $t_{pd}$ | SAB/SBA‡ | B/A | 2 | 11 | 18 | ns |
| $t_{pd}$ | A/B | B/A | 2 | 8 | 15 | ns |
| $t_{en}$ | GBA/GAB | A/B | 2 | 6 | 15 | ns |
| $t_{dis}$ | GBA/GAB | A/B | 1 | 5 | 12 | ns |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.



TEXAS INSTRUMENTS