

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 1.27mm pitch SOIC, 0.65mm pitch SSOP,
0.635mm pitch QSOP, 0.65mm pitch TSSOP packages
- Extended commercial range of -40°C to +85°C
- V_{CC} = 3.3V ± 0.3V, Normal Range
- V_{CC} = 2.3V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVC821A:

- High Output Drivers: ±24mA
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION:

The LVC821A 10-bit bus-interface flip-flop is built using advanced dual metal CMOS technology. The LVC821A device features 3-state outputs designed specifically for driving highly capacitive or relatively low-imped-

ance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

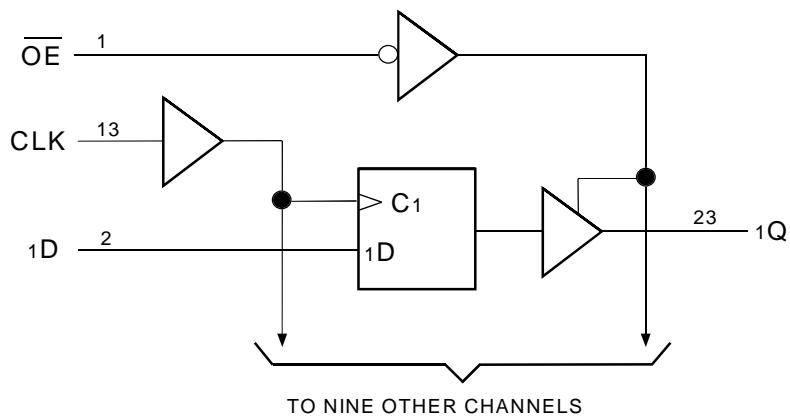
A buffered output-enable (OE) input can be used to place the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components. OE does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The LVC821A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

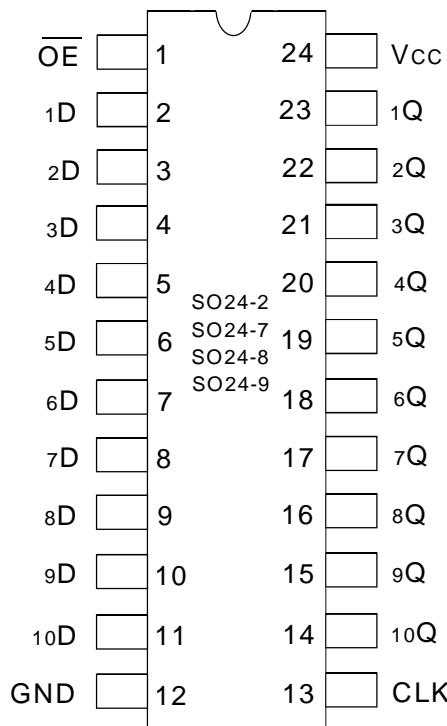
To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V system environment.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC/ SSOP/ QSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
VTERM(2)	Terminal Voltage with Respect to GND	- 0.5 to +6.5	V
VTERM(3)	Terminal Voltage with Respect to GND	- 0.5 to +6.5	V
TSTG	Storage Temperature	- 65 to +150	°C
IOUT	DC Output Current	- 50 to +50	mA
IIK	Continuous Clamp Current, VI < 0 or VO < 0	- 50	mA
Icc	Continuous Current through each Vcc or GND	±100	mA
Iss			

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NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. All terminals except Vcc.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOUT = 0V	5.5	8	pF
Ci/o	I/O Port Capacitance	VIN = 0V	6.5	8	pF

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NOTE:

1. As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
OE	Output-enable Input (Active LOW)
CLK	Clock Input
xD	Data Inputs
xQ	Data Outputs

FUNCTION TABLE (each flip-flop) (1)

Inputs			Outputs
OE	CLK	xD	xQ
L	↑	H	H
L	↑	L	L
L	H or L	X	Q ₀
H	X	X	Z

NOTE:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition

Q₀ = Level of Q before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^\circ\text{C}$ To $+85^\circ\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH} I _{IL}	Input Leakage Current	V _{CC} = 3.6V	V _I = 0 to 5.5V	—	—	± 5	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = 0 to 5.5V	—	—	± 10	μA
I _{OFF}	Input/Output Power Off Leakage	V _{CC} = 0V, V _{IN} or V _O \leq 5.5V		—	—	± 50	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{ICL} I _{ICCH} I _{ICCZ}	Quiescent Power Supply Current	V _{CC} = 3.6V	V _{IN} = GND or V _{CC}	—	—	10	μA
			3.6 \leq V _{IN} \leq 5.5V ⁽²⁾	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND		—	—	500	μA

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NOTES:

1. Typical values are at V_{CC} = 3.3V, $+25^\circ\text{C}$ ambient.
2. This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = -0.1mA	V _{CC} - 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = -6mA	2	—	
		V _{CC} = 2.3V	I _{OH} = -12mA	1.7	—	
		V _{CC} = 2.7V		2.2	—	
		V _{CC} = 3.0V		2.4	—	
		V _{CC} = 3.0V	I _{OH} = -24mA	2.2	—	
V _{OL}	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		V _{CC} = 2.7V	I _{OL} = 12mA	—	0.4	
		V _{CC} = 3.0V	I _{OL} = 24mA	—	0.55	

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NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	$V_{CC} = 2.5\text{V}\pm 0.2\text{V}$	$V_{CC} = 3.3\text{V}\pm 0.3\text{V}$	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance per flip-flop Outputs enabled	$C_L = 0\text{pf}, f = 10\text{Mhz}$	—	65	pF
CPD	Power Dissipation Capacitance per flip-flop Outputs disabled		—	48	pF

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	$V_{CC} = 2.5\text{V}\pm 0.2\text{V}$		$V_{CC} = 2.7\text{V}$		$V_{CC} = 3.3\text{V}\pm 0.3\text{V}$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}		—	—	150	—	150	—	MHz
t _{PLH}	Propagation Delay CLK to xQ	—	—	—	8.5	2.2	7.3	ns
t _{PZH}	Output Enable Time CE or xQ	—	—	—	8.8	1.3	7.6	ns
t _{PZL}	Output Disable Time CE or xQ	—	—	—	6.8	1.6	6.2	ns
t _W	Pulse Duration, CLK HIGH or LOW	—	—	3.3	—	3.3	—	ns
t _{SU}	Setup Time, Data before CLK	—	—	1.9	—	1.9	—	ns
t _H	Hold Time, Data after CLK	—	—	1.5	—	1.5	—	ns
t _{SK(0)}	Output Skew ⁽²⁾	—	—	—	—	—	1	ns

NOTES:

1. See test circuits and waveforms. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.
2. Skew between any two outputs of the same package and switching in the same direction.

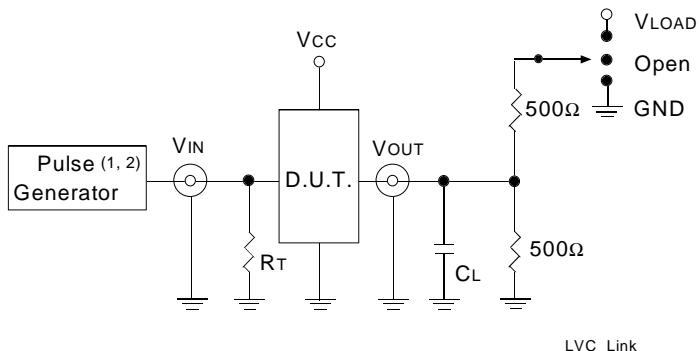
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC(1)} = 3.3V \pm 0.3V$	$V_{CC(1)} = 2.7V$	$V_{CC(2)} = 2.5V \pm 0.2V$	Unit
V_{LOAD}	6	6	$2 \times V_{CC}$	V
V_{IH}	2.7	2.7	V_{CC}	V
V_T	1.5	1.5	$V_{CC}/2$	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
 R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

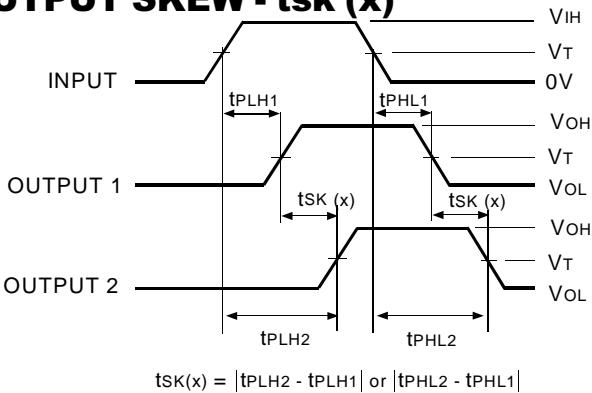
1. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$.
2. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_f \leq 2\text{ns}$; $t_r \leq 2\text{ns}$.

SWITCH POSITION

Test	Switch
Open Drain	V_{LOAD}
Disable Low	
Enable Low	
Disable High	GND
Enable High	
All Other tests	Open

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OUTPUT SKEW - $t_{SK}(x)$

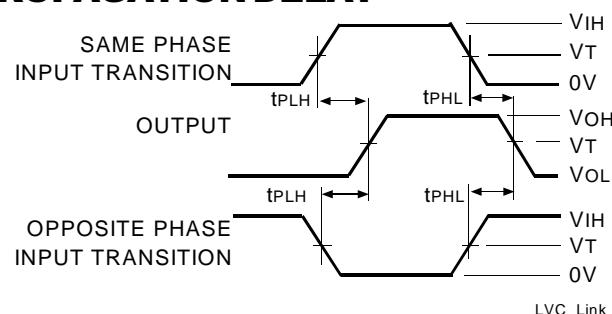


$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

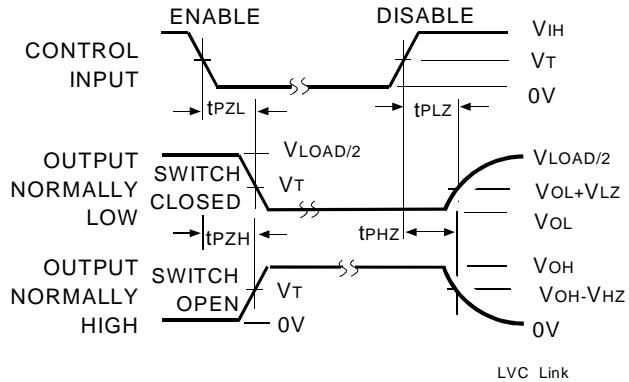
NOTES:

1. For $t_{SK}(o)$ OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK}(b)$ OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



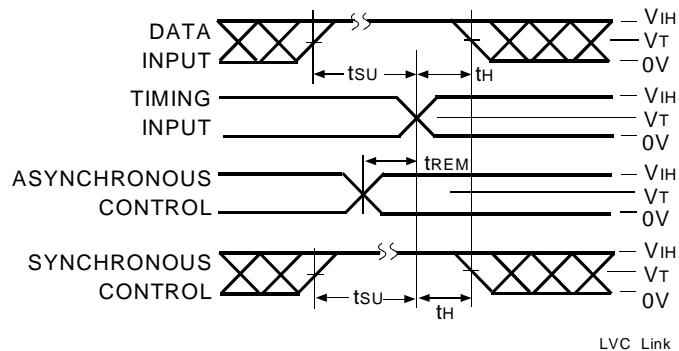
ENABLE AND DISABLE TIMES



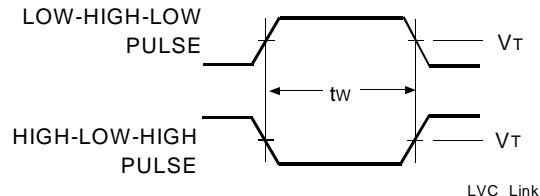
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



PULSE WIDTH



ORDERING INFORMATION

IDT XX LVC X XXXX XX
Temp. Range Bus-Hold Device Type Package

				SO	Small Outline IC (gull wing) (SO24-2)
				PY	Shrink Small Outline Package (SO24-7)
				Q	Quarter Size Small Outline Package (SO24-8)
				PG	Thin Shrink Small Outline Package (SO24-9)
			821A		10-Bit Bus-Interface Flip-Flop with 3-State Outputs, $\pm 24\text{mA}$
			Blank		No Bus-hold
		74			-40°C to $+85^\circ\text{C}$



CORPORATE HEADQUARTERS

2975 Stender Way
Santa Clara, CA 95054

for SALES:

800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com*

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